Novel nano-electromechanical relay design procedure for logic and memory applications

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ABSTRACT

This paper presents a rigorous design approach for (NanoElectroMechanical Structures/Systems) NEMS relays taking generalized nano-forces, *e.g.*, Casimir, van der Waals, into account for their static and dynamic modelling. Key in our approach is the proper definition of the critical pull-in and pull-out conditions as well as the derived non-latching and non-self-actuation conditions, thus improving on previous works that used simplified models and approximated designs.We extend the consistent description of the quasi-static actuation of NEMS devices in presence of nano-forces and present adimensional formulas describing their dynamic actuation in presence of multi-electrode. In particular, we demonstrate the use of these developments to dimension an inverter and a NAND gate in a configuration dominated by the Van der Walls interaction.

Keywords: nano force, adhesion, NEMS, logic gate, van der Waals

1 INTRODUCTION

This paper presents a rigorous design approach for (NanoElectroMechanical Structures/Systems) NEMS relays taking generalized Casimir and/or van der Waals forces into account for static and dynamic modeling. Key in our approach is the proper definition of the critical pull-in and pull-out conditions as well as the derived non-latching and non-self-actuation conditions, thus improving on previous works that used simplified models [1] and approximated designs [2].

NEMS have been the focus of an increasing attention from researchers in recent years for the alternative they offer to conventional CMOS for application in logics, memory and in digital circuitry in general. Scaled-down CMOS transistors suffer from energy-efficiency limitations imposed by the finite sub-threshold slope (large leakage current), which especially becomes troublesome for the sub-90nm devices [3]. Scaled-down NEMS on the other hand exhibit near-ideal switching characteristics, displaying a low effective threshold voltage combined with a near-zero leakage current and thus a low power consumption. Employing NEMS allows new functionalities providing an ideal platform to build multifunctional nanoscale ICs.

A typical electrostatically actuated NEMS relay implements a cantilever beam with two lower electrodes. The beam, actuation electrode and contact electrode are respectively the transistor-equivalent "source", "gate" and "drain" (Figure 1). In the OFF-state ("beam UP"), the source-drain current is nil. When the gate-source voltage V_{gs} reaches the pull-in voltage V_{pi}, electrostatic and elastic forces are unbalanced. The system becomes unstable. The beam collapses thereby closing the source-drain contact and a high and constant current I_{DS} flows (Figure 2). Scaling relays to nanometric dimensions, the surface nano-forces, such as Casimir and van der Waals forces, gain in importance and have to be accurately taken into account and modelled when designing the NEMS relay.

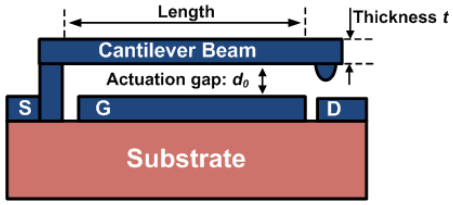


Figure 1 Basic NEMS relay: S source, G gate and D drain.

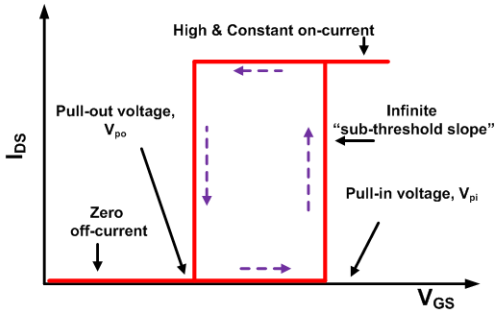


Figure 2 Ideal switching behaviour of a NEMS relay.

The NEMS design approach presented in [1] underestimates the effect of the Casimir force. Indeed as already reported in [2], the pull-in gap, in the presence of Casimir force, d_{pi}, converges, in the limit of V_{pi}=0V, towards d_{pi}=4/5d_0, which is much larger than d_{pi}=2/3d_0 assumed in [1]. We generalize this result to arbitrary nano-adhesion forces with gap dependencies of the form $1/d^n$. We derive self-actuation and latching conditions that are instrumental in our demonstration of inverter and NAND gate design in the presence of van der Waals adhesion force.

2 MODEL

For its modelling, the basic NEMS relay of Figure 1 can effectively be represented by the lumped spring-mass system of Figure 3. The deformable (cantilever) structure is modelled by a rigid plate with mass *m* supported by a linear spring of stiffness constant *k*. It is electrostatically actuated through a parallel-plate actuator of area S_e separated at rest by a vacuum gap of height d_0. A parasitic attractive nano-force F_a is assumed to follow the dependence given in eqn. (1). The forces are exerted across the actual gap *d* to the mobile plate through an actuator of area S_a. The family of forces described by eqn. (1) allows to describe the ideal parallel-plate Casimir or van der Waals interactions using the parameters of eqns. (2) and (3), respectively[1][2][4]. The differentiation of the coupling areas for electrostatic and nano-forces is used to scale both forces relative to each other and to eventually nullify the nano-effects and to make the link to the purely electrostatic actuation case.

$$F_a = \frac{\gamma S_a}{d^n} \tag{1}$$

$$\gamma_C = \frac{\pi^2 \hbar c}{240}, n_C = 4 \text{ and } S_a = S_C \tag{2}$$

$$\gamma_V = \frac{A}{6\pi}, n_V = 3 \text{ and } S_a = S_V \tag{3}$$

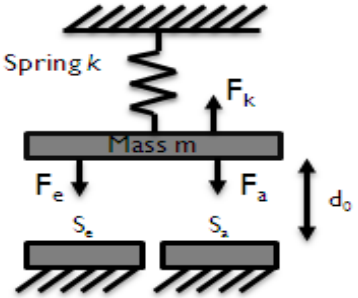


Figure 3 Lumped model of the cantilever relay of Figure 1 in the presence of a parasitic nano-force F_a.

2.1 Static behaviour modelling

The static behavior of the device modelled as in Figure 3 is described by the static force equilibrium expressed by eqn. (4). The nano-force F_a perturbates the normal electro-static actuation of the device and its instability characteristics, *i.e.* pull-in voltage V_{pi} and pull-in gap d_{pi}. These pull-in parameters are obtained by extracting the equilibrium voltage expression eqn. (5) from eqn. (4) and its maximum by differentiation as in eqn. (6).

$$F = k(d - d_0) + \frac{\varepsilon_0 S_e V^2}{2d^2} + \frac{\gamma S_a}{d^n} = 0 \tag{4}$$

$$V = \sqrt{\frac{2k}{\varepsilon_0 S_e}(d_0 - d)d^2 - \frac{2\gamma S_a}{\varepsilon_0 S_e d^{n-2}}} \tag{5}$$

$$\left.\frac{\partial V}{\partial d}\right|_{pi} = \sqrt{\frac{2k}{\varepsilon_0 S_e}\left(2d_0 d_{pi} - 3d_{pi}^2\right) + \frac{2(n-2)\gamma S_a}{\varepsilon_0 S_e d_{pi}^{n-1}}} = 0 \tag{6}$$

Eliminating γS_a between eqns. (5) and (6), V_{pi} is finally given by eqn. (7) as a function of the normalised d_{pi}, $d_{pi}^* \equiv d_{pi}/d_0$. Further, introducing the separation gap d_c remaining in the actuator upon tip-contact and $d_c^* \equiv d_c/d_0$, its normalized value, the pull-out voltage V_{po} is computed from eqn. (5) to give eqn. (8).

$$V_{pi} = \sqrt{\frac{2kd_0^3 d_{pi}^{*2}}{\varepsilon_0 S_e}\frac{n-(n+1)d_{pi}^*}{(n-2)}} \tag{7}$$

$$V_{po} = \sqrt{\frac{2d_0^2 d_c^{*2}}{\varepsilon_0 S_e}\left[k(1-d_c^*)d_0 - \frac{\gamma S_a}{d_0^n d_c^{*n}}\right]} \tag{8}$$

From the above two expressions, we derive the exact self-actuation limit, i.e., V_{pi}=0V, given by eqns. (9) and (10), as well as the latching limit, i.e. V_{po}=0V, given by eqn. (11).

$$d_{pi\_self}^* = \frac{n}{n+1} \tag{9}$$

$$\gamma S_{a\_self} = \frac{kn^n d_0^{n+1}}{(n+1)^{n+1}} \tag{10}$$

$$\gamma S_{a\_lat} = kd_0^{n+1}(1-d_c^*)d_c^{*n} \tag{11}$$

The limit pull-in gap, $d^*_{pi\_self}$, is purely defined by the power *n* of the gap dependence of the nano-force. Eqns. (10) and (11) provide maximum limits for the scaling of the considered nano force to ensure a non-latching, non-self-actuating function of a typical NEMS device. Note that the difference between S_{a_self} and S_{a_lat} can be used to produce non-self actuating but latching memory devices.

2.2 Dynamic behaviour modelling

The previous formalism can be extended to describe the dynamic behaviour of a NEMS device. The dynamics of the device from Figure 3 are driven by eqn. (12) where *m* is the mass of the mobile plate. This equation can be reorganised to produce the normalized eqn. (13), where $d^*=d/d_0$, $V^*=V/V_{pi}$, $\omega_0^2=k/m$ and eqn. (14) describes the link between $S_a^*=S_a/S_{a\_self}$.

$$m\ddot{d} + k(d - d_0) + \frac{\varepsilon_0 S_e V^2}{2d^2} + \frac{\gamma S_a}{d^n} = 0 \tag{12}$$

$$\frac{\ddot{d}^*}{\omega_0^2} + (d^* - 1) + \frac{n-(n+1)d_{pi}^*}{(n-2)}\frac{d_{pi}^{*2}V^{*2}}{d^{*2}} + \frac{2-3d_{pi}^*}{n-2}\frac{d_{pi}^{*n}}{d^{*n}} = 0 \tag{13}$$

$$S_a^* = \frac{(n+1)^{n+1}}{(n-2)n^n} d_{pi}^*(3d_{pi}^* - 2) \tag{14}$$

The dynamic pull-in point of the device under consideration can be derived from the analysis of the phase diagram described by eqns. (13) and (14) and in particular the identification of the saddle point, *i.e.*, the point where both the acceleration and the velocity are zero and that is not the static equilibrium position [5].

3 CASE STUDIES

3.1 Casimir regime: Basic device

In this section, Casimir nano-force, *i.e.,* nano-force parameters given in eqn. (2), are taken into account. In the static case, we use eqns. (13) and (14), ignoring the acceleration term, to generate Figure 4, presenting static equilibrium loci for increasing normalized Casimir surfaces S_C^*. The Casimir force reduces the stable portions of the actuation curves. When the critical Casimir pull-in surface is reached, the solution converges to d_{pi}=4/5d_0 (a result that can be easily derived from eq. (9)).

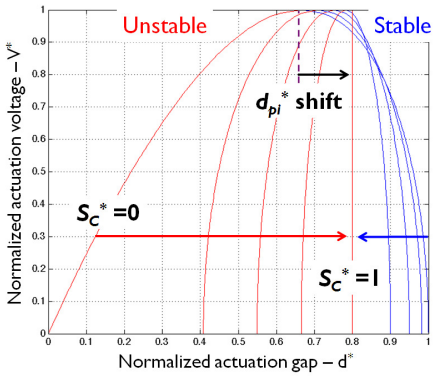


Figure 4 Equilibrium loci for S_c^* increasing from 0 to 1.

In the dynamic case, eqns. (13) and (14) produce the phase diagrams presented in Figure 5, Figure 6 and Figure 7, representing, respectively, Casimir-free, Casimir-impacted and Casimir-limit actuation under the same biasing voltage condition. In Figure 5, the dynamics are purely electro-static. The static equilibrium and dynamic pull-in positions are visible. Dashed trajectories and full orbits depict unstable and stable trajectories, respectively. Increasing S_c^* shifts static equilibrium and dynamic pull-in positions towards each other as shown in Figure 6. In the limit of S_c^*=1, in Figure 7, the stable orbits close on to the static equilibrium position that meets the dynamic pull-in point in d_{pi}^*=4/5. Note that V^*=0.5, but in this last case, V_{pi}=0V.

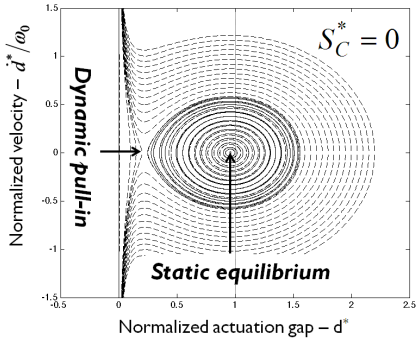


Figure 5 Phase diagram, V^* = 0.5 and no Casimir force.

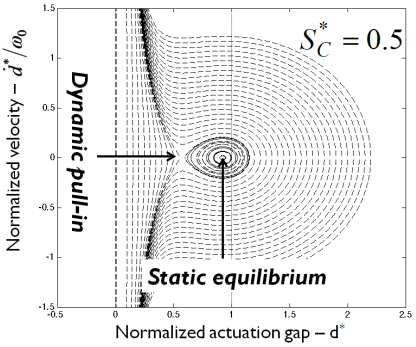


Figure 6 Phase diagram, V* = 0.5, medium Casimir force.

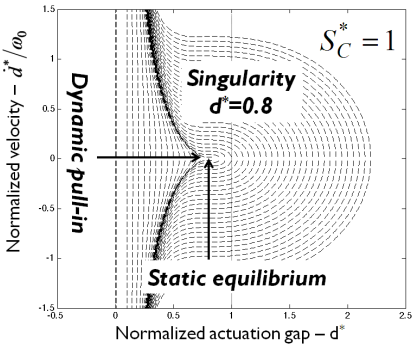
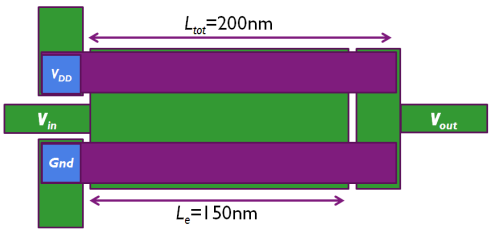


Figure 7 Phase diagram, V* = 0.5 and limit Casimir force.

3.2 Van der Waals regime: Inverter

A NEMS-based inverter circuit is shown in Figure 8. It is composed of two NEMS relays, i.e. cantilever beams respectively at V_{DD} and ground, subjected to an input voltage V_{in} applied to a common actuation electrode and producing an output V_{out} through the selective closure of the relays. With d_0=10nm, much smaller than typical plasma wavelengths, van der Waals interactions dominate. The sub-1V actuation voltage, no self-actuation and no-latching design goals are addressed through eqns. (7) and (9)-(11) with k=2Ebt^3/3L^3 [6], where a prismatic cantilever with rectangular cross section is assumed and t and b denote the thickness and width of the cantilever beam, respectively.



V_{in}	V_{out}
0	V_{DD}
V_{DD}	0

Figure 8 Inverter, and its truth table, implementing two nano-relays associated respectively to V_{DD} and ground d_0=10nm, d_c=6nm, t=10nm, E=117GPa, A=18.65 10^{-20}J.

The basic analytic dimensioning is verified by actuation simulations performed in COMSOL. The nano-force is implemented analytically through a face load boundary including a displacement feedback. The voltage sweep from Figure 9 confirms no self-actuation takes place and the pull-in occurs well below 1V. Further simulations confirmed that no secondary pull-in takes place upon contact and the device reopens upon bias removal.

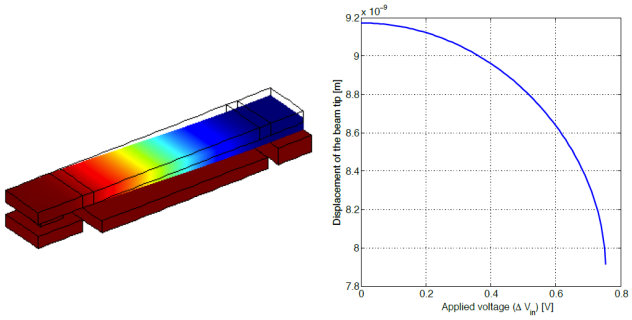
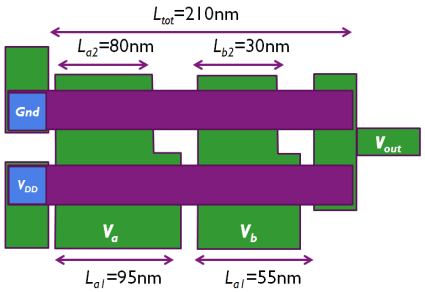


Figure 9 Simulated actuation characteristics of a nano-relay from the inverter of Figure 10.

3.3 Van der Waals regime: NAND gate

The NAND gate presented in Figure 10 implements two nano-relays subjected each to two actuation signals through two electrodes with different overlap areas. By proper dimensioning, these devices can generate the required truth table. Note for example that the electrodes below the V_{DD} beam are large so that one grounded electrode is enough to pull it in. On the contrary, the electrodes below the grounded beam are limited so that it only pulls in when both electrodes are at V_{DD}. The introduction of different S_e and S_a in eqns. (4)-(14) allows designing and verifying all the configurations of the NAND truth table, the non-self-actuation and non-latching to ensure the right state transitions. Comsol simulations presented in Figure 11 confirm the validity of our dimensioning. Note the different portions of each beam denoting the areas where nano-forces are applied.



V_a	V_b	V_{out}
0	0	V_{DD}
V_{DD}	0	V_{DD}
0	V_{DD}	V_{DD}
V_{DD}	V_{DD}	0

Figure 10 NAND gate, and its truth table, implementing two nano-relays associated respectively to V_{DD} and ground and two inputs with non-equal electrode widths d_0=10nm, d_c=6nm, t=10nm, E=117GPa, A=18.65 10^{-20}J.

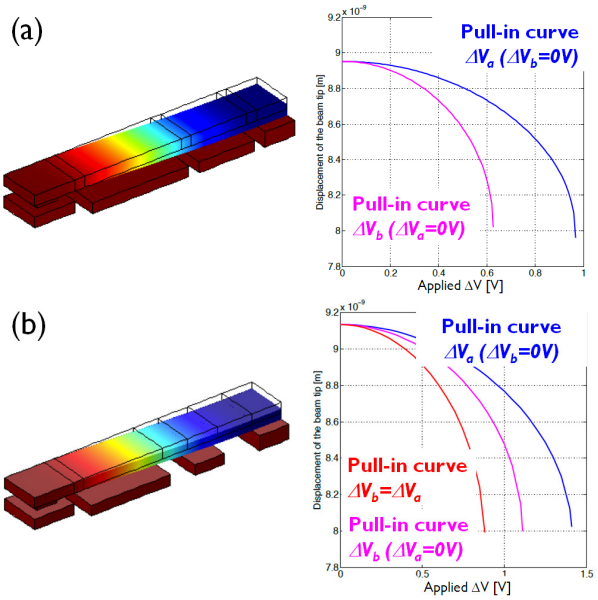


Figure 11 Simulated actuation of the NAND of Figure 10; (a) V_{DD}-beam closes with at least one electrode at 0V and (b) ground-beam closes only with both inputs at V_{DD}=1V.

4 CONCLUSIONS

We presented a rigorous design approach for NEMS relays taking generalized nano-forces into account for their static and dynamic modelling. Key in our approach is the proper definition of the critical pull-in and pull-out voltages as well as the derived non-latching and non-self-actuation conditions. In particular, we demonstrated the design and dimensioning of an inverter and a NAND gate in a configuration dominated by the van der Walls interaction.

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