MIM Capacitors with stacked dielectrics

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ABSTRACT

The SiO_2/Si_3N_4 stacked dielectric is proposed as apossible candidate for realizing metal–insulator–metal (MIM) capacitor. MIM capacitors have been fanricated with single as well as stacked dielectic layers. C-V and I-V characteristics of these devices have been studied. SiO_2 deposited by PECVD, is having lower plasma enhanced traps and hence lower frequency dispersion as compared to Si_3N_4. However, capacitance density is found to be lower for SiO_2 and higher for Si_3N_4. Hence a stack of oxide and nitride is being proposed as a promising candidate as dielectric. This has been found to be resulting in lower frequency dispersion. It has also been observed that post metallization anealing is very effective in improving the characteristics in all cases. The leakage current densities at −0.55V and −1V for nitride-oxide stacked structure are 60pA/cm^2 and 277pA/cm^2, respectively.

Keywords: Stacked dielectric, pre-metallization-annealing, post-metallization-annealing, voltage coefficient of capacitance (VCC).

1 INTRODUCTION

Metal-insulator-metal (MIM) structure is a simple passive device that has been extensively studied due to the vista of high-speed operation, high-density integration, and an excellent process compatibility with the present complementary metal oxide semiconductor CMOS technology [1, 2]. However, increased level of integration and reduced feature size have resulted in many limitations such as higher amount of frequency dispersion, lower values of quality factor and high values of VCC. In addition to these, reduction in the dielectric film thickness have also led to increased leakage current density and reduced breakdown voltage. Different methods have been proposed to improve the characteristics of MIM capacitors [1,3].

In this work SiO_2/Si_3N_4 stack is proposed as the dielectric for MIM device. MIM capacitors have been fabricated and Capacitance Voltage (C-V) and current Voltage (I-V) characteristics have been studied. The effect of post metalization annealing on the electrical characteristics have been investigated. It has been observed that MIM devices with stacked dielectric have lower frequency dispersion, reduced leakage currents and increased breakdown voltage when compared to MIM devices with single dielectric. The

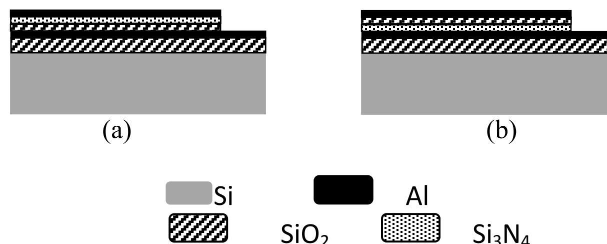

Fig.1. Sectional view of MIM capacitors (a) with dielectric SiO_2-Si_3N_4 (b) with dielectric Si_3N_4- SiO_2

peroformance of MIM devices have been significantly improved when these devices have been subjected to post-metallization-annealing.

2 EXPERIMENTAL WORK

MIM capacitors have been realized on p-type (100) silicon substrates with resistivity of 0.1 to 0.2 Ω cm. Filed oxide of thickness 500 nm has been grown by wet oxidation at 1000 °C after preparing the Si wafers with standard cleaning procedure to ensure the substrate isolation. Al, used as the bottom electrode has been deposited by thermal evaporation. This has been followed by four schedules of plasma enhanced chemical vapour deposition (PECVD). A part of the bottom electrode has been masked during PECVD deposition for bottom electrode contact. Four types of dielectrics viz. (i) only oxide (SiO_2), (ii) only nitride (Si_3N_4), (iii) stack of both with oxide at bottom and nitride on top (SiO_2/Si_3N_4) and (iv) stack with nitride at bottom and oxide on top (Si_3N_4/SiO_2) have been deposited over two sets of samples each. SiO_2 has been deposited at 300 ^oC for 2 minutes and Si_3N_4 has been deposited at 350 ^oC for 1 minute in each of the respective cases. PECVD deposition has been immediately followed by Aluminium top electrode deposition by thermal evaporation. MIM capacitors have been realized by patterning the top metal with circular regions of 100 μm diameter. Sectional view of the MIM capacitors with SiO_2/Si_3N_4 and Si_3N_4/SiO_2 stack dielectrics are shown in Fig.1(a) and Fig.1(b) respectively. One set of samples in each of the four dieletctrics mentioned above have been subjected to post metallization annealing at 400°C in N_2 ambient for 10 minutes. Capacitance voltage (C-V) and current voltage (I-V) characteristics have been measured using Agilent B1500A semiconductor device analyzer.

3. RESULTS AND DISCUSSIONS

3.1 C-V Characteristics with single dielectric

Normalized C-V characteristics of MIM capacitors measured at 100 kHz and 1 MHz, with SiO_2 and Si_3N_4 as the dielectric are shown in Fig.2. C-V Characteristics of MIM devices for which post metalization annealing (PMA) have been carried out are also included in Fig.2 for comparison. It can be observed that both the MIM capacitors with single dielectrics suffer from the problem of higher frequency dispersion. The amount of frequency dispersion is found to be lower in MIM devices with SiO_2 as the dielectric compared to those with Si_3N_4 as the dielectric. This can be attributed to the presence of large bulk nitride traps located within the tunnelling distance of the nitride/metal interface such that they are capable of modulating the total capacitance with different time constants [4]. It can also be seen from the C-V characteristics that even though post metallization annealing reduces frequency dispersion, it is not effective in eliminating the same. Another important observation is that MIM capacitors with nitride as the dielectric yielded higher values of capacitance density when compared with those with oxide as the dielectric. Capacitance density is one of the crucial concerns in MIM capacitors because they occupy much area in a chip. Hence from the C-V characteristics of MIM capacitors with single dielectrics, it is observed that MIM capacitors with oxide as dielectric has minimum frequency dispersion and very low capacitive density. However, MIM capacitors with nitride as dielectric have higher frequency dispersion and higher capacitive density when as compared with those with oxide as the dielectric. This is matching with the previous reports as well [4, 5]. Hence to obtain a dielctric layer with lower values of frequency dispersion and higher values of capacitance density, it was decided to stack both oxide and nitride in the same device and study the characteristics.

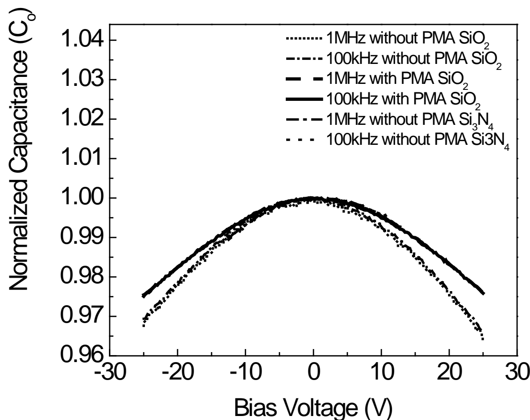

Fig. 2: Normalized CV characteristics of MIM capacitors with SiO_2 and Si_3N_4 as dielectrics at 100 kHz and 1 MHz with and without PMA

3.2 C-V Characteristics with dielectric stack

Normalized C-V characteristics of MIM capacitors measured at 100 kHz and 1 MHz, with SiO_2/Si_3N_4 as the dielectric are shown in Fig.3 and that of MIM capacitors with Si_3N_4/SiO_2 as the dielectric are shown in Fig.4 respectively. C-V characteristics for these devices after PMA are also included in these figures for comparison. It can be observed from these characteristics that stacked dielectrics exhibit lower amount of frequency dispersion when compared with MIM devices with single dielectrics. Further, it can be seen that PMA has resulted in significant improvement in frequency dispersion for these devices. has been obtained for MIM devices with stacked dielectrics.

Voltage Coefficient of Capacitance (VCC) can be approximated by the equation

$$C(V) = C_o(\alpha V^2 + \beta V + 1) \qquad (1)$$

where V is the voltage applied between the electrodes of the capacitor, and C_0 is the capacitance at zero voltage. α, β are the quadratic and linear VCC, respectively as determined by using a second order polynomial curve fit to measured data. The quadratic VCC (α value) is critical for the dynamic range of analog circuit [6, 7]. The linear VCC (β value) can be cancelled out by differential techniques such as cross-coupled arrangement [8]. The quadratic and linear coefficients for MIM with various dielectrics are calculated by quadratic curve fitting of the normalized CV plots and are presented in Table 1. The values of α and β extracted from the C-V characteristics are plotted in Fig. 5-8. Values of α for MIM devices without PMA is given in Fig. 5 and those with PMA is given Fig. 6. Similarly values of β for MIM devices without PMA is given in Fig. 7 and those with PMA is given in Fig. 8. Extracted values of α and β obtained for all devices are presented in Table 1. Significant improvement in the values of α and β have been obtained for devices when subjected to PMA. It is seen that the values of α and β decreases with the annealing treatments

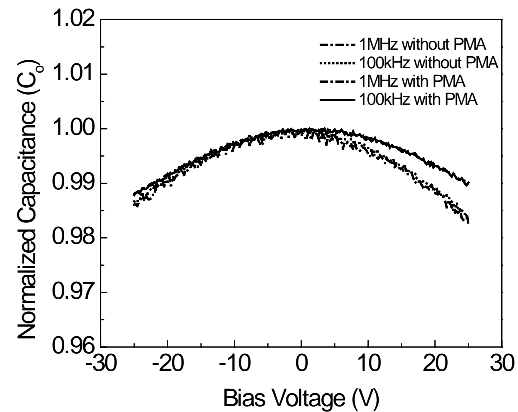

Fig. 3: Normalized CV characteristics of MIM capacitors with SiO_2/Si_3N_4 stack as dielectric at 100 kHz and 1 MHz with and without PMA

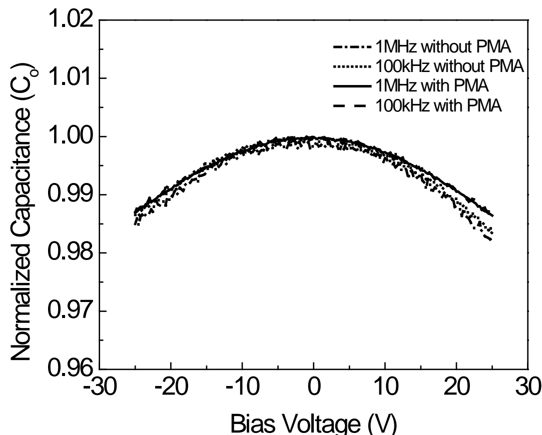

Fig.4: Normalized CV characteristics of MIM capacitors with Si_3N_4/SiO_2 stack as dielectric at 100 kHz and 1 MHz with and without PMA

on MIM devices. This decrease in VCC is due to the reduction in the plasma-enhanced trap generation in the bulk of the nitride. The capacitor charge at some particular frequencies may be strongly influenced by the different trap sites causing charge relaxation that can be smaller or bigger than the exitation wave period being used for the measurements [8]. Also the asymmetry of carrier depletion or injection in the dielectric at top and bottom electrodes is reduced due to annealing. Oxygen vacancies are recognized as one of the most important defect at the interface layer between oxide and nitride causing charge trapping. The decrease in α value indicates a decrease in the charge trapping due to oxygen vacancies existing at the oixide-nitride interface layer.

3.3 I-V Characteristics of MIM Capacitors

The current voltage characteristics of MIM devices without PMA is given in Fig. 9 and those of MIM devices without PMA is given in Fig.10. It is seen that annealing has decreased the leakage current drastically. The annealing has caused a decrease in the settling of dangling bonds at the interface of the SiO_2/Si_3N_4 stacked layers [3]. An excellent source of hydrogen for further passivating the interface states, can be obtained when the silicon nitride is deposited using the plasma-enhanced chemical vapour deposition (PECVD) technique [2]. The hydrogen diffusing from the PECVD silicon nitride on to the silicon dioxide surface is responsible for the reduction in the value of the interface state density. According to ITRS the leakage current density should be less than $10nA/cm^2$ at 1V in 2009 and 0.55V in 2011 respectively. The leakage current density of MIM capacitors are presented in Table 1. It can be seen that PMA is very effective in reducing the leakage currents for the devices.

Hence it has been observed that MIM capacitors with stacked dielectrics shows better characteristics when compared with MIM devices with single dielecrics. MIM capacitors with stacked dielectrics show lower frequency dispersion, higher capacitance density, lower values of VCC, lower leakage currents and higher break down voltage. Hence MIM devices with SiO_2/Si_3N_4 and Si_3N_4/SiO_2 stack as dielecric layers are proposed as better candidates for realizing MIM devices. The reliability characteristics of these devices are being studied currently.

5. ACKNOWLEDGEMENT

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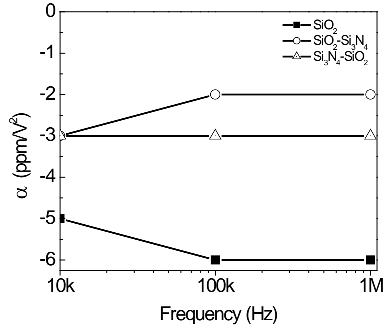

Fig.5: α variation without PMA

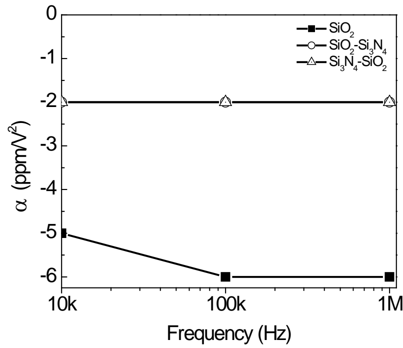

Fig.6: α variation with PMA

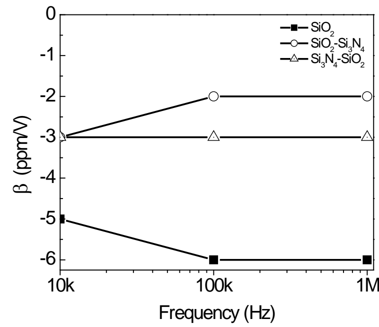

Fig.7: β variation without PMA

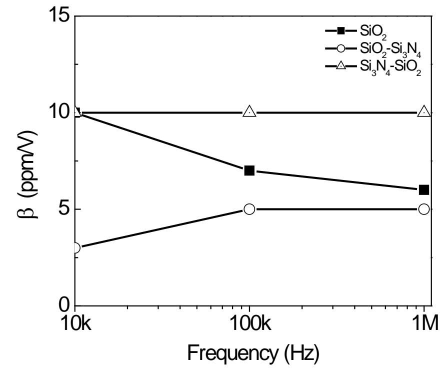

Fig.8: β variation with PMA

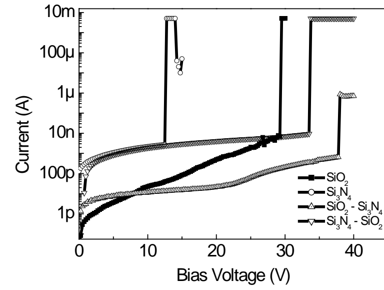

Fig.9: IV Plot for MIM capacitor without PMA

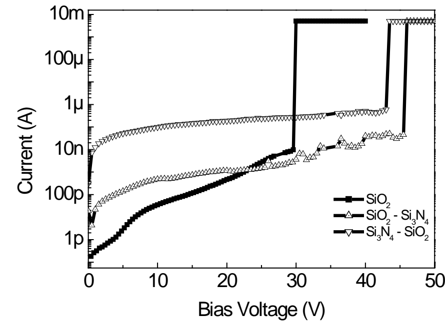

Fig.10: IV Plot for MIM capacitor with PMA

	Without PMA		**With PMA**		**Without PMA**		**With PMA**		**Without PMA**		**With PMA**	
	α (ppm/V²)	β (ppm/V)	α (ppm/V²)	β (ppm/V)	α (ppm/V²)	β (ppm/V)	α (ppm/V²)	β (ppm/V)	α (ppm/V²)	β (ppm/V)	α (ppm/V²)	β (ppm/V)
10kHz	-5	10	-5	10	-3	7	-2	3	-3	6	-2	10
100kHz	-6	7	-6	7	-2	6	-2	5	-3	6	-2	10
1MHz	-6	6	-6	6	-2	8	-2	5	-3	5	-2	10
Breakdown voltage	29.25V		30V		44.5V		39V		43V		45.5V	
Breakdown current Density $A/_{cm^2}$	2.209×10^{-5} **@29.25V**		1.1209×10^{-5} **@29.25V**		16.85×10^{-5} **@39V**		1.901×10^{-5} **@39V**		148.186×10^{-5} **@43V**		1.279×10^{-5} **@45.5V**	

Table 1:Summary of properties