Advances in MEMS Fabrication for Fabless MEMS Companies

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ABSTRACT

MEMS was founded on unique processes and structures based around standard semiconductor fabrication techniques. Only recently, with the massive popularity of micro-sensors in consumer electronics has MEMS become a viable mainstream manufacturing technology. As a fabless company, InvenSense was not encumbered by any legacy fabrication technology and has developed a process platform that is conducive to rapid product development and high volume manufacturing. The Nasiri-Fabrication™ (NF) Platform is described, incorporating single-crystal bulk silicon, direct integration to CMOS electronics, and wafer level packaging. This combination represents the latest evolution in MEMS fabrication. Attributes and benefits of the NF platform addressing basic challenges of high volume MEMS production are highlighted.

Keywords: fabless, platform, integration, MEMS, Nasiri-Fabrication

1 INTRODUCTION

MEMS technology is rapidly gaining acceptance as a viable and reliable solution to a number of technical challenges including navigation, timing, imaging, medical diagnostics, and many others. However, unlike the standardization that occurred in the semiconductor industry to enable the myriad of current fabless CMOS companies, MEMS has largely stayed with the one product, one process paradigm. Furthermore, the difficulty and burden of custom process development for each new device has been a major challenge and hindrance to achieving volume production for many MEMS companies. We will describe a fabrication approach developed by InvenSense, representing the latest advancement in MEMS (Figure 1), which is flexible, attractive to high volume foundries and therefore well suited for fabless MEMS players.

2 MEMS CHALLENGES

Often, in the MEMS industry, device development is based on available processes, whether at a university, in-house fab, or MEMS foundry. The temptation to reach a proof of concept must be tempered by the recognition that manufacturing and production are critical components to commercial success. Historically MEMS devices are differentiated by their fabrication platform giving a false sense of value as a barrier to entry and intellectual property.

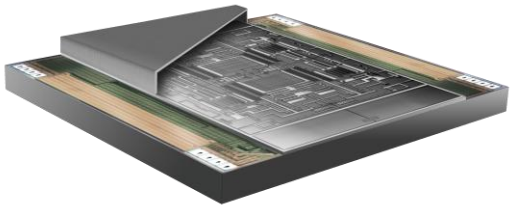

Figure 1. NF Platform integrated CMOS-MEMS device.

In fact one can argue that this process uniqueness will instead present obstacles to product success, especially in consumer electronics where high volume challenges of high ramp rate, capacity, and delivery must be met. Moreover, product cost, of which the MEMS component may only be 20% or less must be fully recognized and addressed.

2.1 Development

Process development has traditionally been the most difficult, costly, and time consuming portion of MEMS development. Building up in-house fabrication facilities with sufficient capabilities and process control is typically prohibitively expensive for a fledgling company. However, using external foundries, while generally lower risk, makes the user dependent on the foundries' capabilities, which may not always match the requirements of the new process; as well as the foundries' commitment of resources and equipment to the product, which may not be high for a new unproven product and company.

2.2 Manufacturing

Once the initial process is developed and the product prototyped, transfer to manufacturing becomes the next big challenge. Once again, with a new and unproven process, the step from demonstration to a fully stable and reliable manufacturable process is often a big one. In fact this step typically requires a much larger outlay of time and resources than the initial development. More than one company has faltered at this stage, unable to achieve yields and reliability requirements.

2.3 Cost

Another critical aspect of bringing a MEMS product to market is the ultimate product cost. However, more often than not for traditional MEMS, the cost of a MEMS product is much more determined by the cost of packaging and testing than the MEMS chip itself. In fact packaging and test for traditional MEMS devices often comprises nearly

80% of the product cost, due to multi-chip package complexity (Figure 2). Failure to realize and account for this reality often leads to great MEMS ideas with a cost-prohibitive implementation.

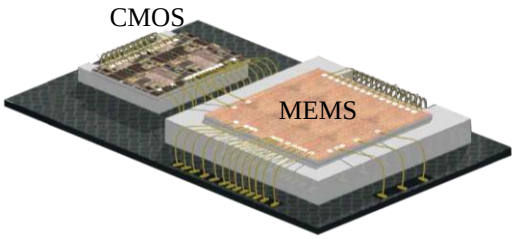

Figure 2. Traditional 2-chip MEMS-CMOS package.

3 NF PLATFORM

The fundamental benefit of NF platform is in its simple MEMS process and its integration to CMOS. This platform produces wafer with sealed and electrically interconnected self-contained die that may be treated, processed, and packaged like a standard CMOS wafer (Figure 3).

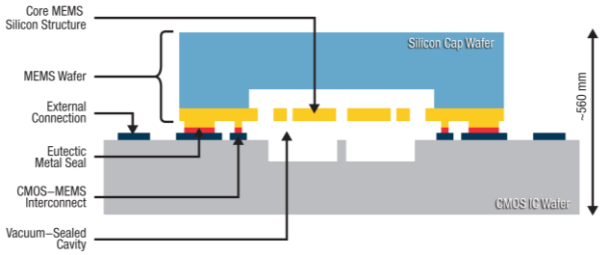

Figure 3. NF platform wafer-level CMOS-MEMS integration.

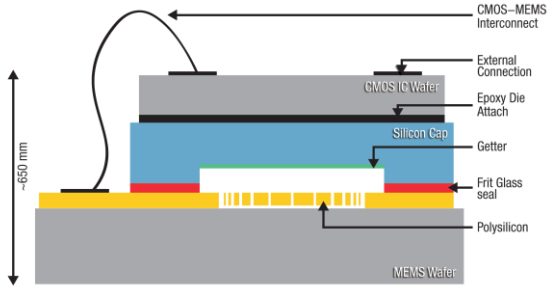

Figure 4. Traditional MEMS to CMOS interconnect using chip-stacking and wire-bond.

Contrast the NF platform to conventional MEMS approaches (Figure 4) where a MEMS wafer is fabricated and capped with a separate capping wafer. The combined stack is then outfitted for interconnection to an ASIC, where the MEMS and CMOS die are connected either in a side by side or vertical stack configuration. Rudimentary testing can be performed on the capped MEMS wafer but extensive test and trim is only accomplished at the completed package level.

3.1 NF Platform – MEMS

Figure 5 illustrates the process sequence, which contains a total of 5 mask layers. A double-side polished silicon wafer is used as the starting substrate and serves as the handle wafer. Shallow features are etched on one side to serve as backside alignment targets (Figure 5a). Cavities are then patterned on the opposite surface and aligned to the backside targets (Figure 5b). The cavities, typically etched in a reactive ion etcher, will define movable and stationary portions of the MEMS structure. A silicon dioxide layer is deposited either thermally or via CVD, with a thickness determined by the isolation or parasitic capacitance requirement of the device. The oxide surface of the completed handle wafer is then bonded to a separate silicon device wafer using a direct bonding technique, and the bonded stack is annealed to enhance its bond strength. Infrared inspection of the wafer and isolated posts formed by the cavity pattern is used for in-line process monitoring to detect any bond defects. The device wafer goes through a grind and polish process to achieve the desired device layer thickness. This single crystal silicon layer serves as the MEMS structural material. The resulting fully bonded wafer with cavities is referred to as an Engineered Silicon on Insulator (ESOI) wafer (Figure 5c).

A third masking step followed by a controlled silicon etch is used to create standoffs on the device wafer surface (Figure 5d) that will define both mechanical and electrical contacts to the CMOS and also serve to define a controlled gap between moveable MEMS structures and the CMOS electrodes. Germanium is then deposited using conventional sputtering techniques and patterned over the standoffs using a phosphoric based etchant (Figure 5e). The next masking and etch step patterns the device layer defining the MEMS structures (Figure 5f). The topology of standoff and Ge is sufficiently shallow to allow fine line lithography at this step and realization of less than 2 um features in the device layer. Deep reactive ion etch (DRIE) with easily achievable 20:1 aspect ratio defines the structure. After photoresist removal the MEMS wafer is complete.

3.2 NF Platform – Wafer level CMOS integration

The CMOS wafer is fabricated using a conventional process available at any CMOS foundry. Options with high voltage, memory, metal capacitors and high resistivity polysilicon resistors are available. It is worth noting that since the MEMS wafer is fabricated separately from CMOS, the CMOS process is not restricted or compromised by the MEMS process in any way. The CMOS wafer undergoes standard wafer acceptance testing (WAT) prior to bonding to the MEMS wafer. Depending on MEMS device requirements, a bottom cavity may be etched in portions of the CMOS wafer to allow greater clearance for

any vertically moving structures (Figure 5g). Top aluminum metallization of the CMOS wafer is used as the mating surface to the germanium on the MEMS. Both sets of wafers are cleaned and placed in an automated wafer bonder. The bond process consists of aligning the two wafers on a bond chuck which is then transferred into the bond chamber. The bond chamber is evacuated to a desired pressure, and the wafers are pressed together and heated with a programmed temperature profile to initiate a eutectic bond between the aluminum and germanium which nominally occurs at 423° C. After this stage, each MEMS die is hermetically sealed and electrically interconnected to the CMOS (Figure 5h). Finally, the wafers are ground to a desired final thickness, and CMOS wire-bond pads are exposed using a dicing tab removal process (Figure 5i). A cross-section of a completed CMOS-MEMS die is shown in Figure 6.

4 BENEFITS AND ATTRIBUTES

As can be seen from the process flow, NF platform provides a number of benefits for the designer - stable and well characterized single crystal silicon structural material, wafer-level sealing and interconnect, intimate CMOS integration, and compatibility with high volume foundries. These attributes will now be described in more detail.

4.1 Versatile MEMS Platform

The silicon device layer of the ESOI wafer offers a versatile mechanical material for MEMS design. The single crystal bulk material is stress-free, fracture-resistant, and can be thinned to any desired thickness. Lateral transduction is achieved by well established DRIE etch, and integration to CMOS enables the use of its metal layers as electrodes to support vertical transduction. This aspect was critical to the success of InvenSense 3-axis gyroscope where the sense architecture was based on lateral displacement detection caused by the Coriolis force, which then required drive motion of the masses to be along the z axis. The ability to use a thick (20 to 50um) structural layer yields a design with high out-of-plane mode rejection and increased sense capacitance for lateral displacement sensing. Furthermore, it allows creation of high frequency and large proof mass structures in a very compact volume. However, since the device layer thickness is fully customizable, MEMS structures requiring thin silicon layers are also possible.

With advances in DRIE technology, foundries can support device size reduction as lateral transduction efficiencies increase with smaller gaps and higher aspect ratios, leading to lower die cost.

MEMS yield is enhanced by the dry release process enabled by the combination of DRIE etch and previously etched cavities in the handle wafer. This approach eliminates the need for troublesome sacrificial wet or vapor etch steps, thereby avoiding many of the yield issues of traditional MEMS such as stiction or breakage.

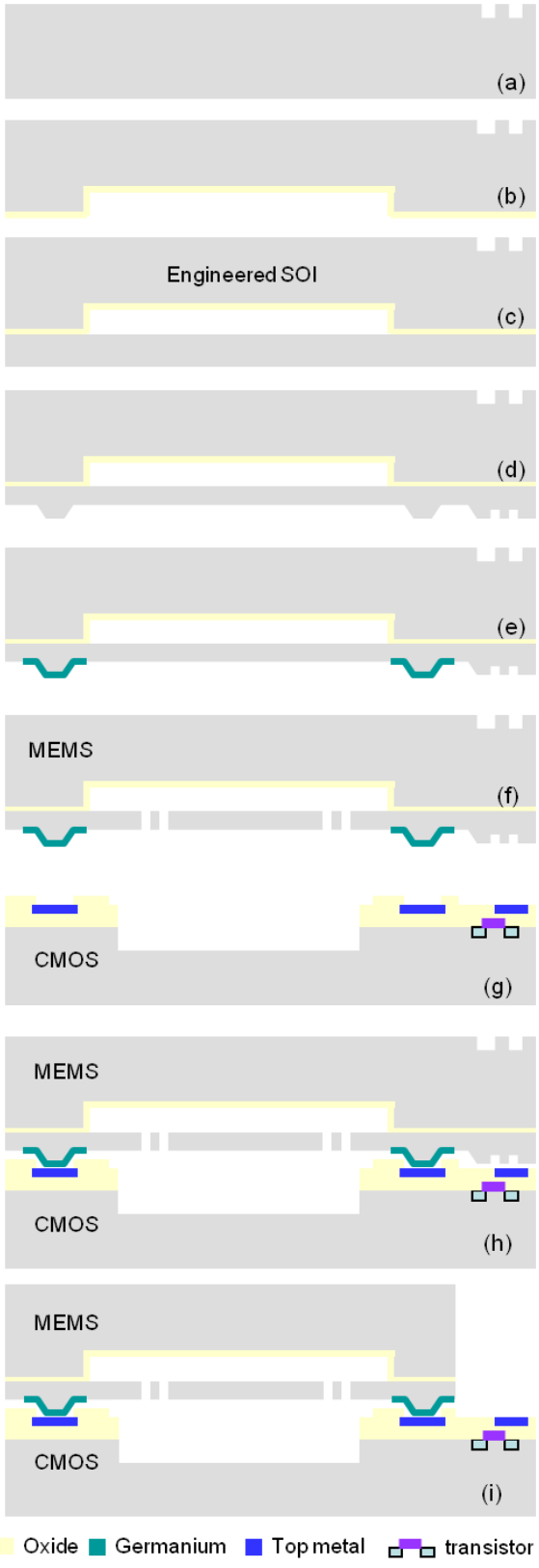

Figure 5. Nasiri-Fabrication process flow.

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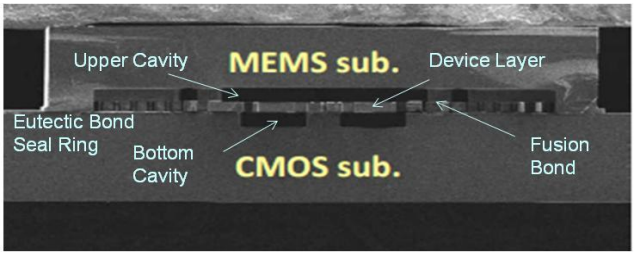

Figure 6. Cross-section of a finished integrated device.

4.2 Wafer-level Sealing

Since the MEMS structures are hermetically sealed, and therefore protected, with contact pads exposed (Figure 7), the wafer may be treated as a normal CMOS wafer, without the need for special handling during further processing (e.g. dicing or grinding). This aspect is very attractive to high volume foundries which are often not outfitted with specialized MEMS equipment such as stealth or laser dicers, and allows them to use their standard high throughput equipment and processes.

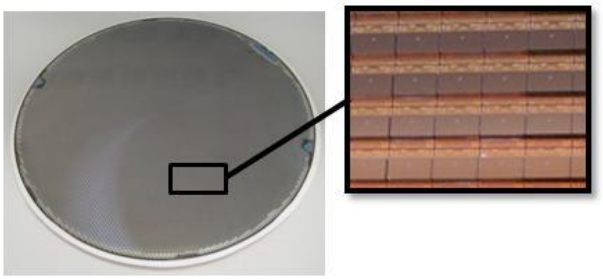
Figure 7. Completed 8" CMOS-MEMS wafer. The inset shows a close-up of the die with exposed wire-bond pads.

Furthermore, the wafers can be fully tested using standard high throughput wafer probers (Figure 8, Figure 9), significantly reducing packaging cost, simplifying yield enhancement, and improving reliability by packaging only known good die.

4.3 MEMS to CMOS Integration

Direct MEMS to CMOS electrical interconnect provides a very low parasitic signal coupling and shielding capability. The CMOS multi-layer metal stack also replaces traditional MEMS routing approach limited by single un-shielded high-resistance silicon layer. Moreover, the close integration with CMOS electronics allows electronic trimming and compensation for any MEMS process variations, thereby relaxing manufacturing tolerances and increasing yield and manufacturability.

4.4 CMOS Compatibility

The entire NF process is CMOS compatible and is sufficiently simple for CMOS manufacturers to embrace the additional MEMS steps. For this reason, it is very attractive to Tier 1 CMOS foundries as a straightforward way to leverage their existing infrastructure and provide a value add to their existing CMOS production. The same benefits that these foundries provide to their CMOS users – great process control and yield, high volume capability, excellent delivery reliability – are also realized by the fabless MEMS customers.

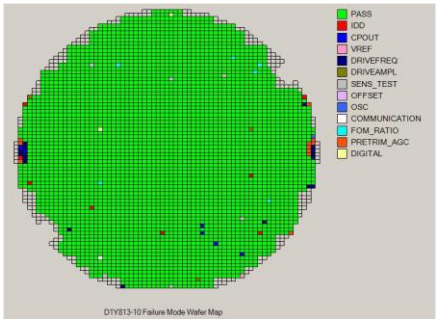

Figure 8. Wafer level probe results showing excellent yield.

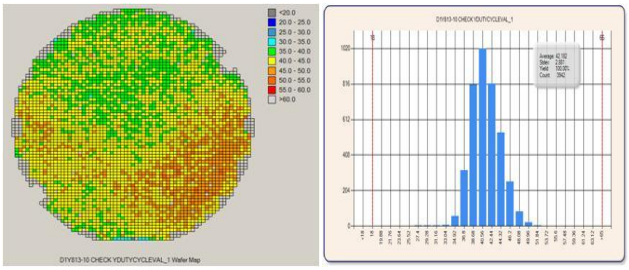
Figure 9. 8" wafer level device vacuum distribution.

4.5 Expandability

As described, the NF platform is based on electrostatic transduction and single crystal silicon. This foundation can support a wide range of devices, including inertial sensors, pressure sensors, and resonators, and other similar systems. However, with simple enhancements, the platform can support a myriad of additional MEMS devices from micro-fluidics to magnetics to acoustics. In fact, a MEMS wafer of almost any technology (bulk, surface, LIGA, containing active bio or chemical sensor layers, etc.), with the addition of Ge deposition, can be integrated to CMOS using the NF platform.

5 SUMMARY

As MEMS continues to play a larger part in the high technology market, it must adapt to requirements for higher volume, better reliability, higher integration, and lower cost, while at the same time lowering the barrier to entry for new and innovative products. The NF fabrication platform is ideally suited to meet those needs for fabless MEMS companies by providing a versatile MEMS technology intimately integrated with standard CMOS and fully compatible with high volume manufacturing, test, and packaging processes.