Modeling of Trench-Gate Type HV-MOSFETs for Circuit Simulation

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ABSTRACT

A wide range of application has made high-voltage (HV) MOSFETs evolve into application-specific structures. Trench-gate type HV-MOSFET is one of them; its user application space tends to fall on a larger power consumption domain, compared with planar HV-MOSFET. As for planar HV-MOSFETs, regardless of DDMOS or LDMOS, HiSIM_HV has begun to serve design community as a world recognized model. In this work, the benefit of HiSIM_HV would be extended to another class of HV device, i.e., trench-gate type HV-MOSFET, while the framework of the HiSIM_HV model formulation is kept intact as much as possible. The modified code successfully can play back TCAD-generated measurement data.

Keywords: high-voltage MOSFET, LDMOS, HiSIM, trench-gate MOSFET

1 INTRODUCTION

High-Voltage (HV) MOSFET is utilized for a wide range of purpose. Due to the wide spectrum of its usages, its structural varieties abound. LDMOS, with its high-resistive drift region at the drain side only, usually covers a lower voltage domain. In contrast, a symmetrical structure, with the drift region both at the source and the drain, covers a higher voltage domain. The HV-MOSFET evolves to another structures, seeking for its usability beyond a few hundred volt realm. The trench-gate structure has been one of them. The notable advantage of trench-gate MOSFET is its lower on-resistance, which contributes to a high performance in switching in the high-voltage applications.

To make the most of it, in circuit designing, an accurate compact model is required. A usual approach for modeling such devices has been macro modeling with sub-circuit descriptions. However, it would deteriorate convergence in circuit simulation, and would make parameter extraction less physically sound than a compact model.

We have so far developed HiSIM_HV [1, 2, 3], a compact model for high-voltage MOSFETs, which is based on surface potential descriptions, valid both for LDMOS and HV-MOSFET. The model is built on top of HiSIM2, a compact model for bulk-, planar MOSFETs. The main focus is the development of the model for the drift region which is usually highly resistive and therefore sustains substantial portion of the applied high voltage. In this work, developed is a compact model for the trench-gate MOSFET, within a framework of HiSIM_HV.

2 MODELING APPROACH

2.1 Feature of Trench-Gate Structure

Two-dimensional device simulation was used for analyzing device operation on the device structures exemplified in Fig. 1. Since the structure is symmetrical, a half of it suffices. Device parameters are described in Table 1. The output characteristics are shown in Fig. 2 for three different trench widths \( W_{\text{tre}} \). For comparison and as reference, the result of a fictitious LDMOS structure with \( W_{\text{tre}}=0 \) is also shown together. The simulation results clearly show that the drain current \( I_{\text{ds}} \) increases as \( W_{\text{tre}} \) increases. The increase of \( I_{\text{ds}} \) becomes more obvious as the gate voltage \( V_{\text{gs}} \) increases.

![Figure 1: A schematic representation of the studied trench-type LDMOS; (a) the whole structure and (b) the left-half of the structure used for 2D-device simulation.](image)

<table>
<thead>
<tr>
<th>Table 1: Device Structure</th>
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<tbody>
<tr>
<td>Channel length ( L_{\text{ch}} )</td>
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<tr>
<td>Overlap length ( L_{\text{over}} )</td>
</tr>
<tr>
<td>Oxide thickness</td>
</tr>
<tr>
<td>Impurity concentration (channel)</td>
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<tr>
<td>Impurity concentration (drift region)</td>
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Figure 3 shows an internal current flow for the three different \( V_{\text{gs}} \). Noteworthy is that the current flow tends to stay away from the bottom of the trench-gate edge for lower \( V_{\text{gs}} \) values. Also noteworthy is that, for larger \( V_{\text{gs}} \) values, the current flow tends to spread to the bottom of the trench-gate edge, gradually filling an otherwise depleted region. In the upper row of Fig. 3, shown is the current density profile along the designated locations. It is seen that the current density underneath the trench is not negligible for the \( V_{\text{gs}}=6 \)V case. This suggests that the origin of the increased current is attributed to the additional current path underneath the trench bottom.
2.2 General HV-MOSFET Modeling

One of notable features in HV-MOSFET characteristics is the quasi saturation of the output characteristics; diminished saturation features as well as the strong channel conductance peaks. The origin of these features is the resistive drift region inducing the potential drop within the drift region. This resistance effect is modeled by a resistor in HiSIM_HV2 as schematically shown in Fig. 4 [2]. The magnitude of the resistance is modeled as

$$R_{\text{drift}} = \frac{V_{\text{dp}}}{I_{\text{ddp}}}$$

where $V_{\text{dp}}$ between $V_{\text{DS}}$ and $V_{\text{DP}}$ is the potential drop and $I_{\text{ddp}}$ is the current flow within the drift region, which is written as

$$I_{\text{ddp}} = W_{\text{eff}} \cdot X_{\text{ox}} \cdot q \cdot N_{\text{drift}} \cdot \mu_{\text{drift}} \cdot \frac{V_{\text{ddp}}}{L_{\text{drift}} + R_{\text{DRL1}}}$$

where $W_{\text{eff}}$, $N_{\text{drift}}$, $\mu_{\text{drift}}$, $L_{\text{drift}}$ are the effective channel width, the impurity concentration in the drift region, the mobility in the drift region and the length of the drift region, respectively. RDRDL1 is an offset parameter for the length of the drift region. The internal node potential $V_{\text{DP}}$ designated in Fig. 4 is solved iteratively during circuit simulation to preserve the current continuity between the channel and the resistor region.

Calculation results from the present HiSIM_HV2 are compared with 2D-device simulation results in Fig. 5(a). For larger $V_{\text{gs}}$, the model fails to capture the specific feature of the trench-gate structure, namely the enhancement of drain current.

2.3 Model Development for Trench-Gate MOSFET

As can be seen in Fig. 3, the key development required for the trench-gate structure is the modeling of the current flow dependence on $V_{\text{gs}}$. For the purpose we consider two resistances connected in a series as shown in Fig. 6. Thus the model equation is rewritten as:
\[
I_{\text{dep}} = \frac{V_{\text{dep}}}{R_{\text{th}} + R_1 + R_2}
\]

where

\[
R_1 = \rho \frac{L}{S} = \rho \frac{W_{\text{tre}}}{W_{\text{eff}} \cdot X_{\text{ov}}}
\]

\[
R_2 = \rho \frac{L}{S} = \rho \frac{I_{\text{drift}} - W_{\text{tre}}}{W_{\text{eff}} \cdot X_{\text{ov}} + W_{\text{tre}}}
\]

The cross section area and the length of the resistor are denoted by \( S \) and \( L \), and \( \rho \) is the resistivity of the drift region. The aperture size of the current flow in the R1 region is denoted by \( X_{\text{ov}} \), and the length of this path is identified with the depletion width denoted as \( W_{\text{tre}} \). In the R2 region, the current flow widens to an effective width, which is the sum of \( X_{\text{ov}} \) and \( W_{\text{tre}} \). The device width is denoted by \( W_{\text{eff}} \).

\[
X_{\text{ov}} = W_0 - A \cdot \left( \frac{W_0}{D_{\text{junc}}} \cdot \frac{W_{\text{dep}}}{L_{\text{over}}} \right)
\]

where

\[
W_0 = \sqrt{\frac{L_{\text{over}}^2 + D_{\text{junc}}^2}{2}}
\]

\[
W_{\text{dep}} = \sqrt{\frac{2e_{\text{si}} \phi_{\text{si}} + V_{\text{dps}} - V_{\text{hs}}}{q \cdot N_{\text{over}}}}
\]

\[
W_{\text{junc}} = \sqrt{\frac{2e_{\text{ai}} \phi_{\text{ai}} - V_{\text{dps}} - V_{\text{bs}}}{q \cdot N_{\text{drift}}} \cdot \frac{N_{\text{sub}}}{N_{\text{sub}} + N_{\text{drift}}}}
\]

The depletion width \( W_{\text{tre}} \) underneath the trench is dependent on \( V_{\text{gs}} \) and is written as function of the charge stored at the bottom of the trench. This charge is identified with the overlap charge and is calculated by solving the Poisson’s equation within the overlap region. In HiSIM_HV, the overlap charge is treated as the sum of two contributions; one at the internal node and the other at the external node. The ratio of these two is adjustable through a model parameter \( B \). With the use of the overlap charge, the depletion width \( W_{\text{dep}} \) can be written as

\[
W_{\text{d,tre}} = \frac{Q_{\text{tre}}}{q \cdot N_{\text{drift}}}
\]

\[
Q_{\text{tre}} = B \cdot Q_{\text{over,int}} V_{\text{dps}} V_{\text{gs}} + 1 - B \cdot Q_{\text{over,ext}} V_{\text{dps}} V_{\text{gs}}
\]

The calculated \( W_{\text{d,tre}} \) is compared with that from 2D-device simulation results, in Fig. 8.

**CALCULATION RESULTS**

The developed model is implemented into HiSIM_HV2, and SPICE simulations are performed for verification. Figure 5(b) shows the comparison. Observed good
agreement supports that the widening of the current-path aperture size is the origin of the trench-gate feature. As shown in Fig. 9, for three different trench widths, \( W_{\text{tre}} \), verified was the predictability of the developed model. For the calculation, only \( W_{\text{tre}} \) was varied according to the given values. By increasing \( W_{\text{tre}} \), the reduction of the resistance occurs (see Eq. 3) and the current increases as a result.

**Figure 9:** Calculated output characteristics with the developed model for various \( W_{\text{tre}} \) lengths compared with 2D-device simulation results.

**Figure 10:** Calculated output characteristics with the further improved model, in contrast to Fig. 9(c).

### 4 DISCUSSIONS

As shown in Fig. 9, the accuracy of the developed model tends to be compromised as \( W_{\text{tre}} \) increases, though it is still better than shown in Fig. 5(a). This increase of current density can be modeled as the increase of the effective carrier density, as is treated in [2]. In HiSIM_HV, the carrier density is set equal to the impurity concentration in the drift region, in the first place. As the drain voltage \( V_{\text{ds}} \) increases, however, the effective carrier density increases to compensate the mobility reduction due to the presence of high-electric field. On this occasion, which is similar to the high injection of carriers, \( N_{\text{drift}} \) in the various equations presented so far, such as Eqn. 10, shall be read as \( N_{\text{drift, eff}} \) to accommodate the high-injection effects. \( N_{\text{drift, eff}} \) is defined as follows:

\[
N_{\text{drift, eff}} = N_{\text{drift}} \left( 1 + RDRCAR \cdot E \right) \left( 1 - \frac{\mu}{\mu_0} \right) \tag{12}
\]

where

\[
E = \frac{V_{\text{ddp}}}{I_{\text{drift}}} \tag{13}
\]

\[
\mu = \frac{\mu_0 \cdot E}{1 + \frac{V_{\text{ds}}}{V_{\text{max}}}} \tag{14}
\]

where \( \mu_0 \) is the low-field mobility, while \( \mu \) is the electric-field dependent mobility with the saturation velocity \( V_{\text{max}} \). RDRRCAR is a model parameter that can be specific to each \( W_{\text{tre}} \), modulating carrier concentration in the drift region.

This treatment leads to a decrease of \( W_{d,\text{tre}} \), leading to the increase of current, effective particularly at higher \( V_{\text{gs}} \). Consequently, accuracy has improved as can be seen in Fig. 10, in contrast to Fig. 9(c).

### REFERENCES

