Modeling of Trench-Gate Type HV-MOSFETs for Circuit Simulation

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ABSTRACT

A wide range of application has made high-voltage (HV) MOSFETs evolve into application-specific structures. Trench-gate type HV-MOSFET is one of them; its user application space tends to fall on a larger power consumption domain, compared with planar HV-MOSFET. As for planar HV-MOSFETs, regardless of DDMOS or LDMOS, HiSIM_HV has begun to serve design community as a world recognized model. In this work, the benefit of HiSIM_HV would be extended to another class of HV device, i.e., trench-gate type HV-MOSFET, while the framework of the HiSIM_HV model formulation is kept intact as much as possible. The modified code successfully can play back TCAD-generated measurement data.

Keywords: high-voltage MOSFET, LDMOS, HiSIM, trench-gate MOSFET

1 INTRODUCTION

High-Voltage (HV) MOSFET is utilized for a wide range of purpose. Due to the wide spectrum of its usages, its structural varieties abound. LDMOS, with its high-resistive drift region at the drain side only, usually covers a lower voltage domain. In contrast, a symmetrical structure, with the drift region both at the source and the drain, covers a higher voltage domain. The HV-MOSFET evolves to another structures, seeking for its usability beyond a few hundred volt realm. The trench-gate structure has been one of them. The notable advantage of trench-gate MOSFET is its lower on-resistance, which contributes to a high performance in swtiching in the high-voltage applications.

To make the most of it, in circuit designing, an accurate compact model is required. A usual approach for modeling such devices has been macro modeling with sub-circuit descriptions. However, it would deteriorate convergence in circuit simulation, and would make parameter extraction less physically sound than a compact model.

We have so far developed HiSIM_HV [1, 2, 3], a compact model for high-voltage MOSFETs, which is based on surface potential descripions, valid both for LDMOS and HV-MOSFET. The model is built on top of HiSIM2, a compact model for bulk-, planar MOSFETs. The main focus is the development of the model for the drift region which is usually highly resistive and therefore sustains substantial portion of the applied high voltage. In this work, developed is a compact model for the trench-gate MOSFET, within a framework of HiSIM_HV.

2 MODELING APPROACH

2.1 Feature of Trench-Gate Structure

Two-dimensional device simulation was used for analyzing device operation on the device structures exemplified in Fig. 1. Since the structure is symmetrical, a half of it suffices. Device parameters are described in Table 1. The output characteristics are shown in Fig. 2 for three different trench widths W_{tre}. For comparison and as reference, the result of a fictitious LDMOS structure with W_{tre}=0 is also shown together. The simulation results clearly show that the drain current I_{ds} increases as W_{tre} increases. The increase of I_{ds} becomes more obvious as the gate voltage V_{gs} increases.

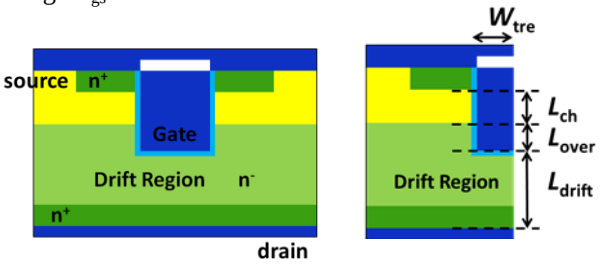

Figure 1: A schematic representation of the studied trench-type LDMOS; (a) the whole structure and (b) the left-half of the structure used for 2D-device simulation.

Table 1: Device Structure

Channel length L_{ch}	0.8 μm
Overlap length L_{over}	0.7 μm
Oxide thickness	30 nm
Impurity concentration (channel)	1× cm^{-3}
Impurity concentration (drift region)	1× cm^{-3}

Figure 3 shows an internal current flow for the three different V_{gs}. Noteworthy is that the current flow tends to stay away from the bottom of the trench-gate edge for lower V_{gs} values. Also noteworthy is that, for larger V_{gs} values, the current flow tends to spread to the bottom of the trench-gate edge, gradually filling an otherwise depleted region. In the upper row of Fig. 3, shown is the current density profile along the designated locations. It is seen that the current density underneath the trench is not negligible for the V_{gs} =6V case. This suggests that the origin of the increased current is attributed to the additional current path underneath the trench bottom.

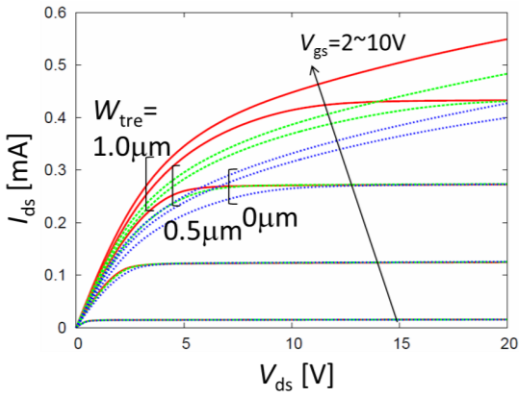

Figure 2: Simulated output characteristics. The trench width W_{tre} is 1.0μm, 0.5μm, and zero, namely without the trench structure, respectively.

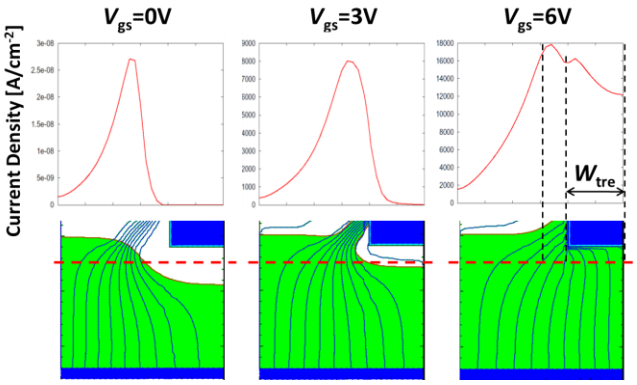

Figure 3: Current flow in the drift region (lower row). Along the locations designated by the dashed, horizontal cut-out line, current density is plotted (upper row). The trench width W_{tre} is 1.0μm. The drain voltage V_{ds} is 5V.

2.2 General HV-MOSFET Modeling

One of notable features in HV-MOSFET characteristics is the quasi saturation of the output characteristics; diminished saturation features as well as the strong channel conductance peaks. The origin of these features is the resistive drift region inducing the potential drop within the drift region. This resistance effect is modeled by a resistor in HiSIM_HV2 as schematically shown in Fig. 4 [2]. The magnitude of the resistance is modeled as

$$R_{\mathrm{drift}} = \frac{V_{\mathrm{ddp}}}{I_{\mathrm{ddp}}} \tag{1}$$

where V_{ddp} between V_{DS} and V_{DP} is the potential drop and I_{ddp} is the current flow within the drift region, which is written as

$$I_{\mathrm{ddp}} = W_{\mathrm{eff}} \cdot X_{\mathrm{ov}} \cdot q \cdot N_{\mathrm{drift}} \cdot \mu_{\mathrm{drift}} \frac{V_{\mathrm{ddp}}}{L_{\mathrm{drift}} + \mathrm{RDRDL1}} \tag{2}$$

where W_{eff}, N_{drift}, μ_{drift}, L_{drift} are the effective channel width, the impurity concentration in the drift region, the mobility in the drift region and the length of the drift region,respectively. RDRDL1 is an offset paramter for the length of the drift region. The internal node potential V_{DP} designated in Fig. 4 is solved iteratively during circuit simulation to preserve the current continuity between the channel and the resistor region.

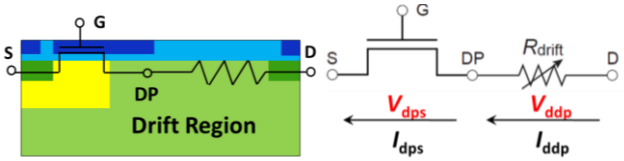

Figure 4: The scheme of modeling an LDMOS structure. The potential drop across the drift region is solved itera-tively. DP is the internal node.

Calculation results from the present HiSIM_HV2 are compared with 2D-device simulation results in Fig. 5(a). For larger V_{gs}, the model fails to capture the specific feature of the trench-gate structure, namely the enhancement of drain current.

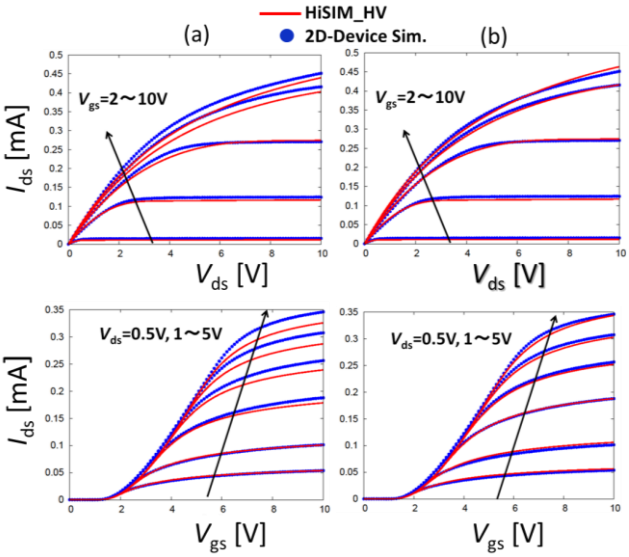

Figure 5: Calculated I-V characteristics with the present HiSIM_HV 2.0.0 vs TCAD simulation results; (a) with the conventional HiSIM_HV2.0.0, (b) with the modified HiSIM_HV2.0.0 to be described afterwards.

2.3 Model Development for Trench-Gate MOSFET

As can be seen in Fig. 3, the key development required for the trench-gate structure is the modeling of the current flow dependence on Vgs. For the purpose we consider two resistances connected in a series as shown in Fig. 6. Thus the model equation is rewritten as:

$$I_{\mathrm{ddp}} = \frac{V_{\mathrm{ddp}}}{R_{\mathrm{dift}}} = \frac{V_{\mathrm{ddp}}}{R_1 + R_2} \tag{3}$$

where

$$R_1 = \rho \frac{L}{S} = \rho \frac{W_{\mathrm{d\_tre}}}{W_{\mathrm{eff}} \cdot X_{\mathrm{ov}}} \tag{4}$$

$$R_2 = \rho \frac{L}{S} = \rho \frac{L_{\mathrm{drift}} - W_{\mathrm{d\_tre}}}{W_{\mathrm{eff}} \quad X_{\mathrm{ov}} + W_{\mathrm{tre}}} \tag{5}$$

The cross section area and the length of the resistor are denoted by S and L, and ρ is the resistivity of the drift region. The aperture size of the current flow in the R1 region is denoted by X_{ov}, and the length of this path is identified with the depletion width denoted as $W_{\mathrm{d\_tre}}$. In the R2 region, the current flow widens to an effective width, which is the sum of X_{ov} and W_{tre}. The device width is denoted by W_{eff}.

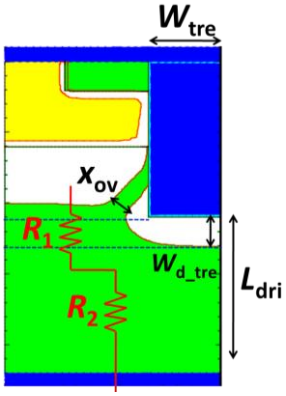

Figure 6: Concept of the developed model for the trench-type LDMOS structure.

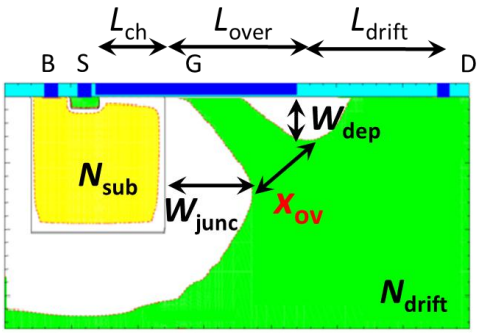

Figure 7: Schematic of the current flow underneath the overlap region The aperture size of the current flow, X_{ov}, is determined by the depletion lengths W_0 and W_{junc} [2].

The aperture size of the current flow, X_{ov}, has been modeled in the present HiSIM_HV2 as a 2D effect, determined by two depletion widths W_{dep} and W_{junc} as schematically shown in Fig. 7:

$$X_{\mathrm{ov}} = W_0 - A \cdot \left(\frac{W_0}{D_{junc}} W_{\mathrm{dep}} - \frac{W_0}{L_{\mathrm{over}}} W_{junc} \right) \tag{6}$$

where

$$W_0 = \sqrt{{L_{\mathrm{over}}}^2 + {D_{junc}}^2} \tag{7}$$

$$W_{\mathrm{dep}} = \sqrt{\frac{2\varepsilon_{\mathrm{si}} \; V_{\mathrm{dps}} - \phi_{\mathrm{s\_over}}}{q \cdot N_{\mathrm{over}}}} \tag{8}$$

$$W_{\mathrm{junc}} = \sqrt{\frac{2\varepsilon_{\mathrm{si}} \; \phi_{\mathrm{bi}} + V_{\mathrm{dps}} - V_{\mathrm{bs}}}{q}} \cdot \frac{N_{\mathrm{sub}}}{N_{\mathrm{drift}} \quad N_{\mathrm{sub}} + N_{\mathrm{drift}}} \tag{9}$$

The depletion width W_{d_tre} underneath the trench is dependent on V_{gs} and is written as function of the charge stored at the bottom of the trench. This charge is identified with the overlap charge and is calculated by solving the Poisson's equation within the overlap region. In HiSIM_HV, the overlap charge is treated as the sum of two contributions; one at the internal node and the other at the external node. The ratio of these two is adjusable through a model parameter B. With the use of the overlap charge, the depletion width W_{dep} can be written as

$$W_{\mathrm{d\_tre}} = \frac{Q_{\mathrm{tre}}}{q \cdot N_{\mathrm{drift}}} \tag{10}$$

$$Q_{tre} = B \cdot Q_{\mathrm{over\_int}} \; V_{\mathrm{dps}}, V_{\mathrm{gs}} \; + \; 1 - B \; \cdot Q_{\mathrm{over\_ext}} \; V_{\mathrm{ds}}, V_{\mathrm{gs}} \tag{11}$$

The calculated $W_{\mathrm{d\_tre}}$ is compared with that from 2D-device simulation results, in Fig. 8.

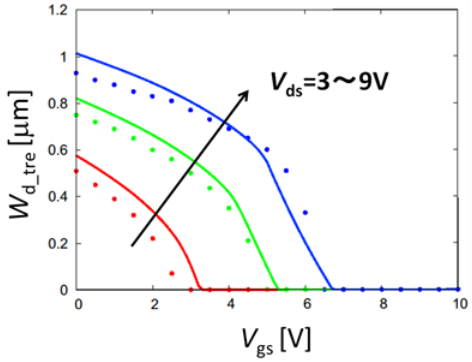

Figure 8: The depletion width underneath the trench $W_{\mathrm{d\_tre}}$, calculated through the developed model (lines) and through 2D-device simulation (dots) for comparison.

3 CALCULATION RESULTS

The developed model is implemented into HiSIM_HV2, and SPICE simulations are performed for verification. Figure 5(b) shows the comparison. Observed good

agreement supports that the widening of the current-path aperture size is the origin of the trench-gate feature. As shown in Fig. 9, for three different trench widths, W_{tre}, verified was the predictability of the developed model. For the calculation, only W_{tre} was varied according to the given values. By increasing W_{tre}, the reduction of the resistance occurs (see Eq. 3) and the current increases as a result.

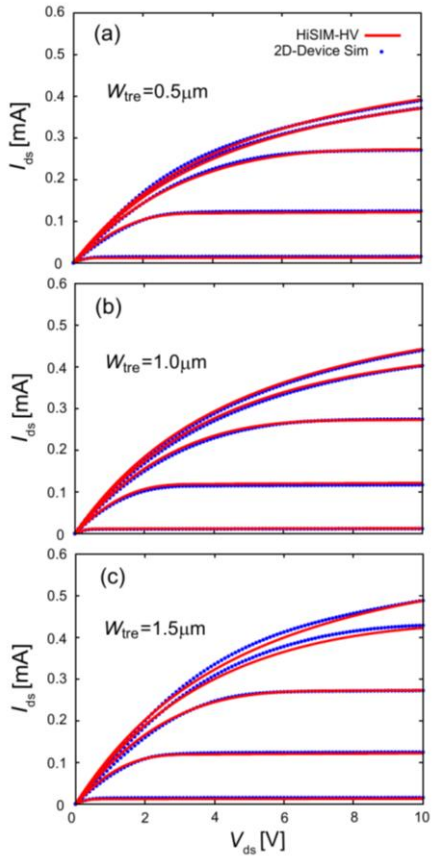

Figure 9: Calculated output characteristics with the developed model for various W_{tre} lengths compared with 2D-device simulation results.

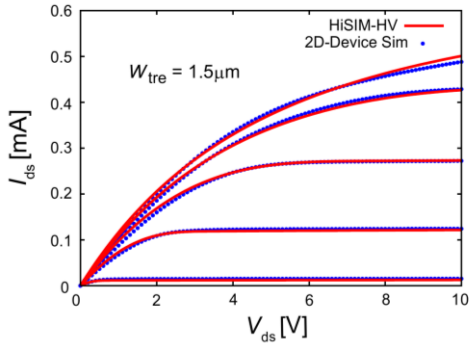

Figure 10: Calculated output characteristics with the further improved model, in contrast to Fig. 9(c).

4 DISCUSSIONS

As shown in Fig. 9, the accuracy of the developed model tends to be compromised as W_{tre} increases, though it is still better than shown in Fig. 5(a). This increase of current density can be modeled as the increase of the effective carrier density, as is treated in [2]. In HiSIM_HV, the carrier density is set equal to the impurity concentration in the drift region, in the first place. As the drain voltage V_{ds} increases, however, the effective carrier density increases to compensate the mobility reduction due to the presence of high-electric field. On this occasion, which is similar to the high injection of carriers, N_{drift} in the various equations presented so far, such as Eqn. 10, shall be read as $N_{drift,\,eff}$ to accommodate the high-injetion effects. $N_{drift,\,eff}$ is defined as follows:

$$N_{\mathrm{drift,eff}} = N_{\mathrm{drift}} \left\{ 1 + RDRCAR \cdot E \left(1 - \frac{\mu}{\mu_0} \right) \right\} \qquad (12)$$

where

$$E = \frac{V_{\mathrm{ddp}}}{L_{\mathrm{drift}}} \qquad (13)$$

$$\mu = \frac{\mu_0}{1 + \dfrac{\mu_0 \cdot E}{V_{\max}}} \qquad (14)$$

where μ_0 is the low-field mobility, while μ is the electric-field dependent mobility with the saturation velocity V_{max}. RDRCAR is a model parameter that can be specific to each W_{tre}, modulating carrier concentration in the drift region.

This treatment leads to a decrease of W_{d_tre}, leading to the increase of current, effective particularly at higher V_{gs}. Consequently, accuracy has improved as can be seen in Fig. 10, in contrast to Fig. 9(c).

REFERENCES

[1] Y. Oritsuki, M. Yokomichi, T. Kajiwara, A. Tanaka, N. Sadachika, M. Miyake, H. Kikuchihara, K. Johguchi, U. Feldmann, H. J. Mattausch, M. Miura-Mattausch, "HiSIM-HV: A Compact Model for Simulation of High-Voltage MOSFET Circuits," IEEE Trans. Electron Devices, vol. 57, no. 10, pp. 2671-2678, 2010.

[2] A. Tanaka, Y. Oritsuki, H. Kikuchihara, M. Miyake, H. J. Mattausch, M. Miura-Mattausch, Y. Liu, and K. Green, "Quasi-2-Dimensional Compact Resistor Model for the Drift Region in High-Voltage LDMOS Devices," IEEE Trans. Electron Devices, vol. 58, no. 7, pp. 2072-2080, 2011.

[3] HiSIM_HV 2.0.0 User's Manual, Hiroshima University and STARC, 2011.