High-Voltage High Input Impedance Unity-Gain Voltage Buffer

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ABSTRACT

The paper presents a novel structure of a voltage buffer intended for application in high-voltage integrated systems. The presented solution is based on both source-input and gate-input voltage buffer, so as to get the best of both structures. The resulting circuitry offers high impedance input node without any DC-path, and voltage gain close to unity. Simulation results of the proposed circuit designed in 0.8 µm HV SoI technology.

Keywords: high-voltage circuits, unity gain voltage buffers, Silicon-on-Insulator process, high input impedance.

1 INTRODUCTION

High-voltage semiconductor processes enable design and production of integrated circuits that offer extended functionality over their low-voltage counterparts. Still, many MOS devices present in high-voltage semiconductor processes tolerate drain-source and drain-gate voltages up to tens of volts, but only low-range (up to a few volts) gate-source voltages. Also, high-voltage MOS devices, due to their structure, provide poor matching, which may reduce quality of high-voltage integrated system operation. Thus, some low-voltage-originating topologies cannot be directly put into high-voltage applications and expected to function as well as their low-voltage counterparts.

The research presented in this paper is targeted to develop possibly simple high-voltage unity-gain buffer that has high input impedance and is able to work in high-voltage systems. The circuit idea originated from the need of buffering a current-mode waveform generator, presented in [1]. Necessity of proper decoupling of current-mode outputs from inputs of following voltage-mode stages is a general rule, as can be seen in [2]. In low-voltage applications voltage buffer that offers very high input impedance can be implemented as an operational amplifier or any others structures [2]. On the other hand, design process of high-voltage versions of circuits like OPAMPs can be a demanding task and other solutions could be more convenient.

2 SIMPLE STRUCTURES

Structures well-suited for acting as high-voltage unity-gain buffers are complementary voltage followers. Two main types of such circuits may be distinguished [3], as basic buffer structures applicable also for high-voltage applications. Source-input followers, like in Figure 1.a, offer higher precision of voltage gain, but have limited input impedance. Input impedance is limited by presence of a DC current-path through the buffer input node. Such current path may easily render current-mode circuits useless, if they are loaded with such buffers.

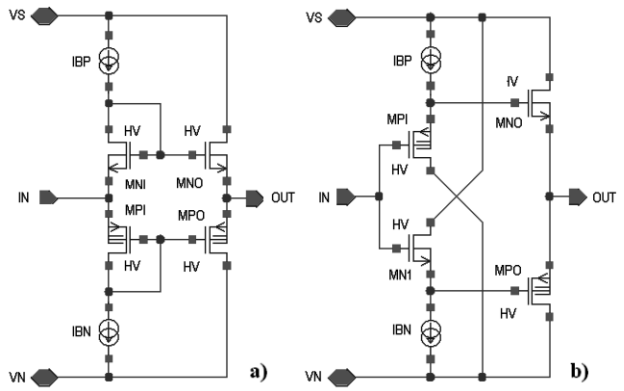

Figure 1: Simple source input (a) and gate-input (b) buffers, applicable to both low-voltage and high-voltage systems.

Gate-input follower, like in Figure 1.b, seems to provide a solution to the input impedance problem. But again, its drawback is imprecise voltage gain value, due to input stage structure of gate-input followers. This structure does not provide any methods of precise aligning output voltage with input voltage. Typical gate-input voltage buffer presented in Figure 1.b shows that its input stage is made of an MOS transistor with its gate connected to the buffer input. This transistor is biased with a current source connected to its source.

Relevant output stage consists of a complementary type MOS transistor with its gate driven by source of the input MOS transistor. Source terminal of the output transistor is connected to the buffer output. Because the input and the output stage MOS transistors are of opposite conduction types, there is only a rough way of aligning input and output voltage levels.

Limitations of the gate-input voltage buffers are aggravated by the fact, that when a drain-source voltage of the input MOS transistor rises, a drain-source voltage of the relevant output MOS transistor falls. This effect makes the input and output transistor to adjust their gate-source voltage in the opposite ways. This in turn adds to a difference between input and output voltage. As a result, the expected unity gain gets reduced in comparison to gain offered by source-input buffers.

3 PROPOSED STRUCTURE

There are attempts to build voltage buffers that use gate-input structures, but offer control over gain value and DC voltage offset [4]. Some solutions use complex adaptive biasing structures for precise control of proposed buffer structures [5]. Unfortunately, most of the structures are designed for low-voltage applications [4], [5].

In this paper a high-voltage buffer solutions are considered and high-voltage device properties are taken into account. Few high-voltage unity gain buffer solution have been proposed and due to their specific application demands, they tend to be quite complex [6]. Possibly effective buffer structure with limited number of transistors and possibly short signal flow-path is investigated in this paper.

The proposed structure is elaborated in order to keep high impedance input of the gate-input voltage buffer and gain value similar to this of a source-input voltage buffer. This goal is achieved by adjusting gate-source voltage drops of the input stage transistor possibly close to the output stage transistor gate-source voltage drops. Or in other words, to make the input stage transistors of the gate-input buffer provide gate-source voltages possibly similar to gate-source voltages in the input stage of the source-input voltage buffer. To achieve proper voltage drop on the input stage transistors, it is required to get these transistors properly polarized. This is made with modification of the input stage bias current sources.

The idea is to provide bias current that produces input transistor gate-source voltage drop equal to that of present at input-stage transistors of source-input voltage buffer. Concept of the idea is presented in Figure 2. There are two current sources, and their currents are equal to input bias currents of the source-input voltage buffer. Each of these currents biases one of reference transistors (MNR, MPR), identical to one of input-stage transistors of the source-input buffer.

These reference transistors are applied in diode connection, just like the input transistors in the source-input buffer. The bias currents produce gate-source voltage drops at these two reference transistors that in turn drive two auxiliary transistors (MNA, MPA), identical to those used in input of the proposed structure. These two auxiliary transistors convert gate-source voltage drops into currents used for input-stage biasing. Next, the input-stage transistors convert devised bias currents into their gate-source voltage drops, expected to be identical to voltage drops at the reference transistors.

Though promising, the solution presented in Figure 2, has several drawbacks that severely limit its application. First, the circuit requires proper matching of several pairs of transistors for proper operation. All these transistors are high-voltage devices, which makes matching difficult. Other issue is a fact, that auxiliary and input transistors, which are expected to work as a voltage-current-voltage chain of signal transmission, change their drain-source voltages in opposite ways.

Increase of the drain-source voltage of the auxiliary transistor causes decrease of drain-source voltage of the relevant input-stage transistor. If drain-source voltage of the auxiliary transistor drops, the bias current, which it produces also drops. Such reduced current flows through the relevant input transistor, causing its gate-voltage to be reduced. Furthermore, while drain-source voltage of the auxiliary transistor drops, drain-source voltage of the identical input-stage transistor rises.

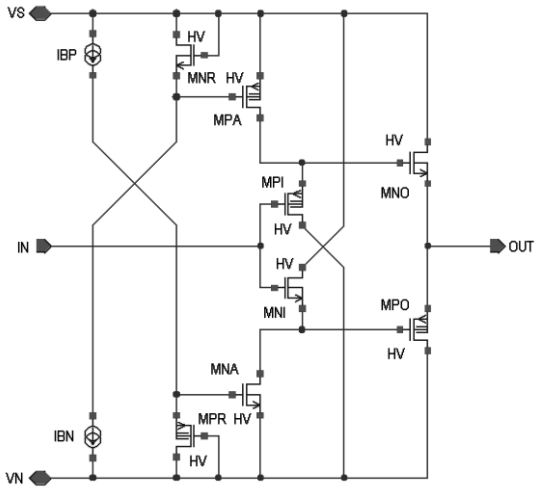

Figure 2: Introductory version of the proposed buffer.

The input-stage transistor is biased with externally provided current and is required to stay in saturation. The only way it can cope with rise of its drain-source voltage, is a slight reduction of its gate-source voltage, so as to keep its drain-source current constant. Thus, there are two causes of gate-source voltage reduction in input-stage transistor, as compared to relevant auxiliary transistor. In complementary pair of the auxiliary and input-stage transistors the process goes in the opposite way. As a result the voltage gain of the proposed buffer gets reduced.

An amendment that solves the presented problems is possible. The basic idea is an application of low-voltage transistors in critical points of the buffer, and using high-voltage transistors as both safety and cascode-like devices. The modified structure is presented in Figure 3. Again, there are two bias current sources. Now, each of the currents polarizes a set of two complementary reference transistors that mimic input-stage of the source-input buffer. Each of these reference transistor pairs drives one auxiliary low-voltage transistor, additionally equipped with one of auxiliary high-voltage cascode transistors (MNAC, MPAC). These high-voltage transistors are driven with help of the previously absent reference transistors (MNRR, MPRR), now added to form an imitation of a complete input-stage of the source-input buffer.

Total voltage drop on each of the reference transistor pair (MNR + MPRR and MPR + MNRR) is made to be

equal to the total voltage drop between source terminals of the input-stage transistors (and thus between gate terminals of the output stage transistors). According to this, it is possible to replace each of high-voltage input-stage transistors with a set of low-voltage input transistors (MNA or MNA) and cascode high-voltage transistors (MNAC or MPAC) - both identical to transistors driven with imitations of source-input type buffer input stages.

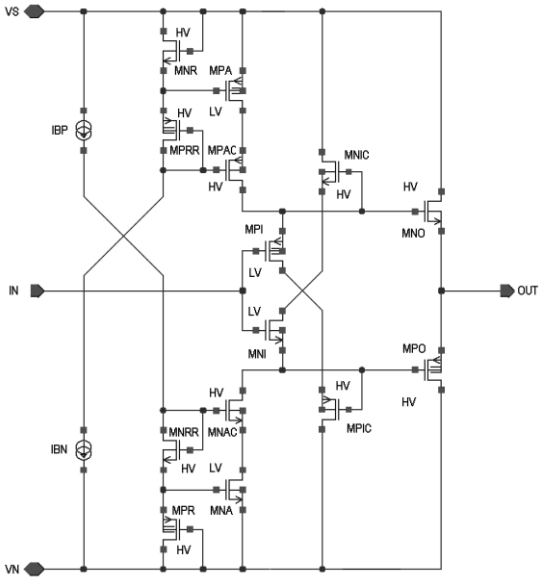

Figure 3: Improved version of the proposed buffer.

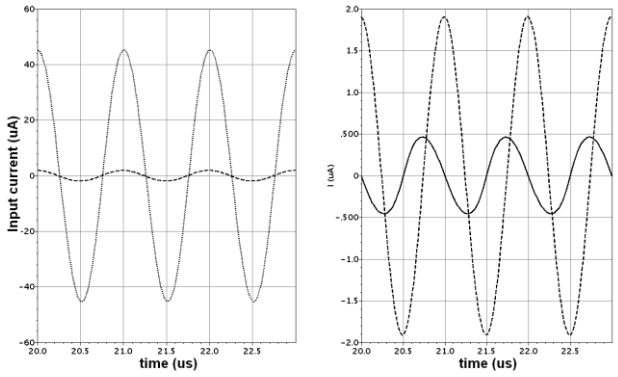

Figure 4: Comparison of 1 MHz input current waveforms for different voltage buffers: source-input – dotted, gate-input – dashed, proposed – solid line.

These high-voltage auxiliary and input-stage transistors primarily are intended to be safety devices. Their presence and way of connection enable application of low-voltage transistors as primary auxiliary and input-stage devices. These low-voltage transistors are easy to match, which improve quality of their voltage-current-voltage signal processing path. This in turn produces closer values of gate-source voltage drop at auxiliary and then input-stage transistors.

Moreover, these high-voltage auxiliary and input-stage transistors work as cascode devices, keeping drain-source voltages of primary low-voltage auxiliary (MNA, MPA) and input-stage (MNI, MPI) transistors almost constant and almost equal one to one another. This additional feature makes the cooperation of auxiliary and input-stage transistors very precise and their gate-source voltage drops nearly identical.

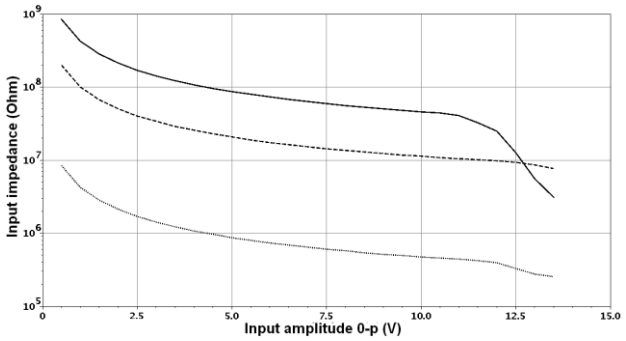

Figure 5: Comparison of large signal input impedance for 1 MHz input sine waveform of voltage buffers: source-input - dotted, gate-input - dashed, proposed - solid line.

The buffer structure presented in Figure 3 is expected to offer precision of voltage gain similar to that of source-input buffers, and high input impedance typical for gate-input voltage buffers. Presented simulations verify properties of the proposed unity-gain voltage buffer.

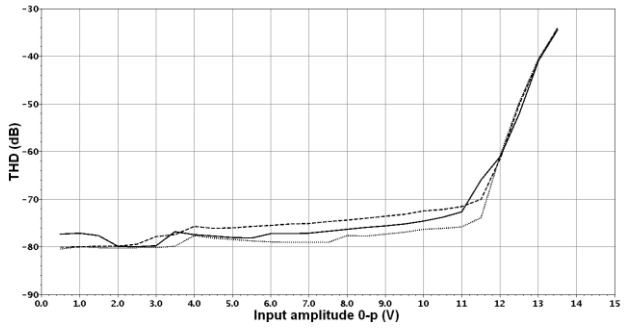

Figure 6: Comparison of output waveform total harmonic distortion (THD) of buffer driven with 1 MHz input sine waveforms: source-input - dotted, gate-input - dashed, proposed - solid line.

4 SIMULATIONS

Due to original automotive application requirements, the presented circuitry is designed to work properly with 24 V of high supply voltage and 5 V of low supply voltage. These are safe values for the utilized process, which is HV 0.8 µm BCDMOS SoI. The high supply voltage is set to be 27 V during simulations, as it is the maximum practically possible supply.

All the presented simulations are performed for a source-input buffer (dotted line), a gate-input buffer (dashed input) and a final version of the proposed buffer (solid line). All presented parameter simulations are performed for 1 MHz sine input waves, amplitudes in range of 0.5-13.5 V. Input voltage offset is equal to 13.5 V.

Figures 4 and 5 clearly show the largest input impedance of the proposed buffer. Its input impedance is larger than that of the gate-input buffer, due to cascode-like structure of the proposed circuit.

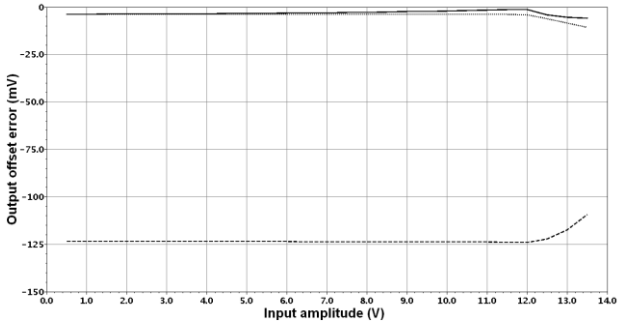

Figure 7: Comparison of offset voltage errors for 1 MHz input sine waveforms, for buffers: source-input - dotted, gate-input - dashed line, proposed - solid line.

Figure 6 shows small and similar values of THD for all checked buffer configurations. Of course, increase of input waveform frequency deteriorates these values.

Figure 7 presents offset voltage errors between output and input voltage. The proposed buffer is clearly free from offset level shift, which is typical for gate-input buffers.

Figure 8 presents values of voltage gain of the source-input, gate-input and proposed buffer. The proposed buffer offers unity-gain precision at least comparable, or even better than the source-input buffer.

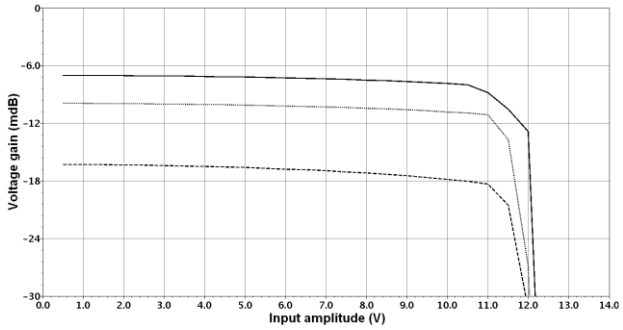

Figure 8: Comparison of voltage-gain for 1 MHz input sine waveforms, for buffers: source-input - dotted, gate-input - dashed line, proposed - solid line.

The price to pay is the voltage-range reduced due to the structure of imitations of the source-input stages, which in turn drive auxiliary transistors that form output stage of current mirrors that polarize input stage of the buffer.

In case of high-voltage systems, usually working with supply voltage levels up to several tens of volts, this limitation may usually be of limited importance.

Simulated bandwidth (for 10 V 0 to pick input) of the proposed buffer is similar to this of the gate-input buffer, due to same input structure and is equal to about 10 MHz.

5 CONCLUSIONS

The unity-gain voltage buffer structure presented in the paper offers interesting set of properties. In a way, it is a kind of mix a gate-input and a source-input buffer structures, constructed to get best of both these structures. The proposed buffer offers precision of voltage-gain, minimal input-output voltage shift comparable to those of the source-input buffer. On the other hand it offers input impedance even superior to that offered by the gate-input buffer.

The proposed buffer can be used as an effective alternative for gate-input and source-input buffers in numerous applications.

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