Application of Micro-channel Cooling to the Local Thermal Management of Detectors Electronics for Particle Physics

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ABSTRACT:

Micro-channel cooling is gaining considerable attention as an alternative technique for cooling of high energy physics detectors. This is of particular interest for future trackers, where large surfaces are involved and the amount of material must be drastically reduced. Combining the flexibility of standard micro-fabrication processes with the high thermal efficiency typical of micro-fluidics, it is possible to produce effective thermal management devices well adapted to different specific applications. The first case presented is the NA62 GTK silicon pixel detector, where low temperature liquid fluid will be circulated in a micro-fabricated silicon plate locally thinned to 130 μm in the detector sensitive area. Other applications are presently being developed for evaporative cooling in the context of the ALICE and LHCb detector upgrades at LHC. In the former case the devices are being optimized for low pressure/room temperature evaporation; in the latter for high pressure and temperature below 0°C.

KEYWORDS: micro-channels, thermal management.

1 MICRO-CHANNEL COOLING IN HEP

Local thermal management through micro-fluidic devices is already under study for possible implementation in future 3D architectures for high power computing [1, 2]. In this context, micro-fabricated cooling devices, capable of dealing with power densities up to 700 W/cm^2 have been recently proposed. Examples span from 2 mm thick silicon assemblies designed for single phase water cooling to thicker copper plates optimized for two-phase refrigerants. When designing the on-board cooling for High Energy Physics (HEP) tracking detectors, the power densities involved are two orders of magnitude lower. However, large surfaces are involved and, depending on the detector size, total heating powers up to few tens of kW must be removed. For these applications some important parameters must be minimized, i.e.:

- The amount of material crossed by particles;
- The temperature difference between heat source and heat sink for a given quantity of heat to be removed;
- The temperature gradients on the surface of the sensor.

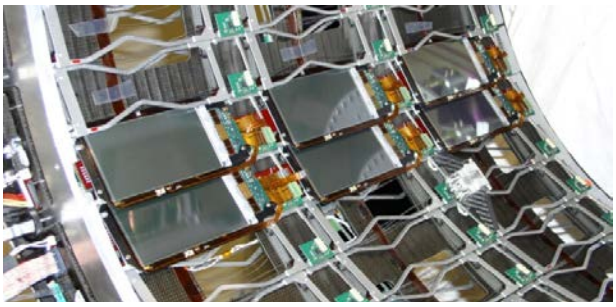

Figure 1: Typical cooling pipe network in today's trackers

Furthermore, the detector layout is often very packed and geometrically complex, thus only limited space is available for piping and connections. In many cases, in order to preserve the silicon sensor from severe degradation caused by the high level of radiation, it is also necessary to operate and maintain the detectors at negative temperatures (typically in the range –10÷–20°C) [3]: this increases the problems of Coefficient of Thermal Expansion (CTE) mismatch between the silicon heat source and a metal heat sink. The thermal management of today's trackers is based on complex networks of mm-size metallic pipes (Fig. 1). The pipes are locally brought in connection with the heat sources through complex heat spreaders, specifically designed to be compliant with mutual displacements due to CTE mismatch. Due to the small contact surfaces and the long chains of thermal resistances, the temperature difference between the module surface and the coolant ranges typically between 15 and 20°C (see e.g. [4]).

Local thermal management through silicon micro-fluidic devices is a good candidate for solving all the above mentioned issues [5, 6]. The concept, schematically depicted in Fig. 2, is simple: a thin micro-structured silicon plate with the same shape and size of the detector module to be cooled is placed in contact with the heat source via an adhesive layer.

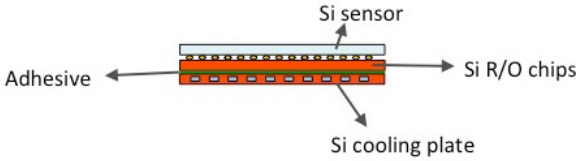

Figure 2: Scheme of micro-channel cooled detector module

As the contact surface between the heat source and the heat sink is maximized and the power density is not high, the thermal conductivity of the adhesive layer is not particularly important. The conductive heat transfer is dominated by the thermal conductivity of silicon (150 W/mK at room temperature). Few tens of μm of adhesive: are only needed to provide a contact between the cooling plate and the chips, avoiding air trapped at the interface.

The minimization of material is naturally addressed by this scheme, as only a thin structured layer of silicon is introduced in the sensitive area. No additional bulky mechanics is required to bridge the heat into the cooling pipes, and any pipes distributing and collecting the cooling fluid can be moved in more favorable regions.

The high heat transfer coefficient typical of micro-channel flows, associated with the large exchange surface involved, allows for small temperature differences between heat source and heat sink for a given quantity of heat to be removed The geometry and the micro-channel patterning of the silicon cooling plate can be tailored to the specific power distribution and shape of each detector module design. It is therefore possible to get an even temperature distribution on the sensor surface. Finally, as only silicon or CTE-matched borosilicate is used for the fabrication of the micro-fluidics cooling devices, all problems of CTE mismatch between the silicon of the tracking module (chip and sensor) and the heat sink are suppressed.

2 STRUCTURAL ISSUES

The fabrication of the cooling devices relies on standard micro-fabrication steps: photolithography, channels and manifolds etching; bonding of unstructured wafers to close the micro-channels; thinning of the assembled cooling plates and device dicing. The thinning can be operated on the whole wafer surface by grinding and CMP, but in some cases it is mandatory to reduce to the strict minimum required for structural purposes the material introduced in the sensing area of the detector modules. In this case a further plasma or wet etching operated on selected wafer regions provide a local selective thinning. For reliable operation, the key point is the final structural resistance with respect to the pressure built up inside the hydraulic micro-circuit. For a given flow condition, this is linked to the dimension of the unconstrained wafer surface exposed to the pressure. Assuming a perfect bonding between the structured wafer and the unstructured cover, it is possible to estimate the maximum pressure attainable in a straight rectangular channel as a function of the channel width and of the thickness of the cover through a simplified 2D Finite Element model. The numerical results – partially confirmed by preliminary experiments [6] – are reported in Fig.3 for Borosilicate and Silicon covers of different thicknesses.

The trends clearly show that up to the typical bonding strength of 10÷20 MPa (100÷200 bar), relatively high pressures can be safely applied even with very thin covers for channel widths smaller than 250 μm. The superior mechanical properties of silicon clearly permit to produce more robust devices and/or to minimize the material. However, even small unbonded areas in the structured region of the wafer can lead to large surfaces where the hydraulic pressure is exerted and very high internal stresses may develop. In this respect, the use of a silicon cover has the disadvantage that Direct Silicon Bonding (DSB) is extremely demanding in terms of surface roughness and wafer planarity: this may create difficulties in presence of deep etchings patterned on large surfaces with reduced bonding areas of the order 50÷75%. As anodic bonding between silicon and borosilicate is more compliant with surface and planarity defects, the use of specific CTE-matched borosilicate glass covers can be envisaged for all application where the operating pressures are small and/or cover thicknesses above 200 μm are allowed. The use of an intermediate thin film of borosilicate for Si-Si anodic bonding [7] is also currently investigated as a viable alternative to DSB.

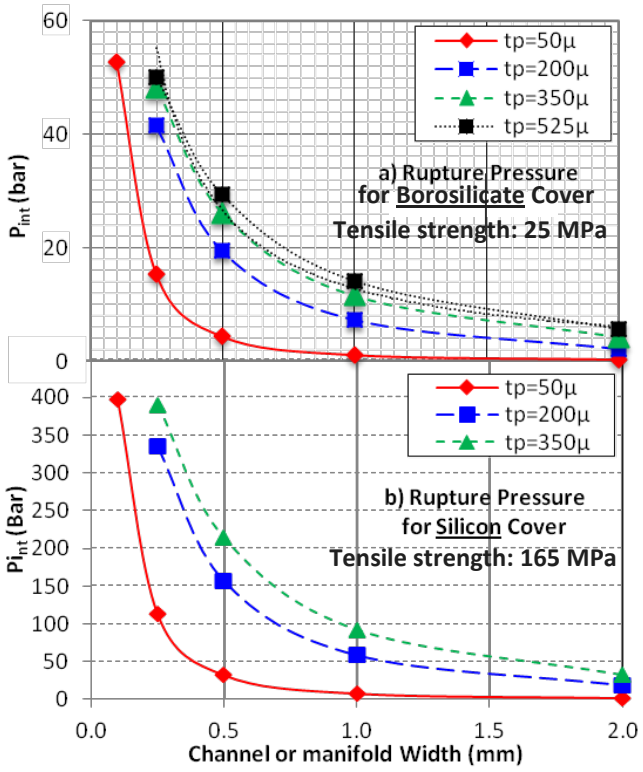

Figure 3: Breaking hydraulic pressure in a straight rectangular channel for different cover thicknesses: a) Borosilicate cover; b) Silicon cover

3 FIRST HEP APPLICATIONS

Three main lines of investigation are currently pursued for HEP applications: (1) a low temperature single phase liquid cooling; (2) a room temperature, low pressure two-phase cooling; (3) a low temperature, high pressure two-phase cooling. They will be detailed in the following.

3.1 NA62 GTK detector

The application where the development phase is most advanced is the GTK detector of the NA62 experiment [8]. The 48 W locally dissipated by the electronics in each 6×4 cm^2 GTK module, must be removed keeping the sensor temperature always below 0°C (or preferably lower) and spatially uniform within ±3°C around the average. The maximum silicon thickness allowed for the cooling device is 150 μm in the 6×3 cm^2 central sensitive area, but can be increased out of this region, where the digital part of the chips is placed. The design of the thermal management device is based on 200 parallel cooling channels 200 μm wide and 70 μm deep separated by 200 μm walls.

The channels cover the entire detector surface and the cold liquid (C_6F_{14}) is distributed and recollected via 2 inlet and 2 outlet rectangular manifolds 1.6 mm wide and 280 μm deep. The structure etched in a 4" wafer is shown in Fig. 4 (a), together with a SEM image detailing the distribution manifold and the channel inlet. Figure 4(b) schematizes the cross section of the final cooling device: after bonding, the silicon cover is ground to 100 μm. The region where the detector module is glued is then further thinned to 30 μm. On the back side of the device, where the holes for the hydraulic connectors are opened, a second selective thinning is performed in order to minimize the material in the sensitive area.

Prototypes of this thermal management device have been produced and submitted to thorough testing in realistic operational conditions [9]. Even in the most unfavorable combination of power dissipation, with a power density of 4 W/cm^2 in the two digital chips regions and of 0.5 W/cm^2 in the sensor area, the temperature variation over the whole surface of the detector module is smaller than 6°C. The temperature difference between the fluid and the warmest point on the detector surface is in the range 5÷8°C. The devices can stand a pressure of 18 bars before failing in the manifold region and have been submitted to long term cycled pressure tests up to 12 bars without any observable deterioration. This provides a comfortable safety margin with respect to the 6 bars maximum pressure difference to the environment observed in operation, with the nominal 10 g/s flow rate of liquid C_6F_{14} at –20°C.

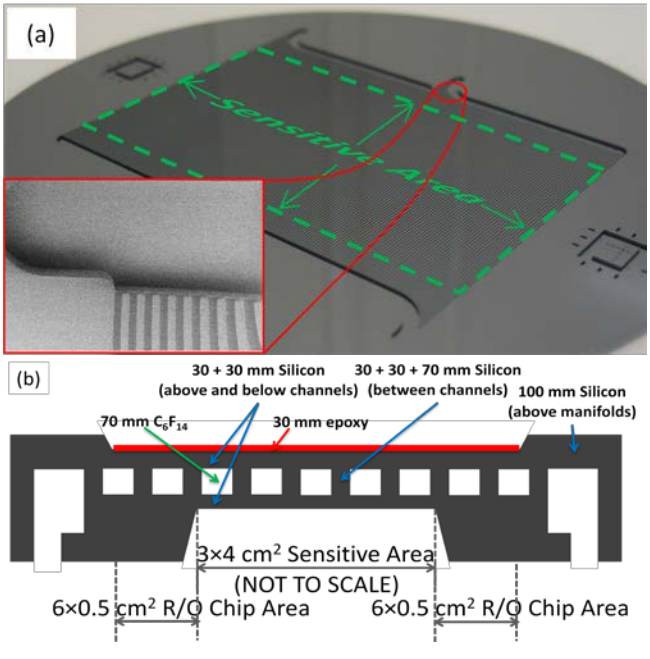

Figure 4: GTK cooling: (a) The device structured in a 4" Si wafer; (b) Cross-section scheme of the cooling device

In order to profit from the uneven distribution of thermal power in the GTK electronic for a further minimization of the material in the sensitive area, an alternative design, shown in Fig.5 (a, b), is presently under evaluation.

In this case cooling channels are only placed in the digital chip region at the periphery of the detector module, and any additional material is removed from the sensitive area, where the power dissipation is 8 times lower. Two narrow independent hydraulic circuits are etched in a silicon frame. As the cooling device is just outside the sensitive area, the requirement on the thickness can be relaxed, the channels can be deeper and a borosilicate cover can be envisaged. Preliminary results indicate that this option can provide a viable alternative to the baseline described above, depending on the final power distribution and on the thickness of the electronic chips, which directly concurs to the thermal management performance.

3.2 ALICE ITS detector upgrade

The second investigation is performed in the framework of the ALICE ITS detector upgrade [10]. In this detector module the heat is only produced along the pixel module edges, where the digital part of the electronics is located.

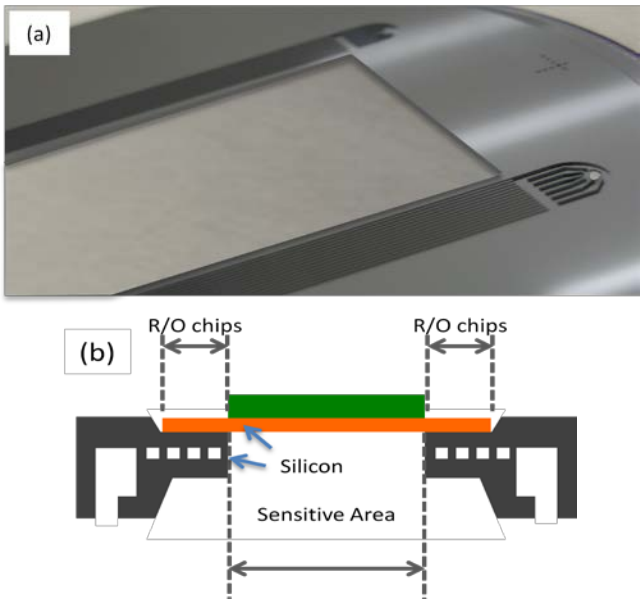

Figure 5: Alternative design for the GTK cooling: (a) The device structured in a 4" Si wafer; (b) Cross-section scheme

The electronics must be kept at room temperature, and any non necessary material must be removed from the sensitive area. A frame configuration is therefore particularly suited for the cooling device. Two-phase C_4F_{10} flow at 2÷3 bars is envisaged for this application: the cooling device prototype shown in Fig 6 directly incorporate in the channel design the inlet orifices required to equalize the two-phase flow distribution and avoid vapor backflow [5]. Thermal tests are ongoing, with very encouraging preliminary results.

Figure 6: Prototype of ALICE ITS cooling device

3.3 LHCb Velo detector upgrade

The third configuration is the one studied as a possible alternative for the thermal management of the LHCb VeLo upgrade [11]. The active electronics of this detector module dissipates 2 W/cm^2 over a surface of 2.8×4.2 cm^2 and must be kept well below 0°C by a two-phase CO_2 flow. Due to its low viscosity and superior thermal properties, CO_2 is particularly well suited for micro-channel application [5]. The detector surface out of the power dissipation region is used in this case to force the CO_2 through a long initial channel section 30x100 μm^2. In this way an evenly distributed flow at saturation conditions is obtained at the entrance of the heat dissipation region, where the channel width is increased to 200 μm (Fig. 7). The requirement on material is less stringent for this application, and a total silicon thickness up to 1 mm can be envisaged. However the pressure involved with the use of CO_2 is very high (up to 60 bar at room temperature) and high quality DSB is mandatory. The first prototypes are presently in production.

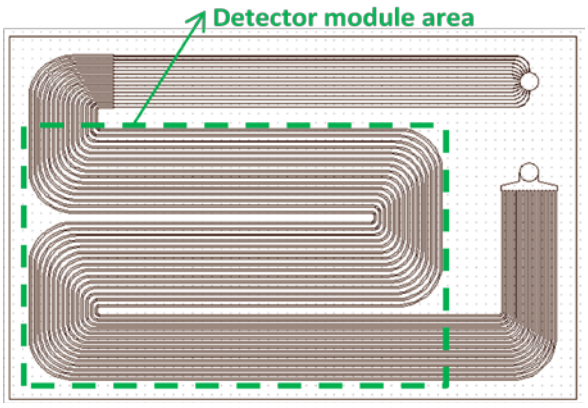

Figure 7: Mask geometry for the LHCb Velo cooling device

4 CONCLUSIONS

Silicon micro-channel cooling devices are being evaluated as a solution for the local thermal management of future tracking devices, where material limitations are a major concern. Such thin cooling plates can provide evident advantages in terms of cooling efficiency, material reduction and suppression of CTE mismatch problems. The flexibility of standard micro-fabrication processes allow to tailor the design of the thermal management devices on the specific needs of each detector module, providing optimized solutions for different applications.

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