

# Fabrication and Characterization of Nanoscale Tellurium Fuses for Long Term Solid State Data Storage

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## ABSTRACT

Many digital data storage methods are limited to data retention times fewer than 10 years. To allow permanent data storage, we have developed an electronically programmable solid state data storage solution. Using electron beam lithography, we have fabricated nanoscale fuses onto silicon chips using Te as the fuse material. The writing voltage required for fuses between 10  $\mu\text{m}$  and 500 nm has been determined. Fuses that have minimum features of 500 nm can be programmed with a writing voltage less than 10 V and a power of 1.5 mW. Finite element analysis was used to estimate the temperature of the fuses at the writing voltage. Larger step voltages (20 V and 30 V) were applied to 500 nm fuses to determine if large gaps could be formed across the fuses by increasing the writing voltage and gaps up to 700 nm could be formed. Characterization of the fuses before and after programming was done by scanning electron microscopy.

**Keywords:** archival data storage, fuse, WORM, tellurium, memory, OTP-PROM

## 1 INTRODUCTION

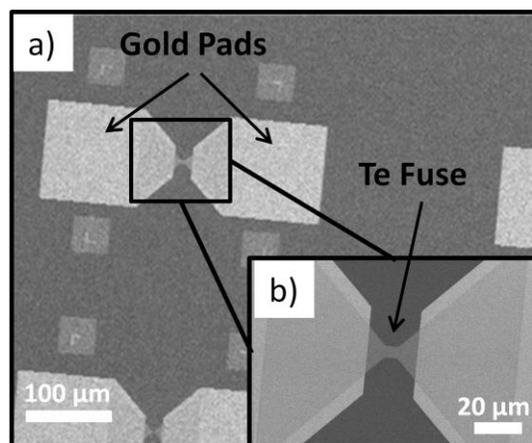
Many common data storage methods, including flash memory, most writable CDs and DVDs, and hard disk drives are limited to data retention times less than 10 years.<sup>1-3</sup> However, longer term memory devices are desirable for many applications that include document and photo storage. In order to develop longer term memory devices new materials and memory device geometries must be developed.

To keep up with the demand for ultra portable devices with high data density, electronically readable and writable devices are desirable. High data density is possible with electronically read and written devices since the size of the individual cell is limited only by the fabrication method rather than by the hardware that does the programming. One electronic device that is promising for long term data storage is write-once-read-many times (WORM) memory, due to the permanent nature of the programming process.

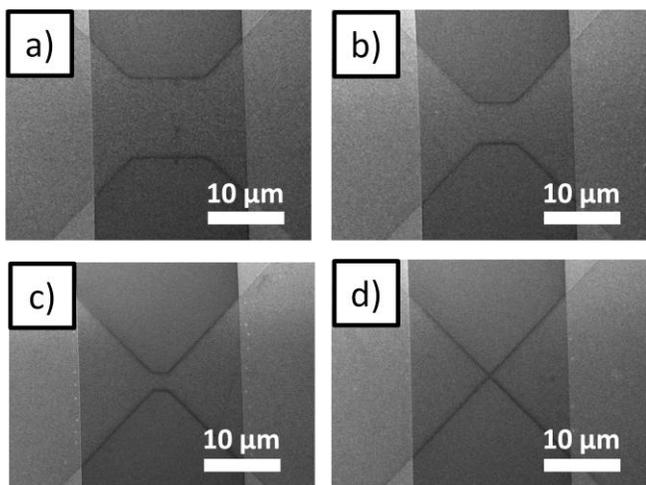
A nanoscale fuse structure is a geometry that is commonly used for WORM devices.<sup>4-6</sup> In the geometry shown, the narrowest region of the fuse is the portion with the highest resistance. This means that most of the power

will be dissipated across this region when a voltage is applied across the fuse, and under a sufficient voltage (or writing voltage) this region will heat up and blow.

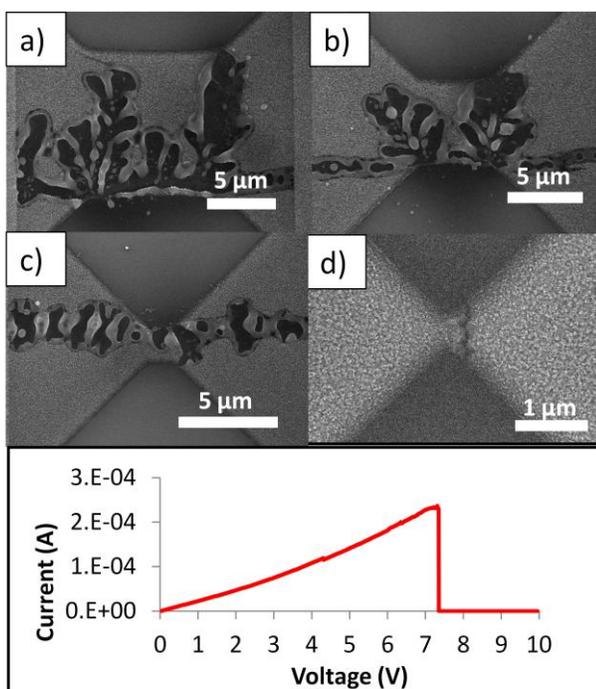
In order to use this idea to develop an effective long term memory device, a fuse material must be chosen that, when programmed, will undergo a large physical or structural change to inhibit reconnection across the blown portion of the fuse. Additionally, low power requirements would be beneficial for a more efficient device; current fuse devices require a programming power of  $> 10$  mW. One promising material to meet these requirements is tellurium. It has a low melting point of 720 K, which will likely allow programming to be done with low power. In a report by Abbott et al, Te was shown to be an effective material for the write layer in CDs and DVDs since it can melt and open up large holes very quickly when struck by a 15 mW laser pulse.<sup>7</sup> This property provided high optical contrast for recording and reading CDs and DVDs. In this report, we have made Te fuse devices to function similarly because the power dissipation under an applied voltage will cause very local heating to the narrow portion of the fuse, causing a hole to open in this region. Large holes would make it unlikely that reconnection could occur over time, and that Te, or related materials, could be used for long term WORM devices.



**Figure 1.** Geometry of Te fuses. (a) The entire structure with Au pads, which provide low resistance contact for external micromanipulator probes. The Te fuse is fabricated between the Au pads. (b) A closer view of the fuse geometry between the Au pads. The fuse in this view is 5  $\mu\text{m}$  wide at its narrowest point.



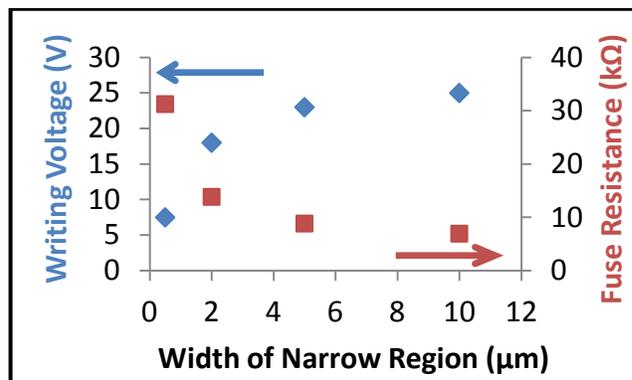
**Figure 2.** Close up images of the different fuse sizes fabricated. a)-d) show fuses with a width of 10  $\mu\text{m}$ , 5  $\mu\text{m}$ , 2  $\mu\text{m}$ , and 500 nm in the narrowest region, respectively.



**Figure 3.** SEM images of fuses after voltage ramping. (a), (b), and (c) show the 10, 5, and 2  $\mu\text{m}$  devices, respectively. Here there is evidence of much material movement before a gap was formed completely through the fuses. (d) shows the 500 nm device. Here only a small crack was necessary to form a gap through the fuse. The plot below the figures shows the current-voltage curve for the device in (d) as the voltage was ramped. At about 7.5 V the fuse blew after which no current was detected.

## 2 METHODS

Prior to fuse fabrication 200 nm of  $\text{SiO}_2$  was grown thermally on each sample. Next, Au pads were fabricated by electron beam lithography (see Figure 1a) to provide low



**Figure 4.** The writing voltage and fuse resistance for each fuse width tested showing the fuse resistance decreasing as the width of the narrow region increased and that the required writing voltage decreased with decreasing fuse width.

resistance contacts for external micromanipulator probes. The gap between each pair of Au pads was 20  $\mu\text{m}$ . Fuses were then fabricated between the contact pads in a second electron beam lithography step (see Figure 1b), where the width of the narrow region was 10  $\mu\text{m}$ , 5  $\mu\text{m}$ , 2  $\mu\text{m}$ , 1  $\mu\text{m}$ , or 500 nm (see Figure 2a-d). All fuses tapered at a 45° angle from the widest point to the narrow portion that was reached at the desired width. Tellurium was deposited by DC magnetron sputtering at 20 W in an argon flow gas to a thickness of 200 nm.

Electrical properties and the required writing voltages of the Te fuses were tested by ramping a voltage across the probes using either LabView (0 to 10 V) or an HP Harrison 6289A DC power supply (up to 50 V). The current was measured either with an Ithaco picoammeter or a multimeter connected in series. In these tests the voltage was ramped continuously until a significant drop in the measured current was seen. The minimum writing voltage is defined as the voltage at which the current drop was measured during these ramping experiments. Finite element analysis was used to estimate temperatures at the writing voltage for each fuse size.

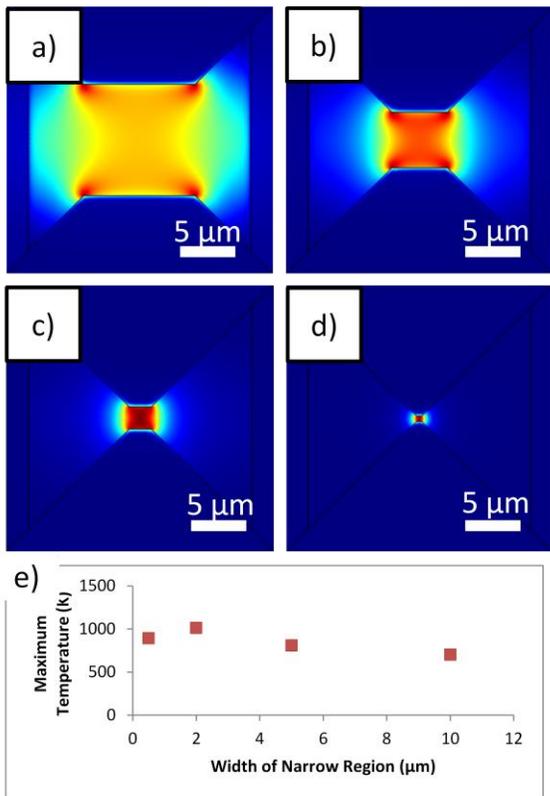
Next, larger step voltages were applied to the smallest fuse (500 nm) to maximize the size of the gaps formed. This was done using the HP power supply at both 20 V and 30 V.

Characterization of the fuses was done using scanning electron microscopy (SEM).

## 3 RESULTS

During voltage ramping on all fuses there was a voltage at which the current fell below what could be measured with our ammeter ( $< 10$  nA), indicating that upon blowing it is likely that no electrical connection remained across the fuse. Figure 3(a-d) shows SEM analysis of the 10  $\mu\text{m}$  - 500 nm fuses after blowing. Figure 3e shows the current-voltage curve for the device shown in Figure 3d.

Only a small crack appeared in the blown 500 nm



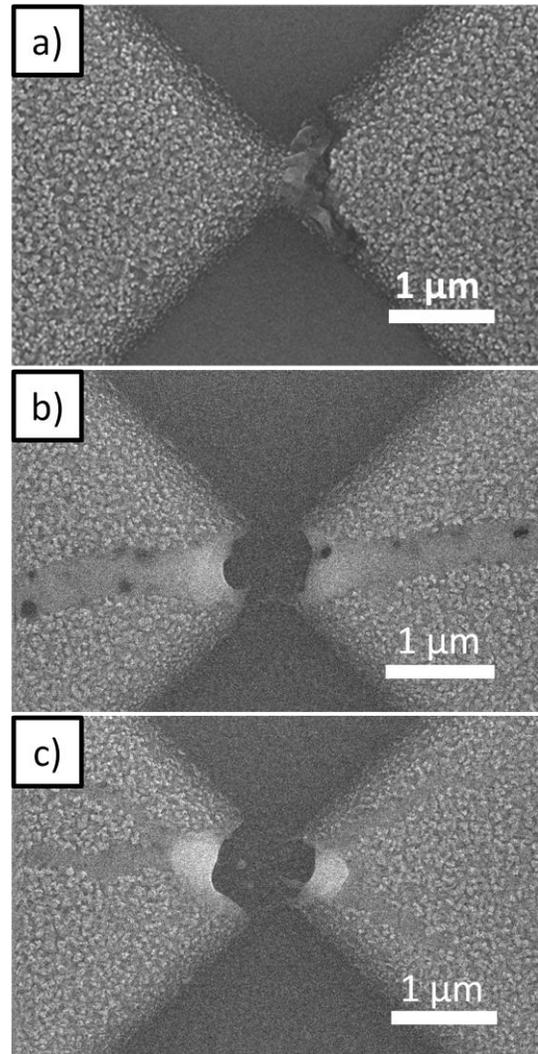
**Figure 5.** (a)-(d) Finite element analysis simulations for each of the fuse sizes. The blue regions are the coldest and the red regions are the hottest. (e) A plot of the maximum temperature for each of the fuse sizes showing a fairly consistent temperature for blowing the fuses.

fuse. However, the 2 - 10 μm blown fuses showed much larger scale damage. Figure 4 shows the writing voltage and resistance for each fuse size.

As shown, the voltage required to blow the fuses increased as the width of the narrow region increased. Additionally, the fuse resistance increased as the width of the narrow region decreased. This resulted in a large decrease in the writing power from 90 mW to 1.8 mW as the width of the fuses was decreased.

Finite element analysis was done using the appropriate fuse geometries with their respective applied writing voltages. These simulation results are shown in Figure 5a-d. The color scheme for these figures has blue as the lowest temperature and red as the highest temperature. The plot in Figure 5e shows the maximum temperature for each fuse width. The temperatures corresponding to the voltages required for writing are fairly consistent across each device with the average temperature being 850 K, which is slightly higher than the melting point of Te (720 K). It is possible that the temperature needs to be higher than the melting point in the narrow region to allow enough mobility for the Te to move outward from the center of the fuse.

In a data storage device it is desirable to have fuses which are as small as possible to achieve high data density, however, our experiments showed the 500 nm fuse devices,



**Figure 6.** (a) A Te fuse where the voltage was ramped from 0 until it blew. (b), (c) Step voltages with magnitudes of 20 V and 30 V, respectively, were applied across the fuses.

our smallest tested, to only have a small break across the fuse (~15 nm), which may not be highly stable, thus is not desirable for long term storage. To determine if a larger hole could be opened in smaller devices, step voltages of 20 and 30 V were applied across 500 nm fuses. SEM images of these fuses following the voltage tests are shown in Figures 6b-c, while Figure 6a shows a fuse that was blown by ramping up to 7.5 V for comparison. These images show that immediate application of larger voltages does indeed create larger gaps in the fuses. The average gap sizes in Figures 6b and 6c are 615 nm and 700 nm, respectively.

## 4 DISCUSSION

We have shown successful programming of Te fuses. However, in order for these devices to be useful for long term data storage the following must be considered. First,

they must be stable in both the on and off states, and second, the writing voltage must be scalable with decreasing device size.

The large gaps formed from applying higher step voltages are very promising for long term memory devices. It is unlikely that reconnection could occur across gaps as large as those which we have formed. To verify this we applied 10 V across the fuse device in Figure 6c for 62 h and saw no signs of reconnection over this time period. Longer tests would be useful for further verification.

One possible limitation of Te as the fuse material is its relatively low resistance to oxidation; it is possible that oxidation could occur in an environment of high temperature and humidity resulting in a loss of conductivity across the devices. This low stability would effectively turn 1s into 0s and corrupt the data. Further work must be done to remove the possibility of oxidation of the Te. Solutions to this issue could include using a more stable alloy of Te that would exhibit the same blowing properties or developing a method to encapsulate the fuses to prevent reaction with oxygen and water vapor from the atmosphere.

The decrease in voltage requirements for decreasing fuse size indicates that this method can be scaled to smaller devices and still be writable by standard voltages available in PCs today. This scalability is likely caused by the relationship between device resistance, the temperature that the fuse blows, and the writing voltage. We expect that the temperature ( $T_b$ ) of the fuse before it blows is proportional to the power dissipated per unit width across the fuse. This can be represented by:

$$T_b \sim \frac{V_w^2}{R} \frac{1}{W} \quad (1)$$

where  $V_w$  is the writing voltage,  $R$  is the resistance of the fuse, and  $W$  is the width of the fuse. From our simulations we see that the temperature required to blow the fuse is fairly constant, so we will assume this is a constant for all fuse sizes. Additionally, we can derive the resistance as a function of the fuse width to be:

$$R = A - B \ln(W) \quad (2)$$

where  $A$  and  $B$  are constants that depend on the resistivity and thickness of the of the Te, and Equation (2) matches the measurements in Figure 4 very well. Using Equation (2) we can rewrite Equation (1) just before blowing to be:

$$T_b \sim \frac{V_w^2}{A - B \ln(W)} \frac{1}{W} \quad (3)$$

After expanding and simplifying the denominator of Equation (3) for only small values of  $W$  this becomes roughly:

$$T_b \sim \frac{V_w^2}{CW} \quad (4)$$

where  $C$  is a constant dependant on  $A$  and  $B$ . From (4) we can easily see that the writing voltage is proportional to the root of  $W$ :

$$V_w \sim \sqrt{CT_b W} \quad (5)$$

Thus as the width decreases so does the voltage. This is advantageous for the fabrication of high density arrays of these fuse devices.

Using this model we can predict the scaling of the power with the fuse size. Our 500 nm fuse requires a power of 1.8 mW at 7.5 V to blow. If the fuse was scaled down to 20 nm, which can be done using state of the art optical lithography, we predict that the fuse would blow at 2.5 V and require a power of 190  $\mu$ W, which is nearly 2 orders of magnitude lower than other fuse structures. Although some optimization likely will need to be done to create larger openings in blown fuse structures.

## 5 CONCLUSION

We have developed a promising method for long term data storage using Te fuses. We have tested the writing voltages and power requirements for various fuse sizes and have used finite element analysis to determine the approximate temperature of the fuses when they blow. We have programmed fuses with a large openings by applying higher voltages and have verified that the fuses are stable under an electric field, with no visible re-growth. Additionally we have shown that the writing voltage of these fuses scales nicely as the fuse size is decreased, making this a viable method to form high density long term data storage devices.

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