Off-Chip Printed Interconnects for Ultrathin Flexible Products

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ABSTRACT

The relentless needs for increasing the functionality of microelectronic products while reducing their size and weight and having the advantages of thinness and flexibility call for novel technologies for the integration and assembly of multi-chip products. Unlike transistor performance which benefits from reduced feature size, interconnects performance, suffers from increased resistance caused by reduced size. At Terepac, we propose a methodology for delivering miniaturized microelectronics by disintegrating the complex ICs connected using off-chip interconnects with nearly no performance penalty. Terepac technologies in releasing thinned dies and printing micron scale interconnects are the key to the chip miniaturization process which becomes a demanding feature for flexible and ubiquitous electronics. The focus of this research work is on the printing technology for the assembly of components for wearable biosensor patches. The components are released using Terepac patented Photoprinting Circuit Assembly™ on flexible substrates. The morphology, electrical conductivity, and mechanical stability of the interconnects are affected by the printing process parameters, and they have been characterized to make interconnects with desired conductivity and mechanical stability.

Keywords: printed interconnects, flexible electronics, ultrathin electronics

1 INTRODUCTION

The relentless needs for increasing the functionality of microelectronic products while reducing their size and weight and having the advantages of thinness and flexibility call for novel technologies for the integration and assembly of multi-chip products. Although increasing the transistor density resulting from sub-90 nm lithography technology can meet the functionality requirements, not having the same scaling factor as transistors, I/O pads have become an important factor limiting area saving in this technology. In addition, unlike transistor performance which benefits from reduced feature size, interconnects performance, e.g., delay, suffers from increased resistance caused by reduced size [1].

In this research work, to address the aforementioned shortcomings, we focus on our printing technology for the assembly of discrete components using off-chip interconnects.

2 PRINTING TECHNOLOGY

The Terepac proprietory methodology aims at delivering miniaturized microelectronics by disintegrating the complex ICs connected using off-chip interconnects with nearly no performance penalty. To compensate for the delay, the interconnects with increased feature sizes are printed off the silicon die; therefore, there is no concern in terms of increasing area due to wider interconnects. In addition to eliminating substrate noise coupling [2], disintegration and off-chip interconnect effectively reduce the cross talk noise.

Terepac technologies in releasing thinned dies and printing micron scale interconnects are the key to the chip miniaturization process which becomes a demanding feature for flexible and ubiquitous electronics. Due to the substantial additional height of packages made by wirebonding and flip-chip mounting technologies, direct printing is considered to be an optimum method for chip-to-chip interconnects in ultrathin electronics.

In this research, we focus on our printing technology for the assembly of components for wearable biosensor patches. Figure 1 shows the chip-to-chip interconnects for an Electrocardiogram (ECG) patch assembled with disintegrated components on Kapton substrate. We use the Aerosol Jet Deposition Technology™ [3] for printing sub-30 um silver interconnects for the assembly of discrete components and thinned silicon chips. The components are released using Terepac patented Photoprinting Circuit Assembly™ on flexible substrates, e.g. PET, Kapton, Polyimide, etc., with a predefined layout [4]. After releasing, the chips, thinned to sub-50 um, are bound to the flexible substrate by an epoxy-based die attach adhesive. To reduce the risk of interconnect failure passing over the silicon die edges, round shoulders made of epoxy-based adhesives are deposited at the edges.

In the interconnect printing process, the aerosol of metallic nano-particles generated from a nano-particle suspension is deposited on the substrate in a drop-on-demand fashion. The deposition is followed by post-annealing to sinter the nano-particles and produce conductive interconnects.

The Aerosol Jet Deposition Technology™ direct write method is well suited for this application due to its drop-on-demand and later-by-layer depopsition feature. In addtion,

the prinitng process can be performed at atmospheric pressure and room temperature followed by thermal sintering at temperatures starting from 150°C depending on the material and nanoparticle sizes. Metal nanoaprticle suspensions such as gold and silver and also insulator maerials can be depsoited. Compared to other direct write methods such as ink jet printing, conformal deposition on non-planar surfaces is possible. All these features increase the flexibility and the speed of the deposition process.

In addition to the geometrical features of the inerconnects, controlled by the aerosol jet primnting parameters, the sintering parameters also affect the performance [3]. The conductivity of the interconnects is influenced by thermal sintering which is a key part of the interconnect fabrication process. The parameters involved in the sintering process are time and temperature. The temperature during the sintering process causes atomic diffsion between naoparticles. The sintering of nano-sized particles is a complex process described by various atomic diffusion mechanisms: surface diffusion, grain boundary diffusion, and lattice diffusion. In sintering of nano-particles, the dominance of a diffusion mechanism depends on the particles size. In the early stages of the sintering process, surface diffusion and grain boundary diffusion with lower activation energies than lattice diffusion are dominant which result in the densification and neck-shape strucutre of the sintered particles [5]. The conductivity of the interconnects can be correlated to temeprature and time. Figure 2 shows the resisitance of the interconnects as a fuction of isothermal sintering time. The steep drop of the resistivity in the grpahs is related to the initial stage of the sintering process invoving surface diffusion.

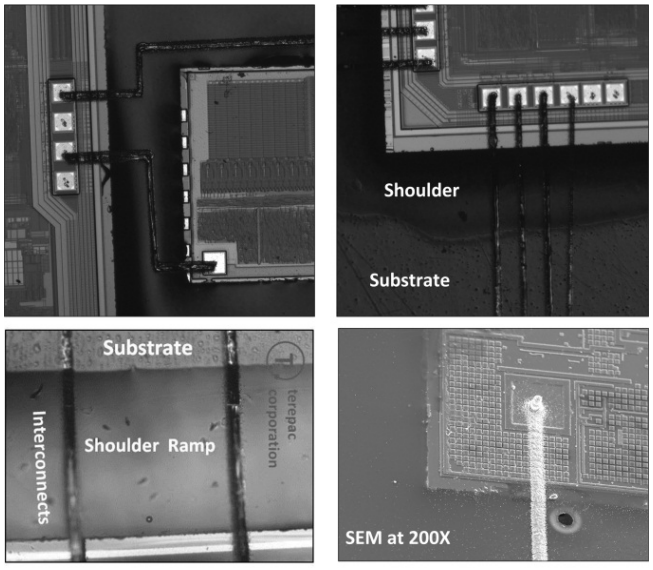

Figure 1: Microscopy images of the chip-to-chip interconnects for an ECG patch on Kapton

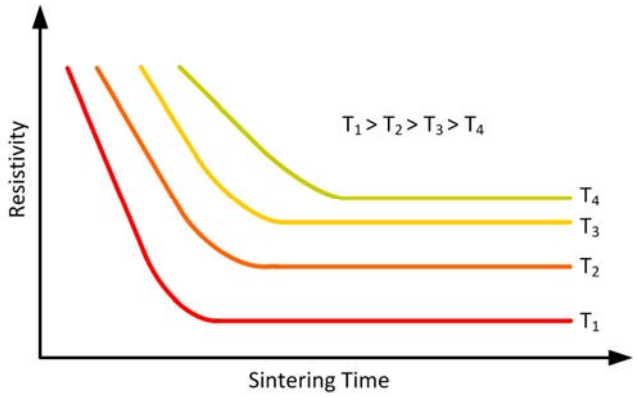

Figure 1: Resistivity as a fuction of isothermal sintering time

3 RESULTS AND DISCUSSION

The morphology, electrical conductivity, and mechanical stability of the interconnects are affected by the printing and post-annealing process parameters, and they have been characterized to make interconnects with desired conductivity and mechanical stability [4]. The annealingprocess causes atomic diffusion between particles leading to particles agglomeration and sintering. The sintered particles can be distinguished from unsintered ones by their compact and neck-shape microstructure (Figure 2) [4]. Figure 3 shows the conductivity per length for interconnects deposited on a Kapton substrate and sintered at 180°C for about 20 to 30 minutes. The sintering temperature and time have been optimized in a comprehensive study to achieve desired values of conductivity.

The functionality tests for the wearable ECG patches is under way to optimize the layout design and enhance the mechanical and electrical reliability of the off-chip interconnects.

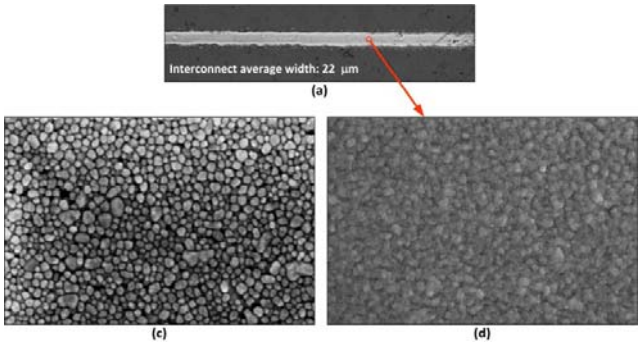

Figure 2: (a) Silver interconnect deposited on Kapton substrate, (b) microstructure of deposited interconnect before thermal sintering (average particle size : < 60nm), (c) microstructure of interconnects after thermal sintering at 180°C for 20 to 30 min

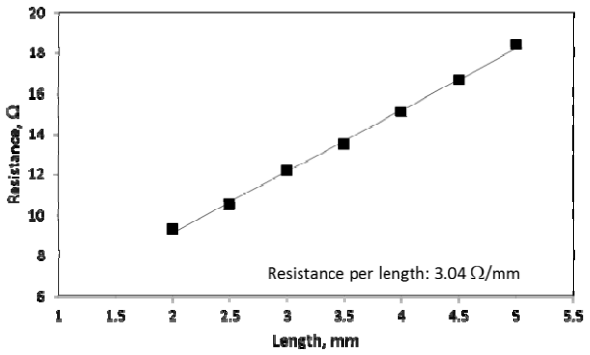

Figure 3-Resistance per length of silver interconnects sintered at 180°C

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