Inherently Radiation Hardened Electronics: An Examination of III-V Nanowire Transistors and Spin-Based Logic Devices

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ABSTRACT

This paper presents novel design concepts currently pursued for the realization of inherently radiation hardened electronics. All-around gate oxide nano-wire transistors made from Si and III-V materials, are the first innovation examined. The carriers in these nanowires have dramatically increased mobility which can be used to increase processing speed, while the transistor geometry provides an avenue for inherent radiation hardness. Secondly, this work will discuss the development of a spin-based magneto-logic search engine. The manner in which the logic is written has the potential to be radiation hardened in addition to being nonvolatile. Realization of this type of logic will have an impact on both space electronics, as well as current terrestrial electronics.

Keywords: Nano-wire transistors, magneto-logic gates, radiation hardened electronics

1 NANO-WIRE TRANSISTORS

Scaling of semiconductor devices to the nanoscale regime can lead to device and performance parameter improvements including reduction in operating voltage, increased speed and greater packaging densities. As silicon is the material of choice for a large percentage of semiconductor devices, the fabrication, analysis and testing of scaled down versions of existing Si devices has been an active research subject [1,2]. The scaling of device parameters of many structures is under consideration and theories for improved effective channel length for a fully depleted, surrounding-gate MOSFET and double-gate SOI MOSFET have been proposed [3,4]. Dimension reduction for current technol- ogies, however, has its limits set by optical lithography, and scaling of MOSFETs has complexities of short-channel- effects (SCEs). Scaling of double gate and silicon-on- insulator (SOI) Delta MOSFETs to the nanoscale regime shows promise but further scaling has been limited due to fabrication difficulties [5].

For MOS transistors, scaling studies have mainly focused on decreasing channel length to submicron dimensions while the width has remained several microns in size due to the necessity of maintaining the current driving capability (width-to-length ratio) of the transistor. True nanoscaling requires the reduction of the overall size of the transistor and not just the gate length. Such studies have recently attracted considerable research interest since the electrical, optical and thermodynamic properties of nanostructures can be significantly different from those of bulk material of the same composition [6]. MOSFETs with a nanowire channel wrap-around-gate (WAG) structure have been shown to have significantly improved carrier transport properties over conventional devices because of reduced scattering and better gate control. Additional study is necessary in order to fully determine the physical processes impacting the transport mechanisms [7].

In this work we demonstrate that the current density is enhanced in nanowire channel WAG MOSFETs as a result of higher carrier mobilities. We discuss the physical processes contributing to the increased mobility, specifically quasi-1D transport at the channel centre of such devices. For this study, we fabricated ~50 nm diameter nanowire, wrap-around-gate MOSFETs with single and multiple parallel channels and compared their characteristics with ~2 mm wide, 200 nm thick slab, top- only-gate MOSFETs that were identical in all aspects except for dimensionality of the channel region. In order to focus on the effects of scaling the channel width region, the nanowire channel length and the slab gate length were both made intentionally long (~2 mm) for this study so that short channel effects would be minimised. Simulations of carrier mobility for both nanowire WAG and slab gate devices are presented. The device conduction processes are explained in terms of changes in the channel mobility, the influence of transverse and parallel components of the channel electric field, and the impurity distribution within the channel as a result of the fabrication process. Fig. 1 shows SEM micrographs of a slab gate and nanowire gate structures before thermal oxidation. At this stage there exists two mesa structures (source and drain regions) connected by a wide slab or by wires, respectively. After the RIE step the PR and the Cr etch mask lines were removed. There is considerable damage left by the RIE step. In order to remove some of this damage, two rapid thermal anneal (RTA) steps were performed. The first RTA

was performed at 900°C for 5min in a nitrogen environment to anneal the damaged surface followed by a second RTA step for 3 min at 450°C in a hydrogen environment to passivate the Si surfaces. Completely fabricated single and multiple nanowire channel WAG MOSFETs and top-only-gate slab MOSFET are also shown in Fig. 1.

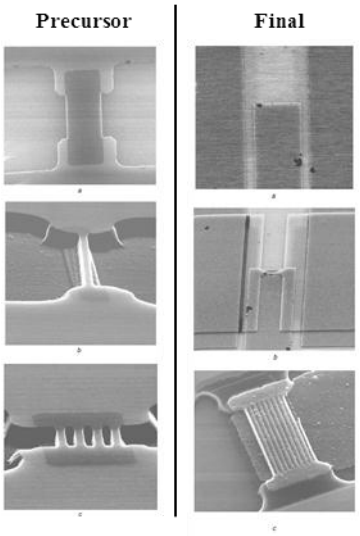

Figure 1: SEM micrographs of slab structure, single and multiple nanowire gate structures in precursor and final stages. Top) Slab structure connecting top source mesa region and bottom drain mesa region; Middle) Nanowire gate structure connecting source and drain mesa regions; Bottom) Multiple nanowire gate structure connecting source and drain mesa regions

Experimental I–V plots for both the nanowire and slab devices are shown in Fig. 2. The drain current (Id) as a function of drain-to-source voltage (Vds) for various gate biases was measured using a digital curve tracer. As seen from the plots, for similar doping profiles, gate length and gate oxide thicknesses the current–voltage characteristics of the nanowire and slab MOSFET are considerably different. The drain current in the nanowire is rather flat in the saturation region (Vds41V) compared to the significant slope in the slab device. This is due to the geometry of the slab MOSFET, in which the fringing fields at the edges of the slab significantly impact the drain current. As the channel approaches pinch-off, the carrier charge drops at the drain end and the lateral fringing field increases at the edges of the slab. Further increasing Vds causes the highfield region at the drain end to widen the channel enough to accommodate the additional potential drop, thus resulting in a further increase in the drain current. In contrast, when the nanowire device is biased in the saturation region, the effective channel length of the nanowire device is essentially unaffected since the depletion region at the drain terminal is physically restricted to ~50 nm. This effect, known as channel length modulation, is a well-known phenomenon in conventional transistor designs [8]. This phenomenon is more dominant in conventional short channel devices. Suppressing such effects in theB1Vds nanowire device (as is the case here) is of significant benefit, specifically in the development of low voltage circuit applications.

Fig. 2 shows that in the nanowire MOSFET the current is an order of magnitude less than for the slab device. Scaling to the cross-sectional area shows that the nanowire device current density is three times higher than that of the planar slab device. From the experimental data the resultant conductivities for the slab and nanowire devices are sslabB9 103A/Vcm2 and swireB3 104 A/Vcm2. This means that we can obtain the same amount of total current driving capability in nanowire channel devices that have much smaller cross-sections by configuring several nanowires in parallel. In order to understand and improve the current characteristics of the nanodevice, we also modelled the current–voltage characteristics of the transistors. We are not aware of any reported standard nanowire channel wrap-around-gate MOSFET drain current-voltage (Id–Vds) relations and in order simulate the results we developed a very simple model based on the 2-D sketch of Fig. 2. Fig. 2 shows simulated I–V characteristics for the B50nm channel device at different gate biases. The results are in agreement with the measured I–V for the fabricated single channel device as shown in Fig. 2. The close match between the simulated and measured I–V plots is an indication of the validity of the model and material parameters chosen for the simulation.

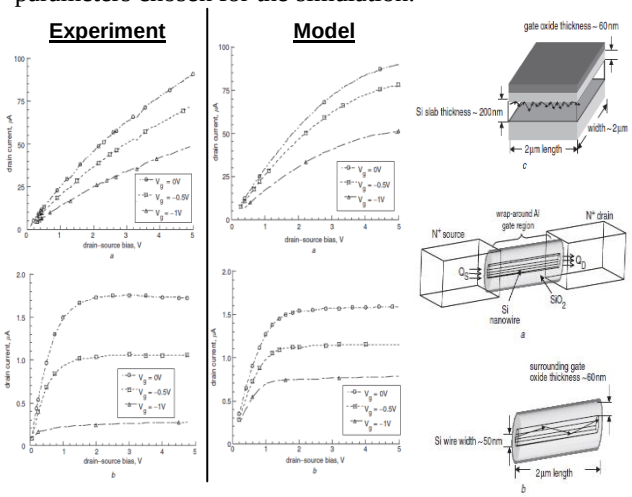

Figure 2: Experimental and model plots of drain current as a function of drainto- source bias for various gate voltages a) Slab-MOSFET and b) Single nanowire-MOSFET.

Following the success of the Si nano-wire MOSFETs, we are now turning our attention to desinging nano-wire MOSFETs using III-V materials. In Fig. 3, we show the the growth of GaAS nanowire sturctures along with a schematic for a potential all around gate oxide, nano-wire transistor. The benefit of using GaAs over Si is that in addition to the ballistic mobilities experienced by both electrons and holes, GaAs is also a direct bandgap material,

which allows for the possiblitiy of creating nanowire photosensor arrays.

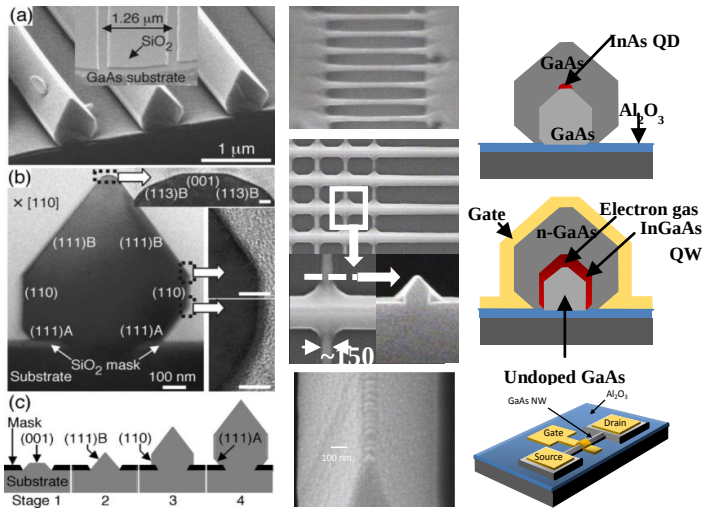

Figure 3: GaAs nano-wire structures and schematic for potential MOSFET design.

2 MAGNETO LOGIC GATES

The continued Moore's law scaling in CMOS integrated circuits poses increasing challenges to provide low-energy consumption, sufficient processor speed, bandwidth of interconnects, and memory storage. CMOS logic circuits rely on the von Neumann computer architecture consisting of central processing units (CPU) connected by some communication channel to memory. The von Neumann bottleneck caused by the communication and memory accesses is the underlying reason for the significant and widening gap between the fast improving transistor performance and our relatively stagnant ability to provide correspondingly faster program executions. Such bottlenecks are especially obvious for data intensive applications where most of the actions involve accessing or checking data. Network routers are a classical example where the Internet protocol (IP) address is compared to a list of patterns to find the best match for further processing. In a typical router, special-purpose associative tables are used where the search data (the key) is simultaneously compared with all of the table entries to find matches. Such tables allow us to fundamentally improve the processing speed. Unfortunately, conventional CMOS implementation of these circuits also suffer from scalability issues, making them ineffective for larger search problems that are increasingly relevant to modern workloads. Dery, et al. have propose a paradigm change for these search applications using spintronics, which possess fundamental advantages over CMOS in chip area and power consumption.

A magneto-logic gate (MLG) is the basic building block due to its potentially favorable properties of spin amplification, speed and scalability.[9] Fig. 4 shows a universal and reconfigurable MLG that consists of five ferromagnetic (FM) electrodes on top of a graphene layer. FM regions are inherently nonvolatile, they preserve the direction of magnetization even in the absence of any power supply. While this feature has been extensively used for robust information storage in magnetic hard drives and magnetic random access memories (MRAMs), here we show how this nonvolatility can also be used for high-performance magneto-logic. The magnetization itself reflects that the FM electrode has an unequal number of electrons with two different spin pro jections (up and down; minority and ma jority). The MLG design employs a stack of FM layers where the elongated permalloy layer (Py) is the free magnetic layer into which the information is encoded.

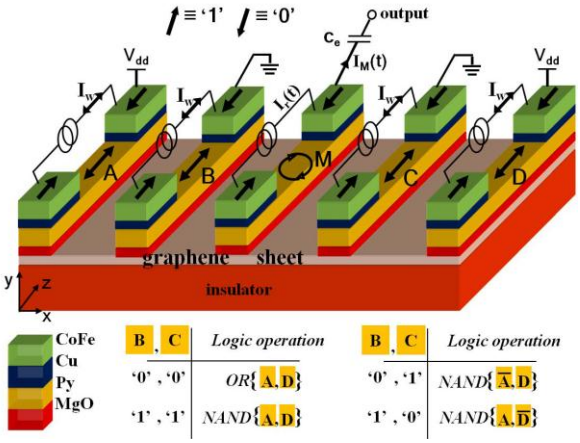

Figure 5: A universal and reconfigurable magneto-logic gate (MLG). Five magnetic terminals are deposited on top of a single layer graphene sheet. The spin accumulation profile in the sheet determines the logic result and it is governed by the magnetic directions of the biased sections (A-B and C-D).

The MLG operation relies on the generation of non-equilibrium spin accumulation when spin polarized electrons tunnel from the free layer into the graphene via the MgO tunneling barrier. The magnitude of the spin accumulation in the graphene strongly depends on the relative orientation of the magnetization directions in the free layers of the MLG. Of the five FM contacts, the middle contact (M) is used for readout and the remaining four contacts (A, B, C & D) are logic operands whose values are defined by the magnetization direction ('0' & '1' in Fig. 1). The output state is given by the Boolean expression (A xor B) + (C xor D). By reprogramming the B and C states we get a universal set of four logic operations between A and D.

The logic operation is triggered by perturbing the magnetization direction of M. The electrical response to the perturbation is governed by the potential level in the middle contact. In steady-state, the potential level is set by the zero electrical current condition, Im (t)=0, due to the external capacitor, Ce . In the case of small external and intrinsic device capacitance, the response is instantaneous and the

potential level 'follows' the magnetization direction. The transient current response depends on the RC of the system and on the spin-accumulation profile in the graphene layer. This profile is a function of the magnetization alignment of contacts A-D.[9] We propose to use graphene due to its robust room temperature spin transport and high mobility. Non-local spin- valve measurements at room temperature measurements of a lateral graphene sheet topped with ferromagnetic contacts has yielded a spin-diffusion length of 3 μm in the graphene sheet.[10]. The long spin diffusion length at room temperature is a unique property of graphene that could be further improved with material optimization. The use of tunnel barriers has recently improved the spin polarization of injected carriers to ~30%.[10]

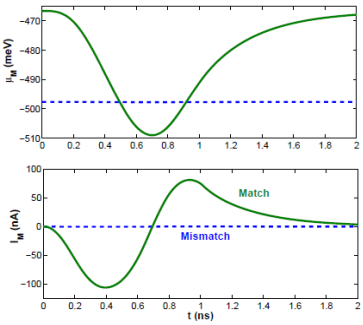

Figure 3. Modeled electrical behavior of a magneto-logic gate set for matching between the stored (B & C) and search (A & D) bits. The upper and lower panels show, respectively, the transient response of the electrochemical potential level in the middle contact and of the transient current across it.

Another novelty in the MLG design of Fig. 4 is the spin-transfer torque (STT) magnetization writing. Each of the FM contacts employs an all-metallic path with ultra-low resistance for the writing current (Iw) during the operand writing phase of the MLG. This path allows significant energy savings compared to the standard STT pillar technique based on a magnetic tunnel junction in which the writing current flows through the MgO tunneling barriers and graphene. In the writing scheme depicted in Fig. 4, the magnetic moment of the free layer (Py) of a logic operand contact (A-D) is switched by applying a nanosecond-scale current pulse Iw(t) between the two top CoFe layers of the operand contact. The magnetization directions of all CoFe regions are fixed (hard layers). A write current pulse in the opposite direction switches the magnetic moment of the free layer of the operand contact to the opposite orientation.

In addition to non-volatility, the MLG circuit enables a range of associative computing applications, whereby a large amount of information can be accessed and filtered in parallel with energy efficiency and high speed. Efficient search capabilities are clearly useful in classical examples such as network routing tables. But more importantly, these capabilities can critically impact more complex applications that are limited by the serial communication and processing von Neumann bottleneck.

The logic operations as performed by MLGs also represent a potentially large technology leap for space vehicle processing. Most importantly, it is because the logic operations appear to be inherently radiation hardened. For example, due to the manner in which the logic is stored and read, single event effects should no longer cause upset operations or failures, as could occur in a current field effect transistor. Additionally, the non-volatile logic operations are preserved in the event that systems need to be powered down to protect the electronics. This aspect results in faster times for bringing such systems back online. Finally, the scalability of this circuitry coupled with the reduced power consumption (as compared to current CMOS technology) appears to fit the tight constraints associated with space vehicle electronics designs, opening the door to potential on-board processing.

3 REFERENCES

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