Correlated Statistical SPICE Models for High-Voltage LDMOS Transistors based on TCAD

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ABSTRACT

The aim of the work is to develop a statistical SPICE model for the design of high-voltage ICs based TCAD simulations by considering process variations. From the in-line data analysis (together with initial TCAD simulations), critical process variables, which are responsible for the electrical parameter shift, have been chosen for process and device TCAD simulations. An interface between commercial process simulator [1] and Minimos-NT [2] (a device simulator developed by TUW) was also addressed, and statistical process and device simulations were performed for the high-voltage n- and p-channel LDMOS transistors implemented in a HV-CMOS technology. Finally, a statistical SPICE model implementation was done successfully as a linear combination of related SPICE parameters.

Keywords: Monte Carlo, LDMOS, Process Variation, TCAD, SPICE Modelling, Statistical Modelling

1 INTRODUCTION

Worst Case and Monte Carlo SPICE simulation is very essential for robust analog/RF and HV design. Predictable process variability (PV) SPICE simulations are usually based on adequate amount of process monitoring data (PCM). Special products need new technologies or even new integrated devices in stable processes during or before device development has been started. In this paper we benchmark the TCAD capabilities in terms of PV predictability for SPICE applications. Beside predictability and accuracy time to final SPICE model is of major interest. Especially in HV CMOS technology new devices are developed very often for new voltage levels where already calibrated TCAD tools can be used.

2 DEVICE/TECHNOLOGY DESCRIPTION

For this investigation an isolated n-channel HV MOSFET device out of austriamicrosystems 0.35um high voltage (HV) CMOS technology has been selected.

From Figure 1 the corresponding cross-section including the relevant descriptions of this device is shown. The lateral HV MOSFET is designed with 5V oxide and poly gate extending the field oxide in order to optimize the device breakdown. The drift region determines the on resistor (RON) and additionally surrounds the body as isolation from the substrate. Typical HV Transistor PCM data is measured with standard parameter extraction strategy. This extraction method requires two device geometries for deriving all necessary data of the underlying MOS transistor. These geometries are the minimum length and a long channel device.

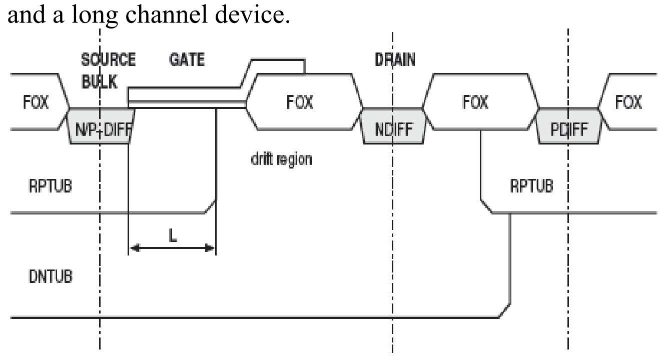

Figure 1: Schematic lateral view of the investigated n-channel high voltage LDMOS transistor

3 PROCESS VARIATION AWARE TCAD SIMULATION

The overall work can be split into two main parts, the generation of statistical data based on TCAD simulations on one hand side and their analysis and manipulation/ implementation of these data into statistical SPICE models on the other hand side. A flow derived from this is shown in Figure2, where the green box is indicating the process and device simulation. The yellow boxes take respect to the implementation into SPICE and its benchmarking. The green light box can be allocated by each part, the process and device simulation as well as the SPICE implementation and therefore builds the connection between them.

Virtual statistics generation does only make sense if its results are more quickly available than the real measurement data. Therefore, the process and device simulations were based on a minimum set of required input parameters and geometries together with efficient DOE (design of experiments) to overcome the huge amount of simulation time. For the investigated n-channel LDMOS transistor (HV-NMOS), a set of 8 critical parameters have been chosen to regard process variations as input parameters (pi) to the system.

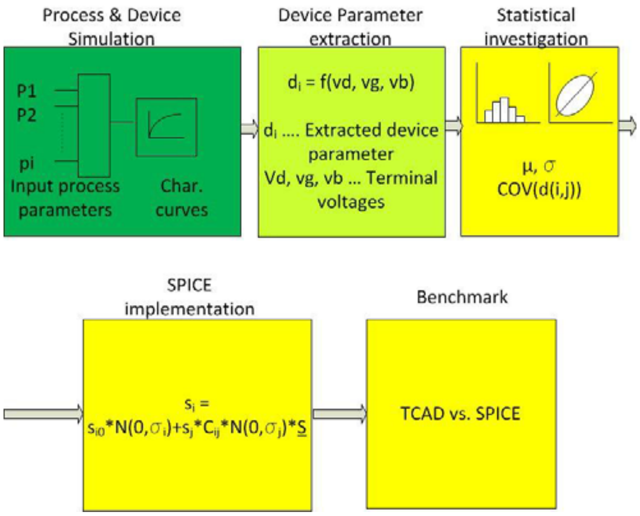

Figure 2: Flow for the generation of statistical SPICE models.

The selected parameters can be seen in Table 1. Hereby the mean value and variation range of the parameters is shown as well. The values are chosen as typical values of the parameters applied from independent measurements. The variation range describes minimum and maximum values of the parameters and can be interpreted as 3σ values of the distribution of the process parameters.

Parameter	Minimum	Mean	Maximum
SX	18	20	22
DN_DOSE	4.05E+012	4.10E+012	4.15E+012
DPOverlay	-0.1	0	0.1
SPOverlay	-0.1	0	0.1
SNOverlay	-0.1	0	0.1
PADOX_VthM	0.1	10.05	20
Vt_2p7e12	2.65E+012	2.70E+012	2.75E+012
TOXTH	-2	0	2

Table1: Input parameters for process simulation (n-channel LDMOS transistor).

In the simulations 3 levels of the parameters, the mean value, the minimum and the maximum value have been investigated. To overcome the time consuming method of 3^8=6561 full factorial combinations a Central Composite Face-centred (CCF) design was chosen [3]. For n parameters this method consists of 2^n full factorial simulations of the min/max combinations, 2n axial points of the screening analysis, and one simulation for the centre point. In sum this leads to 273 variations in 8 parameters for each, the minimum channel length device and the long channel device.

The CCF design is used to model each electrical output parameter ˆy as a quadratic model function

$$\hat{y} = x^T A x + b^T x + c \quad (1)$$

of the based input parameters x by a least square fit of A, b,
and c for all design points i

$$\sum \| y_i - x_i^T A x_i + c \| \to \min \quad (2)$$

of their simulated output parameters yi .

Because of the minimum number of input parameter permutations only three discrete variations of the input values are performed (see Figure 3a).

These setups result in unrealistic large variation ranges, standard deviations or multiple distributions of the output parameters. However, the inputs show a natural distribution and as a consequence the output shows the result of these distributions. Therefore, the methodology of comparison is chosen in a different way.

The simulated output is chosen as a mathematical approximation of the input variables. Afterwards the inputs variables are chosen normally distributed according to the measurements of characteristic values of the input (shown in Figure 3b) and are applied to the mathematical approximation. This leads to an output, in dependence of the natural distribution of input variables.

After this methodology the output variables show realistic distributions compared to measurements.

Now an analysis of output parameters can be performed. These selected output parameters for investigation are:

- The Oxide thickness TOX
- The threshold-voltage (in the linear region) Vthlin of the short device.
- The threshold-voltage (in the linear region) Vthlin of the long device.
- The saturation current IDSAT
- The on-resistance Ron.
- The body factor Gamma of the large device
- The leakage current Sleak.

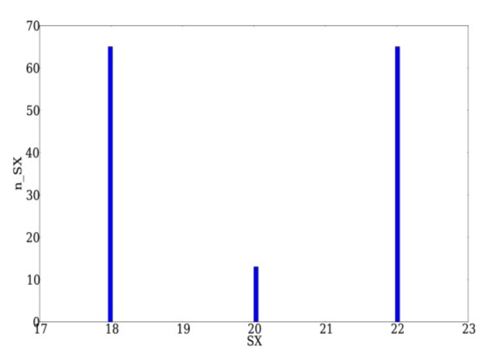

Figure 3a: Discrete input parameter values versus frequency of occurrence used for TCAD simulations.

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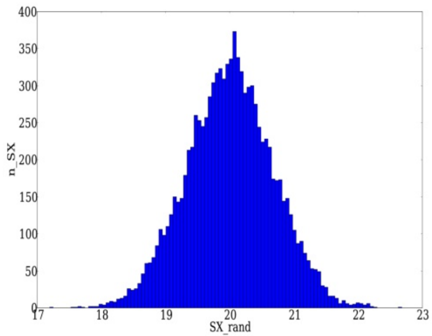

Figure 3b: Normal distributed input parameters versus frequency of occurrence after surface response method [3].

	TOX	VTHS	RON	VTHL	IDSAT	GAMMA
TOX	1	0.55 0.52	0.06 0.10	0.59 0.62	-0.28 -0.38	0.43 0.73
VTHS		1	0.40 0.32	0.93 0.92	-0.36 -0.28	0.34 0.62
RON			1	0.04 0.04	-0.86 -0.68	0.26 0.19
VTHL				1	-0.11 -0.30	0.38 0.78
IDSAT					1	-0.21 -0.39
GAMMA						1

Table3: Covariance matrix of output parameters.

4 TCAD RESULTS VS. PCM DATA

The ultimate benchmark test indicating the correctness of the environment for virtual data statistic generation is to consider the resulting data base in conjunction with already existing silicon data. The main parameters listed above have been used for benchmarking regarding sigma value and correlation.

In Table 2 the sigma values are shown for these parameters. For parameters TOX, short and large VTH, RON and GAMMA the results are in high agreement to the PCM (process control monitoring) data. Only the standard deviation of the IDSAT parameter statistics shows a significant higher value. This will directly be reflected by more pessimistic models.

	TCAD data	**PCM data**
	Sigma	*Sigma*
TOX [nm]	0.09	0.08
VTH short [mV]	3.73	4.24
VTH large [mV]	4.2	4.5
IDSAT [uA/um]	9.0	3.62
RON [kOhm*um]	0.270	0.232
Gamma [$V^{1/2}$]	0.004	0.005

Table2: HV NMOS mean and sigma for TCAD vs. PCM data

The second benchmark criteria is summarized in Table 3 regarding correlation of the relevant parameters. Numbers in red take respect to the TCAD data, where blue indicates the measured behavior. It is shown that correlations between TOX, small and large VTH, IDSAT and RON are well reproduced. The Gamma correlation to TOX, VTH (short and large) is underestimated what again results in pessimistic models.

Finally it can be stated that the introduced strategy is feasible for virtual statistics generation.

5 GENERATION OF STATISTICAL SPICE MODELS WITH MONTE CARLO

Assuming the different parameters to be normally distributed, mean and standard deviation reflect a good picture on the performance of the one-dimensional parameters. In addition to get a complete picture of the full multivariate set of data the covariance matrix was extracted.

The correlation between different parameters can indicate unnecessary variables used for SPICE in best case and can show wrong implementations in worst case.

Common Monte Carlo SPICE [4] models do not use correlations within device parameters. The distributions in such models are normally allowed to vary independently to cover the whole range of possible values. Due to the lack of knowledge regarding the distinct dependency this strategy gives more certainty for the user as well as for the model provider. On the other hand side having additional correlations available their implementation could lead to more degree of freedom in critical designs due to higher confidence.

The Monte Carlo implementation is done as a linear combination of a certain SPICE parameter with its corresponding line neighbours in the covariance matrix.

These combinations can be written as

$$s_i = s_{i0} \cdot N(0,\sigma_i) + \sum \left(s_j \cdot C_{ij} \cdot N(0,\sigma_j) \cdot \underline{S} \right) \quad (3)$$

where si is the SPICE parameter under investigation, s_{i0} is its mean value, $N(0,\sigma_i)$ and $N(0, \sigma_j)$ are mean-free normal distributions, s_j are correlated parameters, C_{ij} are the correlation coefficients and $\underline{S}$ is a sensitivity matrix indicating the sensitivity of the underlying compact model equations.

The used compact model for this investigation was the HiSIM_HV [5] model developed by Hiroshima University. The varied SPICE parameters used for generating the statistical model and their process representatives are summarized in Table2.

Some of the process parameters are covered by more than one SPICE parameter (e.g. the on-resistance) with different weighting to this parameter. This explains the need for the sensitivity matrix indicated in eq.3. A uniform weighting of the correlation factors to all of the corresponding SPICE parameters would result in either an under- or overestimation of the dedicated Monte Carlo simulations.

Process variable	SPICE parameter
Oxide Thickness	TOX
Large threshold	VFBC
Small threshold	VFBC, NSUBP
Body factor	NSUBC
Saturation current	MUEPH1, VMAX
On-resistance	RD, RDVD, RD23
Leakage current	VFBC

Table4: Process parameter and corresponding SPICE parameters used for the Monte Carlo implementation

A visualisation of this implementation regarding the resulting effect on the different device parameters is shown in Figure 4. Here $d_{i,j}$ are indicating two different device parameters. These can be each combination of vth, idsat, ron, sleak. The $p_{i,j}$ are the k corresponding SPICE normal distributions with some sensitivity ($S_{i,j}$) to the device parameters. Implementation of the correlations Cpij to the SPICE distributions results in the overall correlation coefficients c_{ij}.

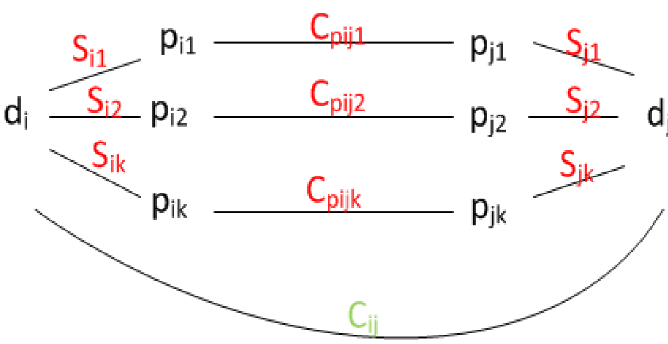

Figure 4 Overall correlation split into sub- correlations

For the benchmarking procedure, four device parameters have been chosen to be compared with the ones extracted from TCAD simulation. For comparison of the mean value and standard deviation these are the threshold voltage of the short device (vths), the on-resistance (ron) and the saturation current (idsat).

Figures 5 to 7 display the histograms of the corresponding parameters. The Monte Carlo results are produced by 1000 runs of the final SPICE implementation and compared to the 10000 data points derived by the surface response method. A pure visual comparison indicates high agreement of the mean value. Finally table 5 displays the results regarding mean and sigma value for both, virtual statistics results and SPICE Monte Carlo results.

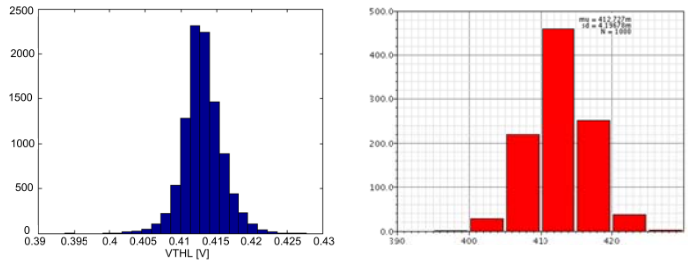

Figure 5 Histograms for VTHL HV NMOS, TCAD (blue, mean 412mV vs. SPICE Monte Carlo (red, mean 413mV)

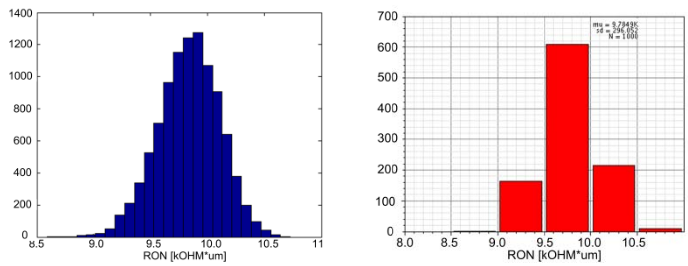

Figure 6 Histograms for RON HV NMOS, TCAD (blue, mean 9.83kOhm*um)vs. SPICE Monte Carlo (red, mean 9.78kOhm*um)

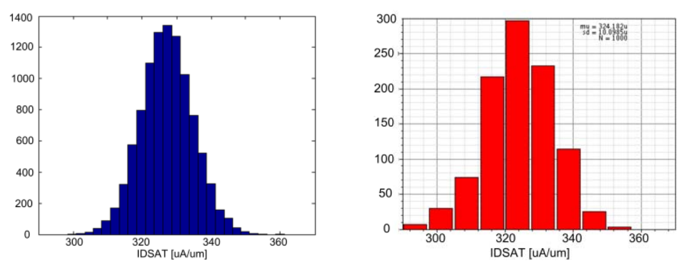

Figure 7 Histograms for IDSAT HV NMOS, TCAD (blue, mean 327 uA/um) vs. SPICE Monte Carlo (red, mean 324 uA/um)

	Target		MC Simulation	
	Mean	*Sigma*	*Mean*	*Sigma*
VTH short [mV]	412	3.73	413	4.19
IDSAT [uA/um]	327	9.0	324	10.0
RON [kOhm*um]	9.83	0.270	9.78	0.295

Table5: HV NMOS mean and sigma for TCAD vs. SPICE.

Regarding investigation of the correlation between two parameters we have chosen threshold voltage (vths) versus leakage current (sleak), threshold voltage (vths) versus on-resistance (ron) and saturation current (idsat) and finally correlation between on-resistance (ron) and saturation current (idsat). Figures 8 to 11 show the scatterplots from Monte Carlo results and Table 6 finally lists the correlation factors in comparison between virtual statistics and Monte Carlo results. For all compared parameters the results highly reflect the basic data.

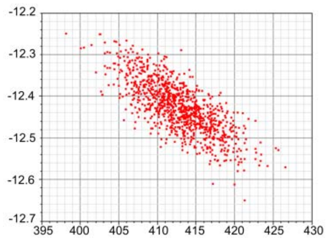

Figure 8 Scatterplot NMOS VTH (mV) vs. log(SLEAK)

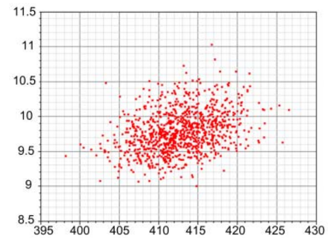

Figure 9 Scatterplot f. HV NMOS VTH (mV) vs. RON (kOhm*um)

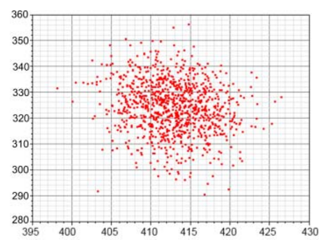

Figure 10 Scatterplot f. HV NMOS VTH (mV) vs. IDSAT (uA)

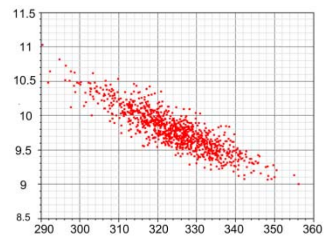

Figure 11 Scatterplot f. HV NMOS IDSAT (uA) vs. RON (kOhm*um)

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	IDSAT		RON		SLEAK	
	Target	*MC*	*Target*	*MC*	*Target*	*MC*
VTH short	-0.36	-0.29	0.40	0.33	-0.89	-0.82
IDSAT			-0.86	-0.87		

Table6: HV NMOS correlation for TCAD vs. SPICE

6 CONCLUSION

In this paper we present statistical SPICE models based on the PV-aware TCAD simulations. The process variation of n- channel LDMOS transistors has been investigated by means of simulations. Process and device simulations were performed by the SYNOPSYS tools and MINIMOS-NT, respectively and benchmarked versus electrical process monitoring parametrs from large silicon database. TCAD based statistical SPICE models were successfully implemented in this work, where errors between target (TCAD) and final simulation results (SPICE model) are in the few per cent range.

Acknowledgement

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References

[1] Synopsys Inc, “Sentaurus TCAD User Manuals”, Version C-2009.06, June 2009.
[2] MINIMOS-NT User's Guide, Institut für Mikroelektronik, Technische Universität Wien, Austria, 2004, http://www.iue.tuwien.ac.at/software/minimos-nt.
[3] R. Plasun, “Optimization of VLSI semiconductor devices, ”Dissertation, Technische Universität Wien, 1999, http://www.iue.tuwien.ac.at/phd/plasun.
[4] Users’ Manuals for BSIMPro+/RelXpert/UltraSim tools, http://www.cadence.com.
[5] Users’ Manuals for HISim_hv, http://www.cadence.com.

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