Optimization of Carbon Nanotube Thin-Film Transistor Fabrication

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ABSTRACT

Effects of various device dimensional parameters, electrode materials, and carbon nanotube (CNT)-electrode configuration on CNT thin-film transistor (TFT) performance (ON/OFF ratio and field effect mobility) were studied systematically using various semiconducting single-walled carbon nanotubes (SWCNTs), including Brewer Science's high-purity, surfactant-free semiconducting-enriched SWCNT dispersion. It was found that the ON/OFF ratio increases with the increase in channel length and starts to saturate beyond the 20-µm channel length. The ratio decreases with an increase in the channel width, but only at longer channel lengths. The ON/OFF ratio dropped while mobility increased drastically at lower CNT channel resistance. Palladium electrodes offered much better TFT performance than silver electrodes. Sandwiching CNTs between metal electrodes in electrode regions did not have an obvious advantage in device performance over a bottom-only electrode/CNT configuration.

Keywords: carbon nanotubes, thin-film transistor, pecolation threshold, ON/OFF ratio, field effect mobility

1 INTRODUCTION

Carbon nanotube–based thin-film transistors (CNT-TFTs) [1-4] have recently gained much interest from many researchers and customers for their potential in large-area electronic applications, including flexible electronics. Single-walled carbon nanotubes (SWCNTs) possess the ability to offer a high ON/OFF ratio, high field effect mobility [3, 5], high device switching speed [6-9], low operating range and threshold voltage, and low power consumption. However, these SWCNTs come as a mixture of metallic and semiconducting CNT species. The metallic CNTs can be a source of metallic transport and can short the electrodes [10], causing significant OFF-state current and making the devices less efficient. Therefore, unless the CNTs are entirely semiconducting, the CNT type density in the TFT channel plays a major role in TFT performance. To avoid metallic transport in CNT channels, the metallic CNT density in the CNT channel network should be less than the percolation threshold density [2].

Besides geometric and dimensional device factors, other factors significantly affect CNT-TFT performance. Those factors include, but are not limited to, the dielectric material, the electrode material [11], and the CNT-electrode configuration. A better dielectric material with optimized dielectric film thickness offers a better gating effect, while a better electrode material and CNT-electrode configuration offer ohmic contact and a lower Schottky barrier between the CNT channel and the metal electrodes [12]. In this paper, we discuss these practical aspects of fabricating CNT-TFTs as well as our efforts to optimize device dimensions and variables to fabricate high-performance CNT-TFTs.

2 EXPERIMENTAL

Semiconducting SWCNTs for this work were obtained from NanoIntegris (NI) and SouthWest NanoTechnologies (SWeNT). NI-99% SC semiconducting SWCNT material was obtained in surfactant solution form directly from the vendor. The SG-65 semiconducting SWCNTs from SWeNT were dispersed in sodium dodecyl benzenesulfonate (SDBS) using a microfluidizer and then were centrifuged at 51,000 g for 30 minutes to remove the non-dispersed CNT chunks. Brewer Science's high-purity, surfactant-free semiconducting-enriched SWCNT dispersion was also used. All TFTs that were used in this work were prepared on silicon wafers, with 1000 Å of SiO_2 that was used as a TFT dielectric layer, and TFTs were universally back-gated. Photolithographically patterned palladium was used as source and drain electrodes of the transistors. The CNT channels of the TFTs were printed using Optomec's Aerosol Jet® printer. After printing, surfactant from the surfactant-based CNT channel was removed by dipping the devices in methanol for 30 seconds, rinsing with deionized water, and drying with compressed air. A schematic of a CNT-TFT is shown in Figure 1.

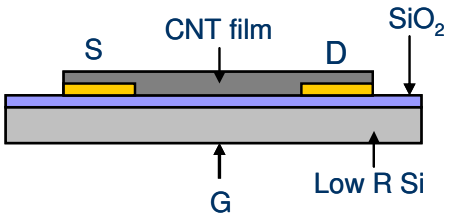

Fig 1: A schematic of a CNT-TFT.

To investigate the effect of sandwiching the CNT channel in the source and drain electrode regions, a layer of nano-Ag was printed on top of CNTs in the source and drain regions. A layer of aluminum oxide (Al_2O_3, 9 wt% in water) was printed on top of CNT channels of bottom-gated TFTs in order to compare the TFT performance of the same TFTs made with SiO_2 or Al_2O_3 dielectrics. Nano-Ag ink was printed on top of Al_2O_3 to use as a top-gated electrode. The printed Ag electrode was cured at 150°C for 30 minutes.

For each study, 10 TFTs were prepared and tested, and data from all working TFTs are presented. All CNT channel resistances were measured using a digital multimeter and a probe station, while all other TFT electrical characterizations were done using a Keithley SCS-4200 semiconductor analyzer. The ON/OFF ratios of the TFTs were determined from transfer curves (I_{DS}-I_G curve), and mobility was calculated from the transfer curves by using the following equation:

$$\mu_{FE} = \frac{l}{w}\frac{dI_{DS}}{dV_G}\frac{d}{\varepsilon}\frac{1}{V_{DS}}$$

where l is CNT channel length, w is channel width, d is dielectric film thickness, ε is dielectric constant, V_{DS} is bias voltage, and dI_{DS}/dV_G is the slope of the transfer curve in the linear region.

3 RESULTS AND DISCUSSION

Figure 2 shows a typical current-voltage (IV) curve and a transfer curve of a CNT-TFT that was fabricated by using Brewer Science's (BSI's) purified, surfactant-free, semiconducting-enriched SWCNT dispersion. Using a surfactant-free CNT material eliminates the need for surfactant removal and improves the device-to-device consistency. The IV curve shows good semiconducting behavior. As shown in the transfer curve in Figure 2(b), BSI's surfactant-free semiconducting SWCNT material provided a consistent ON/OFF ratio of ~ 10^3, with field effect mobility of ~ 0.5 $cm^2/V{\cdot}s$ in our TFT device platform that used 1000 Å of SiO_2 as the dielectric material. We expect that the device performance of this CNT material can improve significantly with further optimization of TFT fabrication and with the use of high-dielectric-constant materials.

The effect of CNT channel length on the performance of TFTs fabricated using NI-99% SC semiconducting SWCNTs and with two different channel widths is shown in Figure 3. As seen in the figures, the ON/OFF ratio continuously increases with the increase in channel length and begins to saturate at channel lengths larger than 20 µm. Also, the ON/OFF ratios for the 75-µm channel width are 1-2 orders of magnitude higher than those for the 300-µm channel width for the respective channel lengths.

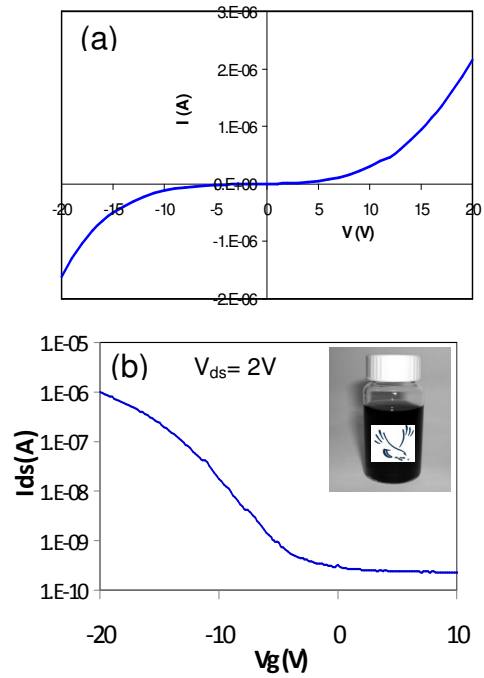

Figure 2: (a) IV curve, and (b) transfer characteristics of a CNT-TFT that used BSI's surfactant-free, semiconducting-enriched SWCNT dispersion. Inset: BSI's SWCNT dispersion.

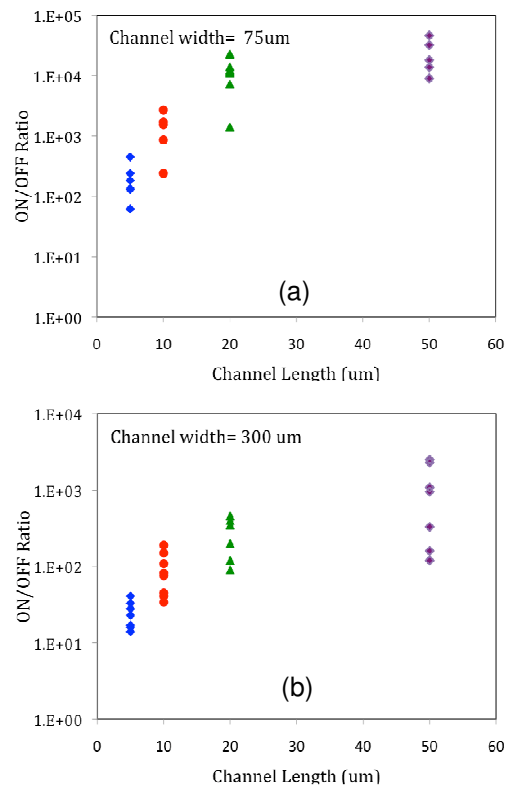

Figure 3: ON/OFF ratio vs. CNT channel length graphs of TFTs with channel widths of (a) 75 µm and (b) 300 µm.

Figure 4 shows the effect of CNT channel width on device performance of TFTs with channel lengths of 5 µm and 50 µm. For the 5-µm channel length, the ON/OFF ratio remained the same and low for the channel width range of 100-300 µm. It is interesting to see that the ON/OFF ratio increased by 1 order of magnitude when the channel width was reduced to 75 µm, suggesting that 75 µm is the threshold channel width for TFTs with 5-µm channel length. However, a clear, inversely proportional dependence of ON/OFF ratio on channel width is seen for the 50-µm channel length. In addition, ON/OFF ratios for the 50-µm channel length are much higher than those for the 5-µm channel length at respective channel widths. With a channel length and width of 50 µm and 75 µm, respectively, the experimental semiconducting material (NI-99% SC) offered a consistent ON/OFF ratio of > 10^4, with a mobility of > 5 $cm^2/V{\cdot}s$.

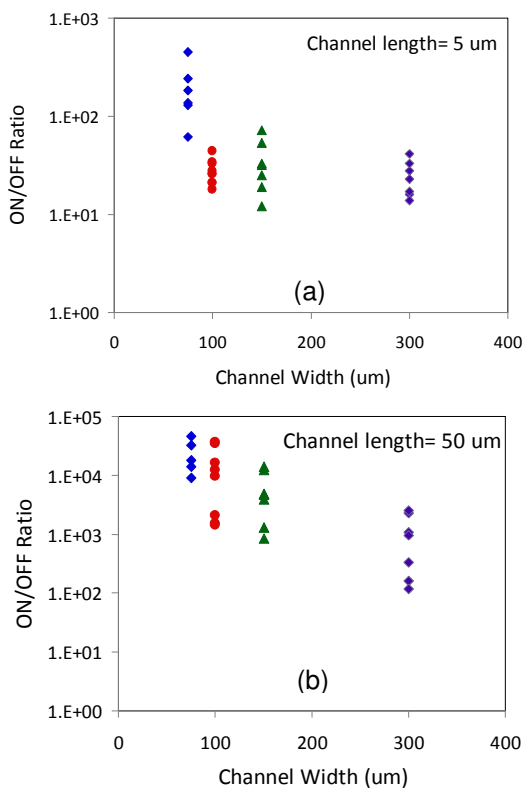

Figure 4: ON/OFF ratio vs. CNT channel width graphs of TFTs with channel lengths of (a) 5 µm and (b) 50 µm.

TFTs with the same channel length and width (50 µm and 150 µm, respectively) but with different channel resistance were fabricated using the same NI-99% SC semiconducting SWCNT material in order to see the effect of channel resistance on TFT performance. Results are summarized in Table 1. The ON/OFF ratio increased but the mobility decreased with increase in CNT channel resistance.

CNT Channel Resistance (kΩ)	ON/OFF Ratio	Mobility ($cm^2/V{\cdot}s$)
80	800	17.2
130	1300	14.6
175	4700	10.7
260	12000	6.2

Table 1: Dependence of CNT-TFT ON/OFF ratio and field effect mobility on CNT channel resistance. Channel length = 50 µm, and channel width = 150 µm.

The same effect of channel resistance on TFT performance was observed with TFTs that used the SWeNT semiconducting SWCNT material as the active channel material. However, the material had much lower mobility than the NI-99% SC semiconducting material.

From our studies on channel length, channel width, and resistance, we found that all three factors affect TFT performance in the same way, i.e., transport through metallic SWCNTs below percolation threshold values. Smaller channel length increases the probability of charge transport through metallic SWCNTs by bridging the source-drain gap with individual metallic nanotubes or bundles that contain metallic nanotubes. On the other hand, wider channel width or a thicker channel (i.e., lower channel resistance) can provide multiple metallic pathways for charge to be transported from source to drain. These types of metallic transport cannot be effectively controlled by gate voltage and result in high current, even in the OFF state, giving lower device ON/OFF ratios. Also, due to greater charge transport through metallic tubes, the mobility for shorter, wider, or thicker channels becomes higher.

In order to see the effect of electrode material on TFT performance, TFTs with channel length of 25 µm and channel width of 100 µm were made with BSI's surfactant-free semiconducting dispersion using palladium and silver electrodes. The ON/OFF ratio results are shown in Figure 5.

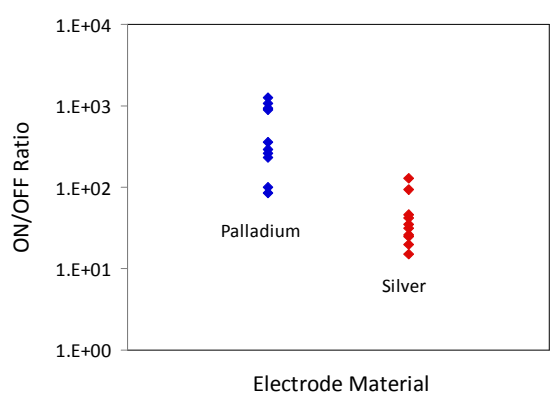

Figure 5: Comparison of ON/OFF ratios of TFTs made with palladium and silver electrodes.

Clearly, palladium electrodes provided much higher ON/OFF ratios than silver electrodes. In addition, palladium electrodes provided better mobility (~ 0.45 $cm^2/V{\cdot}s$), compared to silver electrodes (~ 0.04 $cm^2/V{\cdot}s$). The better performance of TFTs made with palladium is attributed to the fact that its work function (5.2 eV) matches that of CNTs (5.1 eV) better than that of silver (~ 4.7 eV), which reduces the contact resistance and Shottky barrier [12] in the CNT-electrode interface.

We did not observe an obvious TFT performance advantage of sandwiching CNTs between a bottom palladium electrode and a top printed silver electrode over placing CNTs on a palladium electrode only. This result may be due to the dominance of the palladium-CNT interface because it provides lower contact resistance and Shottky barrier than the CNT-silver interface; therefore, most transport takes place through the palladium-CNT interface. However, we saw some drop in current level after printing the top silver layer, which may be caused by a morphology change in the CNT film due to heat-induced stress from the curing process (150°C for 30 minutes) used to make the printed silver electrode.

Our effort to compare the performance of the same TFTs using a bottom SiO_2 dielectric layer and a top printed Al_2O_3 dielectric layer instead was not successful. We suspect that pinholes may have been present on the Al_2O_3 dielectric layer and may have caused those shortings. This effort continues. Two other dielectric materials are also under study, and the results on the efffect of these dieectric materials on TFT device performance will be published in the future.

SUMMARY

In CNT-TFTs, the ON/OFF ratios of TFTs were found to increase with an increase in channel length, but decreased with the channel width when above the threshold channel length. ON/OFF ratio dropped while mobility increased drastically with a decrease in CNT channel resistance. Palladium performed better than silver as a TFT electrode material. Sandwiching of CNTs between metal layers in source and drain electrodes did not have any advantage in device performance over a bottom-only electrode layer configuration.

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