Nano-contacts and Nano-interconnects

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ABSTRACT

Nanotechnology is reaching the market today in electrical products and systems. Performance of nano-enabled components and products depends partially on the nanoscale contact and interconnect quality. Superior characteristics of CNTs, nanowires, and graphene have been reported, but to take advantage of these attributes, one must insure that an excellent nanoscale electrical contact is formed. Otherwise, high mobility, electron velocity, and conductivity; and other features, may never enhance a component/product. The semiconductor industry hopes that graphene/nanotube interconnects will extend Moore's Law for additional 'technology nodes.' This paper will discuss pros and cons of various nanotube and graphene interconnect approaches. Major technological issues remain unsolved, and restrict incorporation of nanoscale contacts and interconnects into products. Requirements, fabrication, characterization, performance, reliability, and market expectations will be addressed.

Keywords: nanoscale, contact, interconnect, graphene, carbon nanotube

1 INTRODUCTION

SWCNTs, MWCNTs, nanowires, carbon nanofibers (CNFs), and graphene have all been used to conduct electricity in various devices [1-3]. Thermal and electrical conductivity have been cited by researchers and product designers as a feature of nanotechnology that might enhance the speed and frequency performance of devices. Typical products that expect to utilize these nanostructures include, in part: semiconductor devices and integrated circuits; photovoltaic panels; batteries; flexible electronics and displays; solid-state lighting; organic LEDs; and printable electronics. One feature that most of these applications require is an excellent nano-structure to bulk-conductor contact that allows for low-resistance current flow. However, nanotubes, nanowires, nanofibers, and graphene are difficult to make contact to, and those barriers must be overcome before manufacturing of nano-enabled electrical products will become mainstream.

Issue topics and questions that arise can be broken into groups:

1. Type and configuration (what materials are being contacted, size, number of contacts);
2. Requirements (voltage, current, frequency, transparency, mechanical and chemical stability, conductivity);
3. Fabrication methods and controls (process used, requirements on nanomaterials, control processes, surface treatments, post-fabrication processes, high-volume manufacturing capability);
4. Characterization techniques (quantifying contacts, I-V measurements, ohmic behavior, Schottky behavior, frequency behavior);
5. Functionality and performance of nanoscale contacts (were requirements met, what efforts are needed to improve the characteristics);
6. Reliability (are reliability requirements known, has reliability been measured, accelerated life testing);
7. Market expectations (when will nanoscale contacts or interconnects be ready for mass production, are plans in place for future generations).

A thorough review of existing publications related to nanoscale contacts was conducted in this research. Particular attention was paid to nanotubes /nanowires/nanofibers and graphene nanoscale contacts and interconnects primarily as these have had the greatest expectations and investment. Individual contacts as well as the use of these materials in via and lateral interconnects were studied. Graphene has been cited as a potential replacement for copper in semiconductor interconnects, as performance of copper degrades in technology nodes around 20 nm.

It will be shown in this paper that the *results from nanoscale contacts and interconnects are falling far short of the requirements and expectations*. Additionally, there appear to be difficulties that may be impossible to overcome, and this informs the conclusion that without significant breakthroughs, nanoscale contacts and interconnect may not enable devices, components, products, and systems as many in the research and product development community wish.

2 REVIEW OF MOST COMMON NANOSCALE CONTACTS AND INTERCONNECTS

In this section we will explore the state-of-the-art for: 2.1 nanotubes and nanofibers; 2.2 via interconnects using

CNTs or CNFs; 2.3 Surface (lateral) interconnects using CNTs and CNFs; and 2.4 Graphene interconnects.

2.1 Nanotubes and Nanofibers

SWCNTs have room-temperature, mean-free paths (MFP) of 1000 nm, compared to 40 nm for Cu. Expected current densities of 10^{12} A/cm^2 have been cited. However, forming a low-resistance nanoscale contact to an isolated nm-sized SWCNT is challenging. First, when fabricating SWCNTs, one cannot deterministically produce either a metallic or semiconducting nanotube bundle during growth. If one wishes to use MWCNTs, unfortunately the MFP is a few nanometers. This makes MWCNTs virtually unusable in a semiconductor device environment. For semiconductor nanowires like Si, an oxide forms on the surface, and it must be removed before attaching a bulk conductor like Ti/Au. Also, the nickel-silicide process from typical semiconductor devices made today will not port well to Si-nanowires as they must have a (111) orientation to produce low-resistance ohmic contacts. Virtually every effect that can happen at the surface of a semiconductor will be made more impactful as one scales to the nanometer size. These surface issues appear unsurmountable at this time.

Researchers have done most characterization on individual contacts, and not strings of millions of contacts as required in semiconductor technology. A manufacturing approach for characterization must be found before nanoscale contacts emerge. Researchers also still contend with too much process variation to do direct comparisons of models and experiment. Process control does not yet exist.

During characterization, virtually all researchers have cited using annealing techniques to heat the contact area, and to break down the oxide in the interface that leads to formation of Schottky contacts rather than ohmic contacts. After an appropriate 'thermal' process, an ohmic contact can be formed, but these techniques cannot be used in manufacturing, and really bring into question whether clean (oxide-free), ohmic contacts can be fabricated directly, and without annealing processes being employed. Another common observance of researchers is a lack of correlation of resistance and capacitance to diameter and length of CNT and CNF devices. This again points to the lack of process control in the use of nano-structures.

2.2 Via Interconnects using CNTs and CNFs

Copper vias are having issues with electromigration, resistance increases, and limited current density as the technology nodes continue to shrink. CNTs and CNFs exhibit robust thermal and mechanical properties that should make them ideal for on-chip interconnect. Researchers have stated that SWCNTs have a theoretical current density 1000 times greater than Cu. Arrays of SWCNTs might also provide the lowest resistance in an interconnect, outperforming Cu by 10-100 times for wires of 30-nm diameter. Unfortunately, these estimates neglect the real issue that 100% conducting SWCNT arrays are not possible to fabricate today. Another major problem has been that experimental results do not reach theoretical predictions. In fact, reported MWCNT results have two orders of magnitude less current density and two orders of magnitude higher resistance than equivalently sized Cu wires. Also, 900ºC annealing was required to deal with interfacial oxides between the bulk conductors and the MWCNTs. The contacts started as Schottky barriers before annealing. Part of the explanation of poor experimental performance compared to theoretical predictions has to do with the difficulty of making electrical contact to every shell of the MWCNT. This is a grand challenge for this type of contact, and no researcher has suggested a solution. At this time, there appears to be no real solution for making vias with either SWCNTs or MWCNTs that will rival the performance of Cu in integrated circuits today. And this also neglects the huge fabrication challenge for such processes that are not even close to production ready.

2.3 Surface (Lateral) Interconnects using CNTs and CNFs

Some research efforts have predicted that a CNT FET might outperform the speed of a traditional MOSFET by 8 times. Unfortunately, the researchers also assume that high-level integration and process-related challenges are met. No research group has proposed how millions of transistors can be integrated on an IC that will have perpendicular current flow, excellent contact resistance, and reliability of 100%. These are requirements of transistors in an integrated circuit today.

Here is a summary of the major challenges to using CNTs or CNFs as local interconnect in an IC:

1. Aligning nanotubes in orthogonal directions;
2. Making ohmic contacts to all nanotubes;
3. Producing only metallic nanotubes for interconnects;
4. Mass-producing contacts;
5. Making connections to vias on ICs; and
6. Blending all new process technology into the fabrication process for CMOS.

How would one insure ohmic contacts between nanotubes? How would lengths and orientation be controlled? How would the nanotubes be made perpendicular to each other? And the largest question of all: How would one do this with high yield for millions of interconnects on every chip manufactured?

Some researchers have also looked at the use of arrays of CNTs for interconnect. The problem arising is that for a voltage-driven circuit, the interconnect resistance, and not the current density, determines the switching speed. For SWCNTs, the clear winner is Cu. So, even though CNTs have high current densities and greater reliability, the intrinsic resistance limits their performance in voltage-driven circuits. Some authors have shown superior

performance from CNT interconnect in circuits as compared to CMOS circuits, but the work used transistors 100 times wider than typical drivers. This is an unrealistic comparison to actual circuits that are designed with minimum size to achieve the frequency performance desired. Having transistor 100 times bigger than they need to be would make it impossible to make dense ICs.

2.4 Graphene Interconnects

Graphene is a single-layer of carbon atoms in a honeycomb-shaped lattice, discovered just recently in 2004. It has garnered increased attention and investment, particularly by the semiconductor industry that is searching for the replacement of Cu interconnect for future technology nodes. Some of the attributes of graphene include: tensile modulus of ~100 GPa; breaking strength 200 times that of steel; Young's modulus of 0.5 TPa; spring constant of ~5 N/m; mean free path of 1 μm; optical transparency; high thermal conductivity of ~$5x10^3$ W/m-K; high room-temperature electron mobility of 10^5 cm^2/V-sec; and current carrying capacity of giant nanoribbons (GNRs) of ~10^{10} A/cm^2.

The question is whether these attributes can be realized in an integrated circuit or other application. Demonstrations have already shown that transparent conductors with 10 times the conductivity of ITO are feasible. Sheets of flexible graphene have been fabricated nearly 1-m wide, and they are cheaper to fabricate than ITO conductors that need vacuum chambers to deposit materials on rigid glass substrates.

One good piece of news related to graphene is that it is relatively easy to make low-resistance ohmic contacts between graphene and bulk metals like Ti/Au, Al/Au, Ni/Au, Cu/Au, Pd/Au, and Pt/Au. However, the ability to use graphene on an IC requires patterning of graphene layers into GNRs, positioning those GNRs perpendicular to each other, and preventing any surface effects either above or below the graphene layer from degrading its characteristics. Surface treatments, oxides, and metal contacts all seem to impact graphene conductivity performance. Other items such as layer morphology, background doping, film stress, and defectivity levels will impact graphene performance in an IC.

GNRs introduce numerous issues that must be surmounted. The edges of the GNR could be either zigzag or armchair shaped, and the width of the GNR will determine its metallic character, with a very slight change in width determining whether the GNR is metallic or semiconducting. For instance, an 11-atom wide, armchair GNR would be semi-metallic, whereas a 7-atom wide, armchair GNR would be semiconducting. At the present time, there is no lithography control that would allow one to fabricate a GNR with precise control at the atomic scale as needed. Also, no researcher has suggested a way to place GNRs with controlled width and edge-shape on an IC perpendicular to each other.

Experimental results for graphene, just as reported above for CNTs, CNFs, vias, and lateral interconnects, have not achieved the theoretical performance levels desired. In fact, graphene has been reportedly about 15-40 times more resistive than copper conductors of similar dimensions. It may be that the edge effects from either zigzag or armchair edges may be reducing the mean free path beyond what theory would predict for an infinitely wide graphene sheet.

Another issue also exists in that single graphene layers will not provide the necessary current capacity, even though the mean-free-path and conductivity are very high. Researchers have tried stacking graphene sheets to improve current capacity and resistance, but multi-layer graphene has a much lower conductivity per layer due to inter-sheet electron hopping. Edge-width control and edge smoothness are crucial parameters for single-layer graphene, and the problem gets far more complicated in multi-layer graphene. Research has not demonstrated the single-atom width control necessary for multi-layer graphene to date. Research has demonstrated that both intercalation doping and high edge-specularity (smoothness) must be controlled for GNRs to be better than Cu interconnect. This appears nearly impossible for the near future.

To summarize the present status of GNRs, the following barriers will need to be addressed before graphene will become part of mainstream IC fabrication:

1. Resistance changes from isolated GNRs to deposited-on-dielectric GNRs;
2. Different dielectric affects on GNR electrical characterisitics;
3. What bonding and stability exists with underlying substrates on which GNRs are placed;
4. Which power requirements are needed for high-performance interconnect; and
5. How do packaging and thermal constraints affect GNR interconnects.

3 SUMMARY

There are significant challenges ahead for the manufacture of nanoscale contacts and nanoscale interconnects. It is also believed that without a firm understanding of the science, methods, and manufacturing techniques related to nanoscale contacts, useful electronic devices employing nanomaterials and nanoscale devices may be difficult to achieve. Indeed, there appears no feasible way to utilize either SWCNTs, MWCNTs, CNFs, or nanowires in any real via or lateral interconnect at this time. These technologies face a list of issues that would require significant additional research investment and may still not reach the desired results.

Graphene appears to be the only nanoscale material that might have a chance of helping the semiconductor community with its future technology-node barriers. However, even with this technology, the number of issues makes it difficult to see a successful future for graphene. However, the semiconductor industry has vast resources,

and a strong desire to extend Moore's Law for many more technology generations, and this support may be able to knock down any barriers in its way.

The researchers in the graphene area would be advised to combine their research efforts in a coordinated manner to bring the technology forward quickly, if there is any hope that graphene interconnect might replace Cu interconnect in ICs.

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