

# A NOVEL ELECTRICAL CONTACTING TECHNOLOGY TO GRAPHENE

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## ABSTRACT

The paper reports on a Ni based electrical contacting technology to graphene that is simple and effective and can be adopted by laboratories lacking high grade infrastructure. The graphene surface was masked, activated and then chemical plating was employed to produce the desired contact. The initial results indicate good adhesion of the contact with a contact resistance of 17 $\Omega$ .

**Keywords:** electroless plating, graphene contacts, contact resistance .

## 1 INTRODUCTION

Graphene being an atomic sheet of carbon is a non-metallic film and a zero-bandgap semiconductor in its pristine form [1]. The layers of atomic carbon present a novel electronic structure, where the conduction and valence bands meet at the Dirac point. These special characteristics enable the electrical transport to be tuned between hole or electron conduction by shifting the Fermi level with an applied electrical field. Thus, graphene shows not only potential applications in fabricating high speed electronic devices but also novel microelectromechanical systems (MEMS) and sensors. In order to fully maximise the unique electronic properties of graphene, especially in achieving extreme speeds in graphene based devices, one must address a potential limiting factor, one being the construction of graphene/metal electrical contacts. Work of producing state-of-the-art epitaxial graphene field effect transistors on 6H-SiC substrates [2,3] demonstrate the need for such developments. In this work Moon et al obtained ohmic contacts by a Ti/Pt/Au non alloyed metal stack with a resistivity of 10<sup>-6</sup>  $\Omega\text{cm}^2$ .

Understanding the physical principles underlying this contact interface is an important first step in optimising the contact. Malec et al [4] investigated Au-graphene contact properties. Graphene from mechanically exfoliated graphite was utilised with gold deposition onto the samples undertaken prior to any lithography to maintain a contamination free surface. The work demonstrated that direct contact of Au onto single layer graphene cause significant p-doping in the graphene. Another problem with the direct use of gold is the poor adhesion onto the

surface. The use of an adhesion layer to circumvent this problem has been shown to create a large contact resistance at room temperature. To try and help understand the issues around contacting to graphene, Berdebes et al have modelled this graphene metal interface [5] for graphene transistors. Their model explains the gate-dependent resistance asymmetry found in experimental work and is attributed to an interfacial layer between the graphene and metal contact. Further modelling work by Parrish et al also highlight the importance of reducing contact resistance [6].

To improve on performance, a range of metal options are reported. Watanabe et al investigated the contact resistance onto graphene for a variety of metals (Ti, Ag, Co, Cr, Fe, Ni and Pb) [7]. Micromechanical cleavage of Kish graphite was used to produce the graphene and then e-beam lithography and reactive ion etching were used to define transmission line geometries of the contact metal on the graphene surface. From a series of resistance measurements at varying transmission line distances, the contact resistance was inferred. The work indicated contact resistances varying from 10<sup>2</sup>-10<sup>3</sup>  $\Omega\mu\text{m}$ . Results highlighted the importance of a small grain size in the contact metal which maximises contact area and helps reduce contact resistance. Huang et al also investigated a variety of metal stacks in work on graphene field effect transistors [8]. Graphene sheets grown on a Ni film were transferred via the PMMA method onto a SiO<sub>2</sub>/doped Si substrate. E-beam lithography and a lift-off procedure was used to pattern the metal contacts. The results showed Ti/Au, Ni/Au and Ti/Pd/Au stacks having contact resistances of 7500  $\Omega\mu\text{m}$ , 2100  $\Omega\mu\text{m}$  and 750  $\Omega\mu\text{m}$  respectively.

Geometric considerations may be used to improve contact performance. Franklin et al demonstrated a novel geometric approach to reducing the contact resistance problem. In their work [9], contact to the graphene layer was made from both above and below the graphene layer. Both single layer graphene, grown by chemical vapour deposition on Cu foils and then transferred, and bilayer graphene, from mechanical exfoliation from graphite flakes, were used in the study. A minimum of 40% decrease in contact resistance was demonstrated in the work with the bilayer case showing the more pronounced improvement. Matsuda et al investigated the advantages of applying end contacts to graphene structures in comparison to side contacts [10]. The approach used first principle quantum mechanical density functions to

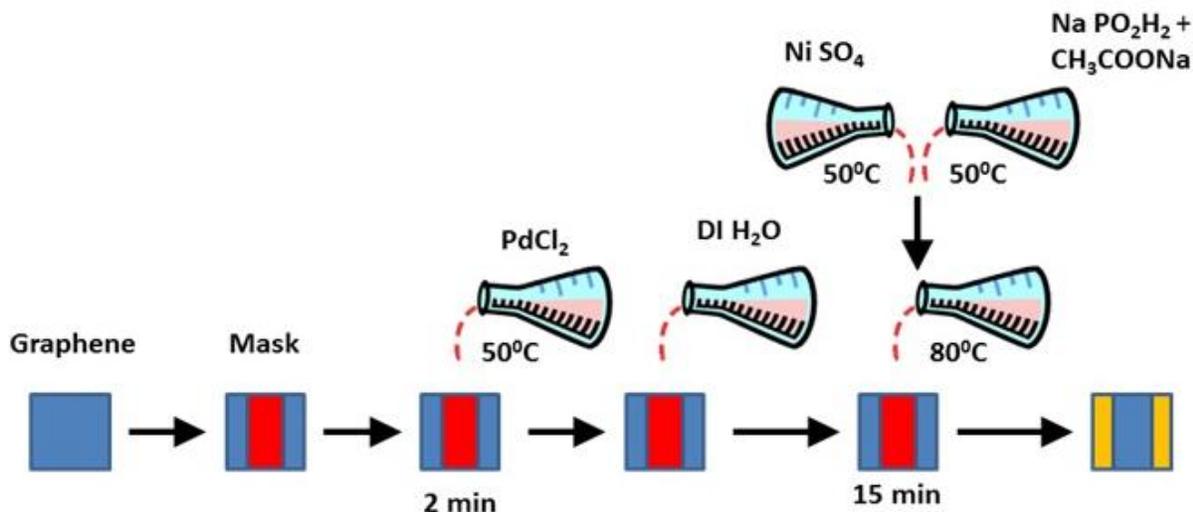


Figure 1: A schematic of the process flow to create the nickel contacts on to graphene substrates.

calculate the contact resistance for Ti, Pd, Pt, Cu and Au. Their side contact calculations are in good agreement with experimental work and results for the end contact configuration infer over an order of magnitude improvement. A practical configuration for such end contacts is proposed.

Processing conditions have also been investigated to maximise performance. Hsu et al investigated the graphene interface quality on RF device performance [11]. Processing of the CVD produced graphene surface incorporated an Al sacrificial layer to reduce surface roughness. Their results showed an improvement from  $2\text{K}\Omega\mu\text{m}$  to  $0.2\text{-}0.5\mu\text{mK}\Omega$  in contact resistance. Robinson et al looked at improving the metal graphene contact resistance through careful consideration of process conditions [12]. The work examined contact configurations of Al/Au, Ti/Au, Ni/Au, Cu/Au, Pt/Au and Pd/Au onto exptial graphene produced via sublimation of Si from 6H-SiC. Results demonstrated an improvement in resistance of over 3 orders of magnitude by the inclusion of an oxygen plasma etch and heat treatment of the sample.

Other factors potentially affecting contact performance have also been investigated. Xia et al investigated the temperature dependence of resistance on a Pd-graphene junction [13]. Pd/Au contacts were made on exfoliated single layer graphene flakes and source-drain resistance measurements taken over a temperature range of 6K to 300K. Results at 6K showed near ballistic transport in the graphene and contact resistance of  $110\pm 20\Omega\mu\text{m}$ . At room temperature, this increased significantly due to diffusive transport. Russo et al investigated the contact resistance between Ti/Au and varying numbers of graphene layers (single, bi and tri-layer) [14]. Graphene flakes from exfoliated graphite was used with e-beam lithogprahy and a lift-off process used to fabricate the contacts. Two and four point probe measurements were then used to extract the contact resistance. Results show that the contact

resistance is dominated by a gate independent component of  $800\pm 200\Omega\mu\text{m}$  which is insensitive to layer thickness. Venugopal et al also investigated the dependence of layer number on contact resistance using Ni electrodes [15]. Mechancial exfoliation of natural graphite was used to produce the graphene flakes with two-point probe structures being lithographically patterned onto the graphene flakes. Results showed contact resistivity of the order of  $1\text{K}\Omega\mu\text{m}^2$ , this being independent of layer number, and the work concluded that only the top layer or two impact on the contact resistance.

In previous work by Ghosh, an electroless technique for creating electrical contacts for II–VI semiconducting devices was reported [16]. This work looked at Ni electroless plating in combination with other materials for example Cu, Au, Mo, W, Co to engineer the work function and determine performance characteristics for such combinations. The work reported here is an extension of this and discusses one potential electrical contacting technology being developed that is highly suitable for graphene substrates.

## 2 NICKEL ELECTROLESS PLATING ON GRAPHENE SUBSTRATES

In this study, epitaxial produced graphene films, transferred onto clean Si/SiO<sub>2</sub> substrates were purchased from Graphene Laboratories. To achieve the placement of electrical contacts onto graphene, a method of electroless nickel plating was performed following the protocol previously described in [16]. Prior to the plating process, the graphene substrate was masked using Kapton tape to allow the placement of nickel contacts in specific locations at fixed distances apart. The graphene was first activated by dipping the substrate into a palladium chloride activation solution that improves the adhesion of the nickel. Secondly, the activated graphene was placed in a

heated nickel plating solution to start the growth of the contacts on graphene. The plating solution composed of nickel sulphate as the source of nickel and sodium hypophosphite as a reducing agent alongside a stabiliser and pH buffer. After sufficient mixing, the chemical plating solution was heated to 80°C and maintained at constant temperature for the entire plating process to ensure uniform plating. After 15 minutes the graphene substrate was removed from the plating solution and a thin shiny layer of nickel was observed, the samples were left to dry for 3 hours. After the samples had dried the Kapton tape mask was removed to leave the specifically placed nickel contacts on the graphene substrate with exposed graphene between. A schematic of the process flow is shown in figure 1.

### 3 QUALITY OF THE GRAPHENE FILM AFTER THE PLATING PROCESS

Once the electroless plating process was complete, optical microscopy and scanning electron microscopy were utilised to assess the quality of the graphene/nickel contacts and the non-plated graphene film. As shown in figure 2, the graphene film appeared clean and undamaged from the process.

Graphene has three main characteristic Raman peaks [17], denoted as the D peak ( $1320\text{ cm}^{-1}$ ), the G peak ( $1549\text{ cm}^{-1}$ ) and the 2D peak ( $2650\text{ cm}^{-1}$ ). The intensity and wavenumber of these peaks give an indication of the characteristics of the graphene layer: the D peak intensity gives an indication of the degree of defects in the graphene basal plane carbon-carbon bonds, the G peak relative intensity gives an indication of the stacked graphene layers present, the 2D peak wavenumber and width indicates the number of graphene layers present. Raman spectroscopy was utilized to assess the quality of the non-plated graphene film. In this study, Raman spectroscopy was performed immediately after the graphene had cooled from the electroless plating process using a FHR1000 Horiba Jobin Yvon Raman system with 633nm probe beam.

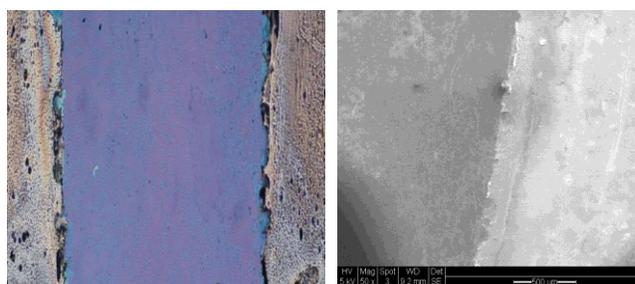


Figure 2: Optical microscopy (left) and SEM imaging (right) were used to visually assess the quality of the surface after the plating process.

The Raman spectra obtained for the non-plated graphene regions is shown in figure 3. The spectra of the processed samples showed comparable relative intensities to untreated samples with the defect peak remaining relatively small compared to the G peak. This indicated that the graphene film was not damaged by the plating process. The characteristics of the G peak and 2D peak indicate that the graphene film was of monolayer thickness, indicating that graphene layers had not become crumpled and overlapped during the plating.

### 4 GRAPHENE/NICKEL CONTACT ELECTRICAL MEASUREMENTS

The graphene/nickel contacts were placed at varying distances on the graphene films between different samples and electrical resistance measurements taken. To perform the electrical measurements, a fine tip conducting probe needle, connected to a Fluke multimeter, was placed on the nickel contacts and the electrical resistance values measured. The graphene/nickel contact resistance was calculated by plotting the measured resistance values against the distance between the contacts. The resistance data is shown in figure 4, with the intercept indicating twice the contact resistance. Measurements were performed on 7 samples indicating a contact resistance of  $17\pm 3\Omega$ .

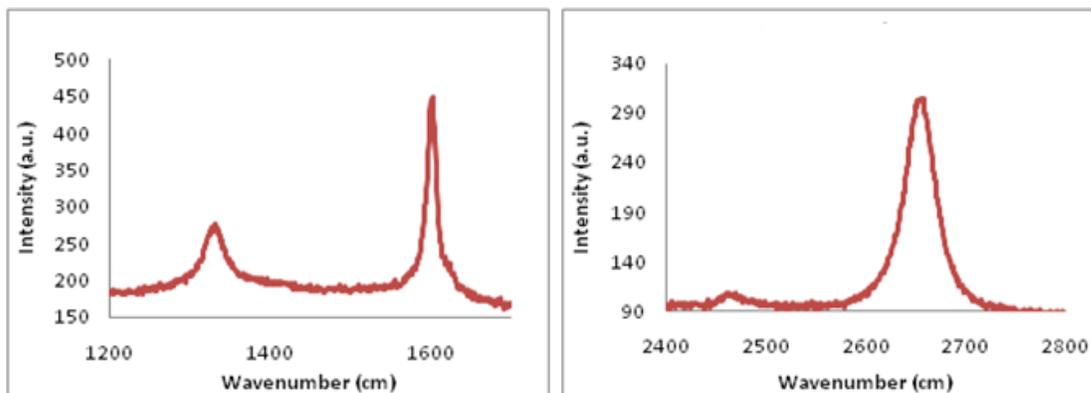


Figure 3: The Raman spectra of the sample indicated that single layer graphene was present after the plating process with no apparent increase in defect density of the layer.

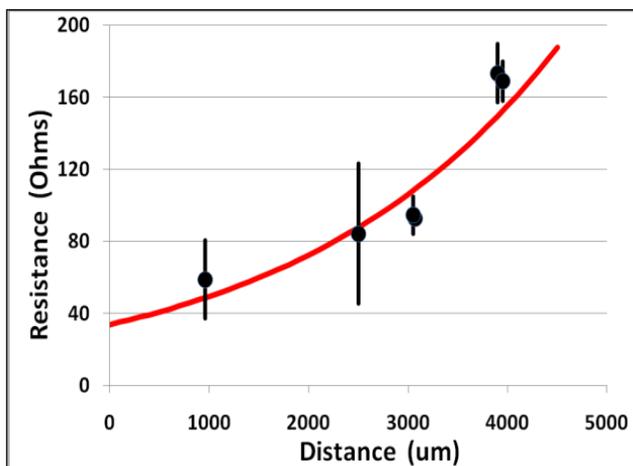


Figure 4: Electrical resistance measurements between nickel contacts on the graphene surface. The intercept indicates twice the contact resistance.

## CONCLUSION

The facile placement of nickel contacts onto graphene films using electroless plating was demonstrated. The optical imaging, SEM and Raman spectra all indicated that the plating process deposited the nickel contacts effectively whilst maintaining the integrity of the graphene film. The contact resistance between the graphene/nickel interface was calculated by performing empirical electrical resistance measurements with varying contact distance that indicated a contact of low resistance with good adhesion. Future work will involve the optimisation of the electroless plating chemistry to improve on the currently demonstrated contact resistance. This work is aimed at allowing the electrical properties of graphene to be optimally exploited for real world commercial applications.

## 5 ACKNOWLEDGMENT

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## REFERENCES

- [1] K. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva and A. A. Firsov, *Science*, 306, 666-669, 2004.
- [2] S. Moon, D. Curtis, M. Hu, D. Wong, C. McGuire, P. M. Campbell, G. G. Jernigan, J. L. Tedesco, B. Vanmil, R. M. Ward, C. Eddy and D. K. Gaskill, *IEEE Electron Device Letters*, 30, 650-652, 2009.
- [3] S. Moon, D. Curtis, S. Bui, M. Hu, D. K. Gaskill, J.L. Tedesco, P. Asbeck, G. G. Jernigan, B. L. Vanmil, R. L. Myers-Ward, C.R. Eddy, P. M. Campbell and X. Weng, *IEEE Electron Device Letters*, 31, 260-262, 2010.
- [4] C.E. Malec and D. Davidovic, *Physical Review B*, 84, 033407, 2011.
- [5] D. Berdebes, T. Low, Y. Sui, J. Appenzeller and M. S. Lunstrom, *IEEE Transactions on Electron Devices*, 58, 3925-3932, 2011.
- [6] K. N. Parrish and D. Akinwande, *Applied Physics Letters*, 98, 183505, 2011.
- [7] E. Watanabe, A. Conwill, D. Tsuya and Y. Koide, *Diamond and Related Materials*, 24, 171-174, 2012.
- [8] B. C. Huang, M. Zhang, Y. Wang and J. Woo, *Applied Physics Letters*, 99, 032107, 2011.
- [9] A. D. Franklin, S. J. Han, A. A. Bol and V. Perebeinos, *IEEE Electron Device Letters*, 33, 17-19, 2012.
- [10] Y. Matsuda, W. Q. Deng and W. A. Goddard, *Journal of Physical Chemistry*, 114, 17845-17850, 2010.
- [11] A. Hsu, H. Wang, K. K. Kim, J. Kong and T. Palacios, *IEEE Electron Device Letters*, 32, 1008-1010, 2011.
- [12] J. A. Robinson et.al., *Applied Physics Letters*, 98, 053103, 2011.
- [13] F. Xia, V. Perebeinos, Y. Lin, Y. Wu and P. Avouris, *Nature Nanotechnology*, 179-184, 2011.
- [14] S. Russo, M. F. Craciun, M. Yamamoto, A. F. Morpurgo and S. Tarucha, *Physica E*, 42, 677-679, 2010.
- [15] A. Venugopal, L. Colombo and E. M. Vogel, *Applied Physics Letters*, 96, 013512, 2010.
- [16] B. Ghosh, *Microelectronics Engineering*, 86, 2187-2206, 2009.
- [17] A. C. Ferrari, J. C. Meyer, V. Scardaci, C. Casiraghi, M. Lazzeri, F. Mauri, S. Piscanec, D. Jiang, K. S. Novoselov, S. Roth and A. K. Geim, *Physical Review Letters*, 97, 187401, 2006.