Flexible Graphene Transistor via Printing Transfer

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ABSTRACT

Graphene is an atomic layer material with the characteristics of high mobility, high mechanical strength and transparency etc. Graphene is also an excellent candidate material for flexible electronics applications. However, due to the temperature limit of typical flexible substrates and the typical difficulties associated with implementing small feature size lithography process on flexible substrates, it is very challenging to directly fabricate fine feature sized graphene transistors on flexible substrates. We proposed an approach to fabricating fine feature sized graphene transistors on rigid substrates and transfer the fully fabricated transistors to flexible substrates via transfer printing. We demonstrated the successful transfer of arrays of monolayer graphene transistors with minimum feature size of 500nm with high yield and the demonstrated approach can be easily scaled to wafer size.
Keywords: graphene, flexible transistor, printing, surface energy,

1 INTRODUCTION

Efforts to develop the process of fabricating transistors on flexible substrate had been accelerated due to the rapid evolved of portable applications [1-3]. There are already a variety of methods that could be used to fabricate flexible devices [4-7]. Most of the prior demonstrations of flexible transistors adapts the process of transferring channel materials to a flexible substrate and fabricate transistors on the flexible substrates. For this typical approach, different methods of transferring channel materials had been developed, such as spin coating [8] and printing [9] etc. These processes were developed by targeting at different purposes: low cost, easy processing and/or high performances. However, the performance quality of transistors resulted from these approach is not comparable to that are made on the rigid substrate using the same active materials. In order to enhance the performance of the flexible devices, transferring high crystal quality materials such as single crystal membranes [10], high quality nano scale organic materials like carbon nano tubes had been attempted [11]. The results are significantly improved but are still hard to compete with those obtained from the rigid substrates, which is limited by properties of most flexible substrates. Due to the temperature limit of typical flexible substrates and the typical difficulties associated with small feature size lithography process on flexible substrates, it is very challenging to directly fabricate fine feature sized transistors on flexible substrates. In order to solve the issues, releasing the devices that are fully fabricated on the rigid substrate was carried out[7]. The technique was largely based on sacrificial release of layers, expensive and requiring special protection materials etc. For graphene devices, the traditional approach may not be accessible.

The good electrical and mechanical properties of graphene draw attention to build up the flexible graphene transistors [8,12]. And the inherent transparent nature made graphene a good candidate for display related devices like touch pad [1], portal display. For these applications, graphene may also be a substitute for the ITO like rare earth materials in the application of the flexible electrodes [1,12]. Methods of transferring large areas of the CVD graphene onto the flexible substrate had been reported and the quality of the graphene is well maintained under good protection layer like PMMA [13] when graphene is transferred from copper substrate grown by standard CVD or a thin metal layer such as Au is used for graphene obtained from silicon carbide substrate [9,14]. All these approaches demonstrated the future potential of using graphene in flexible transistors. Nevertheless, challenges on fabricating fine structures and constraints on processing temperature still exit in designing a suitable fabrication process for the abovementioned applications.

Here we report the approach of printing transfer arrays of prefabricated monolayer graphene transistors with fine features size, without using SOI substrates or any other releasing layers, to flexible substrates. The devices were first fabricated on a rigid substrate using standard transistor fabrication procedures such as channel preparations, metal contacts, dielectric layer and top gate metal contacts. The use of conventional photoresist based photolithography process, metal evaporations, and atomic layers deposition for dielectric layers is of no difference from fabricating other transistors and ICs. By pre-fabricating the devices on rigid substrates, it eliminates the need for the concern of the processing limitation of flexible substrate during the fabrication, and enables of use of much smaller dimensions (CD) in critical feature sizes. The printing transfer of fabricated transistors does not need to use any protection layers or to use any undercutting etching process. Without further processing of graphene, the graphene itself facilitates the transfer printing. These fabrication process features simplified the overall process and shows the potential to reduce the cost during practical implementation.

2 EXPERIMENT AND RESULTS

To enable successful transfer from a source substrate to a destination substrate, it strongly depends on adhesion strength control, which can be tuned by controlling the

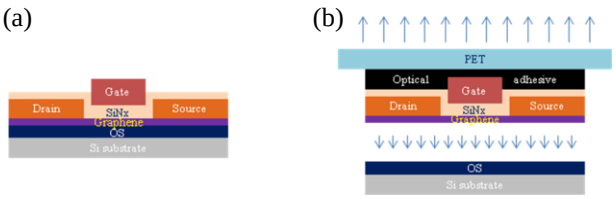


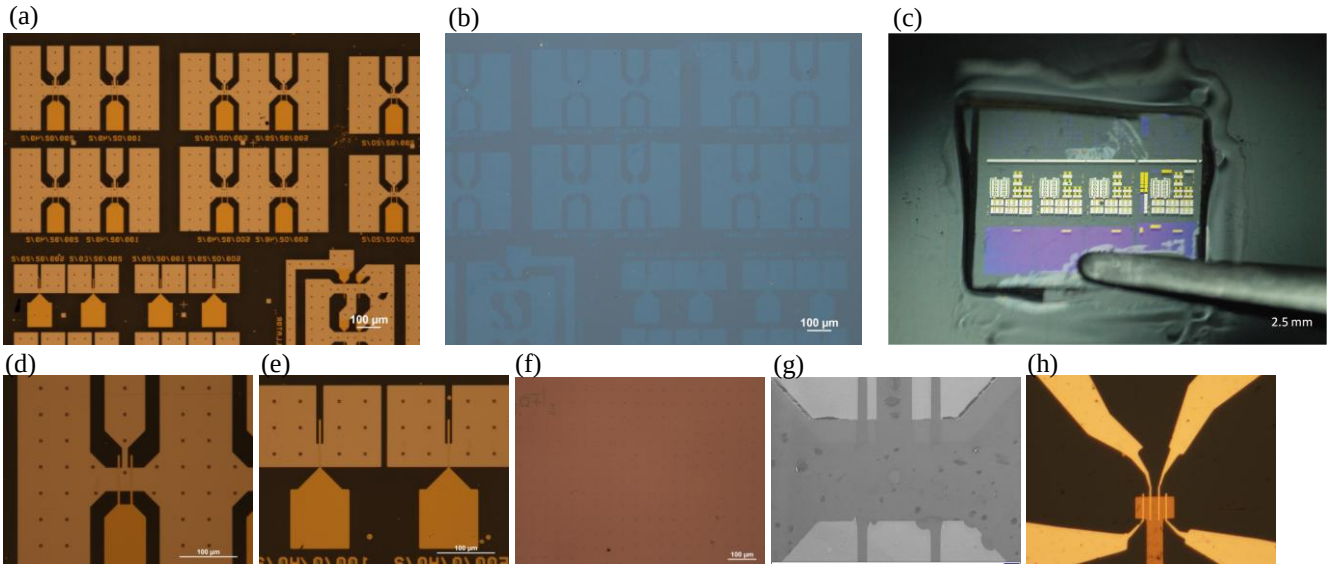
Figure 1: Cross section structure of the device before and after transfer printing. (a) Fabricated device on a rigid substrate. (b) Print transferred device with UV crosslink able optical adhesive.

surface energy of a substrate. Our source substrate is Si, where graphene is transferred to from a copper substrate. The transistors were also fabricated on the Si substrate. In order to control the surface energy of a Si, we coated organosilicate (OS) film as a surface energy-tunable passivation layer. OS was synthesized with sol-gel reaction [16]. The OS initially contains a significant amount of hydrophilic silanol (Si-OH) group so that the OS film is also relatively hydrophilic as spun on a Si wafer. However, the amount of hydrophilic silanol decreases as we increase the temperature by thermal treatment during its curing process. As a result, the OS become gradually hydrophobic. By controlling this curing temperature of OS, we were able to finely tune the surface energy of the OS substrate, which also enables us to control the adhesion strength between the OS substrate and the other layer such as a graphene in this study.

After the device fabrication was finished, a UV cross-linkable optical adhesive (Norland optical adhesive 81) was spun on the target flexible substrate. The adhesion strength between the adhesive and the device should be stronger than the graphene and the OS substrate. Cross section of the device before and after printing transfer was shown in Figure 1. The separation started from the interface between the graphene and the OS surface of the Si substrate.

Figure 2 demonstrates the direct printing results of hundreds of fabricated devices. The devices were printed one time with the yield more than 95%. When the control of the surface energy of the OS substrate is correct, a large area of low defeats was achieved as the Figure 2a. The transfer was done uniformly across the devices region especially the region with metal or the dielectric presents. This is mainly because the adhesive used in the research had a good adhesion to the two materials. The surface of the OS substrate after transferred was showed in Figure 2b and the clean surface indicates a good transfer without cracking metals. The foot print of the device remained on the substrate due to a slightly over etching outside the device region at the last step described in process fabrication. Figure 2c shows the centimeter square of the printed device. The large square of the purple membrane is PECVD silicon nitride film outside the device area. Since there is also graphene in between the membrane and the OS substrate, thus is transferred together and is shown in Figure 3f.

Figure 2d and 2e are individual Radio Frequency



Figer 2 Image of the transferred devices (a) trasferred arrays of DC and RF devices (b) surface of organosilicate (OS) substrates after device transferred (c) camera image of the transferrd device on PET substrate (d) (e) higher magnification of the RF and DC devices. (f) printed 100nm silicon nitride film (g)SEM image of the printed OS substrate (h) 500nm feature size devices by e-beam lithography process

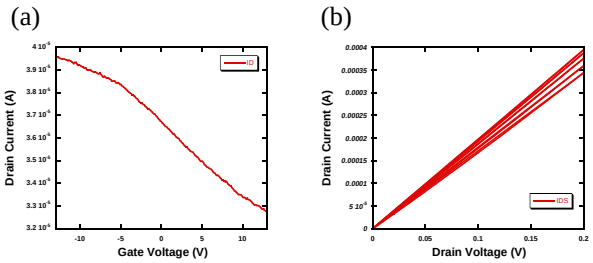


Figure 3: DC and RF measurement of the printed devices. (a) ID-VD measurement at Vds=20mV (b) ID-VG measurement at VG=-10 to 10

transistors and DC transistors. Figure g shows a SEM image on the OS substrate after transferred. And figure 2h showed the printed results of 500nm features size devices through e-beam lithography process. There was no significant dependence of the devices thickness and the device yields. In the experiment, OS substrate started to show good printing yield as the contact angle increased above 79 degree.

DC measurements were performed on the device with dimension: gate length Lg=3.45um, channel length= 1.4um, channel width 17um with analyzer HP 4155 at ambient condition. The results are shown in Figure 3. The channel after defined process is covered with the PR for protection. The results showed a high p-type doping low on/off ratio due to the protection layer used. No significant decay in the channel resistance was found indicates the graphene structure is not damaged during the transfer process. This could be improved if a better capping layer is used. RF measurement showed only cut off frequency 160MHz and maximum available gain of at 560 MHz. The low frequency mainly come from use of thick dielectric layer and the high gate-to-source and gate-to-drain capacitance with unnecessarily overlapping structures and also contributed from the low mobility result from the PR protection layers

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3 CONCLUSION

In conclusion, we demonstrated the approach of direct transfer printing fully fabricated flexible graphene transistors to flexible substrates. The process was compatible with photolithography process and is scalable to large area for batch fabrication. Future high performance flexible transistors may be achievable with graphene on low-temperature flexible substrates using graphene.

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