A Comparative Analysis of Transistors Based on Dielectrophoresis-Aligned Carbon Nanotubes (CNTs) and Assembled Random-Network CNTs

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ABSTRACT

The purpose of this project is to investigate the fabrication and characterization of carbon nanotube (CNT) thin-film transistors (TFTs), based on two solution-based fabrication methods: dielectrophoretic deposition of aligned CNTs and self-assembly of random-network CNTs. The fabrication procedures of the two transistors and their corresponding electrical characteristics are studied comparatively. The electrode design enables repeatable CNT thin-film deposition and results in transistors with comparable structures. Electrodes are fabricated on low-resistivity Si/SiO_2 wafers using lithography and wet etching. The measurement results of these two CNT transistors are compared to determine the differences in electrical characteristics. The results indicate that the self-assembly method produces a stronger field effect. This phenomenon can be further enhanced in future work by decreasing the concentration of metallic CNTs (mCNTs) through a number of different methods.

Keywords: carbon nanotube (CNT), thin-film transistor, dielectrophoresis, alignment, random network

1 INTRODUCTION

Carbon nanotubes (CNTs) have gained significant attention due to their potential as an alternative nanomaterial to be utilized in micro/nano-scale electronics. The physical and electrical properties of CNTs make them an excellent candidate for devices of this scale. At room temperature, the mobility of an individual semiconducting CNT (sCNT) can exceed 100,000 cm^2/Vs [1]. In addition, CNTs are excellent electric current carriers [2]. Another benefit of CNTs is that they can behave as a semiconductor or metallic material depending on their physical properties. Therefore, they have potential to be used as the active material to fabricate transistors or as interconnects between electronic components. A wide variety of devices, including transistors, integrated circuits, optoelectronics, and high-frequency electronics have been successfully fabricated using CNTs [3, 4].

In order to continuously improve the quality and performance of CNT-based electronic devices, the CNTs and their manipulation methods must be further explored. It is particularly important to obtain an improved understanding of the physical and electrical properties of CNTs to successfully use them in electronics [2, 5-8]. Although a significant amount of research has investigated the electrical properties of CNTs, limited research has compared the electrical properties of CNT transistors fabricated using different approaches. The purpose of this project is to compare the field effect of CNT transistors, based on two solution-based, inexpensive fabrication methods: dielectrophoretic deposition of aligned CNTs and self-assembly of random-network CNTs [2, 5].

The performance of aligned CNT devices is dependent on the alignment and density of CNTs. When dielectrophoresis (DEP) is used to position and align CNTs, varying the applied voltage and frequency can impact the concentration of deposited metallic CNTs (mCNTs), as well as sCNTs [8]. The DEP process has a selection effect on mCNTs and sCNTs, as they react to an electric field differently. The mCNTs can be removed later using various techniques, such as electrical breakdown, to obtain enhanced on/off ratios of aligned CNT transistors. A random-network CNT transistor has no selection on mCNTs or sCNTs. Both aligned arrays and random networks of CNTs have their benefits and limitiations in terms of ease of fabrication, repeatability of deposition, and device performance.

Therefore, here we report a comparative analysis of two CNT transistors. Sample devices with surface source/drain and back gate electrodes are fabricated on low-resistivity Si/SiO_2 wafers with lithography and wet etching. Aligned CNTs are deposited using DEP based on dielectrophoretic forces, and random-network CNTs are self-assembled based on electrostatic forces. The fabrication procedures are described and discussed in this paper. Electrical characteristics of the CNT transistors are obtained and analyzed to indicate the difference of the two methods. This comparative analysis can be used as a pilot study for future exploration of various types of CNT transistors.

2 EXPERIMENTS

The devices are fabricated on 4-inch low-resistivity (0.001-0.005 Ohm-cm), n-type, (100) orientation, Si wafers with a 100 nm SiO_2 insulator layer. The fabrication process of the electrodes using contact lithography and wet etching

are demonstrated in Figure 1. The Si/SiO_2 wafer is sputtered with 100 nm of Cr (adhesion metal), then 200 nm of Au (electrode metal). The wafer is cleaned with acetone and isopropyl alcohol then rinsed with deionized water. An adhesion promoter (MCC primer 80/20) then positive photoresist (Shipley S1805) are applied on the surface of the wafer using a spin coater (300 rpm for 10 s then 4000 rpm for 30 s). The exposed photoresist, Cr, and Au are removed using 351 developer for 45 s, Cr etchant for 100 s, and Au etchant for 15 s, respectively. The unexposed photoresist is removed using 1:1 mixture of H_2SO_4 and H_2O_2 at 110°C for 10 minutes. The patterned Cr/Au electrodes are used as the source and drain terminals for the transistor, while the substrate is used as the back-gate terminal.

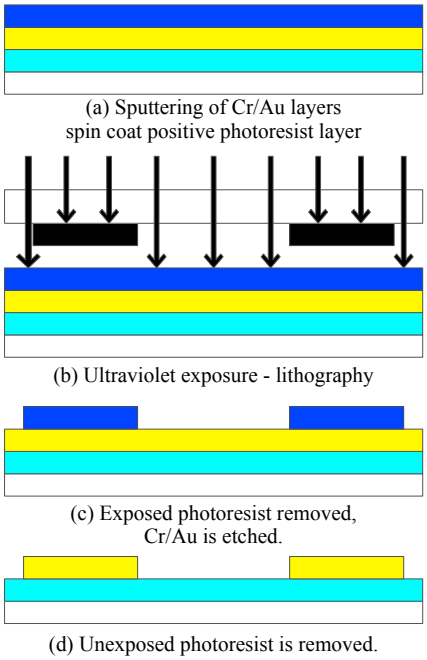

Figure 1: Fabrication process of the electrodes.

Two solution-based methods are used to deposit CNT semiconducting films. The first method is to use DEP to align CNTs between the source and drain terminals, as illustrated in Figure 2. In the DEP process, a 90% sCNT solution (IsoNanotubes-S 90%, Nanointegris) is placed between the source and drain electrodes. The CNTs are aligned across the electrodes by applying an AC voltage source (frequency of 5 MHz and peak-to-peak voltage of 10 V) using a function generator (Agilent Technologies 81150A). After 60 s, the AC signal is turned off and a syringe is used to remove the CNT solution from the device, leaving only the CNTs in contact with the substrate and electrodes. It has been proven that varying the applied voltage and frequency during DEP can impact the concentration of deposited mCNTs and sCNTs, resulting in a selection effect [8, 9]. This effect will be further explained in the following section.

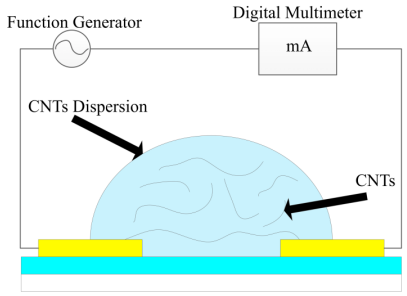

Figure 2: DEP setup for the aligned CNT transistor.

The second method used to fabricate CNT transistors is based on layer-by-layer self-assembly of CNT films, as illustrated in Figure 3. During this process, a random-network thin film of CNTs is generated with no selection of mCNTS or sCNTs. After electrode fabrication, a sacrificial layer of photoresist is patterned using a spin coater (300 rpm for 10 s then 2000 rpm for 30 s), lithography, and developer. The CNT solution, poly(diallyldimethyl ammonium chloride) (PDDA), and poly(4-styrenesulfonic acid) (PSS) are then added layer-by-layer as depicted in Figure 4. Once the random network of CNTs is applied, the substrate is submersed in a beaker of acetone, which is then placed in an ultrasonic bath. This lift-off process removes the photoresist sacrificial layer, along with the other layers above the sacrificial layer.

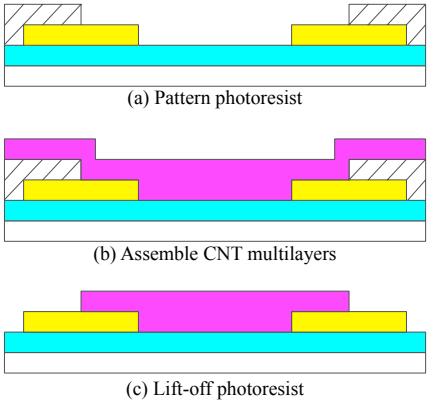

Figure 3: Process flow of the self-assembled CNT thin-film transistor.

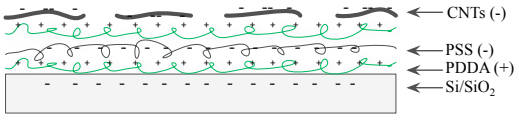

Figure 4: Layer-by-layer self-assembled CNT semiconducting layer.

Figure 4 shows the schematic of a self-assembled CNT film. Materials with different charges are held together by strong electrostatic forces. The surface charging properties

of CNTs (-), PDDA (+), and PSS (-) are determined with a zeta potential instrument (Malvern Zetasizer Nano ZS90).

An optical image of the fabricated electrodes is shown in Figure 5. The electrodes are arranged in an array so that they can be connected by external interconnection wires to other nearby electrodes to create logic gates in future work. CNTs are then applied between the electrodes by DEP (Figure 2) or self-assembly (Figures 3-4).

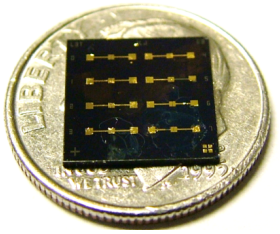

Figure 5: Optical image of a fabricated device on a dime. .

Figure 6 illustrates a structural comparison between CNT transistors based on DEP and self-assembled random-networks with their corresponding top views. The structure depicted is a back-gate transistor configuration. The low-resistivity silicon acts as a gate to simplify the fabrication and testing procedures.

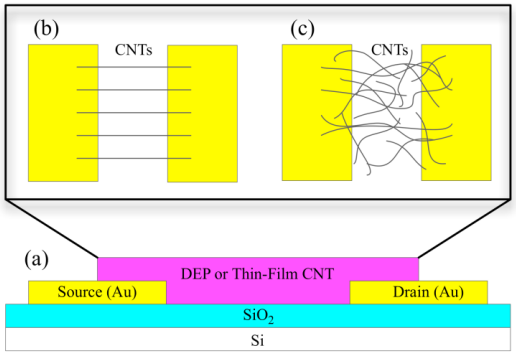

Figure 6: (a) Structure of the carbon nanotube transistor. Top views of (b) aligned CNTs based on DEP and (c) self-assembled random network of CNTs.

3 RESULTS AND DISCUSSION

Structural characterization of the CNT devices is carried out using scanning electron microscopy (SEM) (FEI Quanta 3D 200i). The electrical characteristics are obtained using a semiconductor analyzer (Agilent Technologies B1500A). The drain voltage is swept from 0 to -5 V in -100 mV increments, with gate voltage sweeping from 0 to -5 V in -1 V increments. An SEM image of the electrodes with teeth-shaped patterns and DEP-aligned CNTs is shown in Figure 7. As depicted, the CNTs are successfully positioned between the electrode teeth patterns, in the 3 µm gap. As reported by Nanointegris, the mean diameter is 1.4 nm, with a length of 0.1-4 µm.

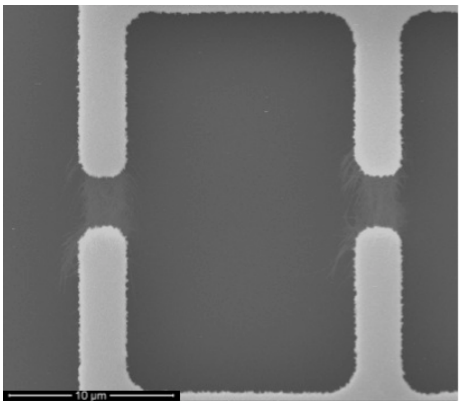

Figure 7: SEM image of aligned CNTs between source and drain electrodes.

The current-voltage (*I-V*) characteristics of a DEP-aligned CNT transistor are shown in Figure 8. The transistor demonstrates p-type output characteristics with an explicit field effect as its current is controlled by the gate voltage. However, the on/off ratio, defined as the high current (I_{on}) over the low current (I_{off}) at a drain voltage of -5 V, is low (approximately 1.48). This low on/off ratio may be a result of primarily mCNTs being aligned [8].

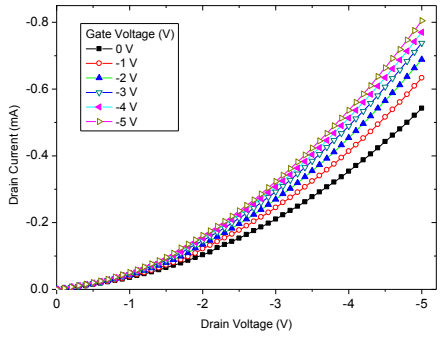

Figure 8: Output *I-V* characteristic of a DEP-aligned CNT transistor.

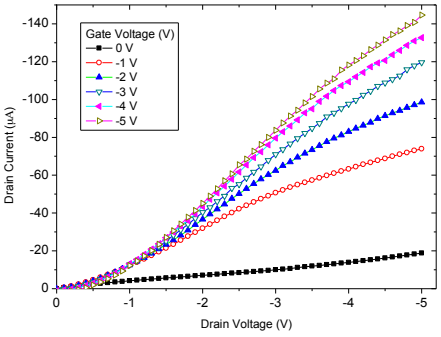

Figure 9: Output *I-V* characteristic of a self-assembled random network of CNTs transistor.

Figure 9 illustrates the *I-V* characteristics of a transistor using the self-assembled random-network CNTs. These curves show a greater field effect (larger separation between adjacent curves) when compared with the DEP results. The on/off ratio obtained at a drain voltage of -5V is found to be approximately 7.69. The current is in the 10-150 μA range, compared with the 500-800 μA range for the DEP-aligned CNT transistor. The smaller current suggests that the self-assembled random-network CNTs are less conductive.

The on/off ratio results indicate that the self-assembly method of fabrication produces a greater field effect. The reason the DEP method has a lower ratio is due to the polarizability difference between mCNTs and sCNTs. When mCNTs are placed in an alternating electric field, an alignment parallel to the induced field is the most likely scenario. This is due to their band gap being at or near zero, allowing their polarizability to be along the tube axis. Contrary to mCNTs, sCNTs have a non-zero band gap, leading to their semiconducting properties. The band gap creates transverse polarizability, which is comparable to the polarizability along the tube axis. This variation causes sCNTs to be aligned in a pseudo-random orientation [8]. Thus, when fabricating transistors with the DEP method, a higher concentration of mCNTs are aligned between the source and drain electrodes. Consequently, the electrical properties, such as the on/off ratio and the current range are shifted towards the metallic region. This effect limits the applications of these transistors, especially when they are used as electrical switches. Some potential optimization approaches have been proposed and investigated by a number of groups. Once fully developed, they can be used to reduce the concentration of mCNTs, leaving only the primarily sCNTs for transistors [6-8].

Further research will entail reducing the concentration of mCNTs. One method to accomplish this is to use a higher concentration sCNT solution, which contains a smaller number of mCNTs. For example, there are commercial 99% sCNT solutions available on the market. This could potentially increase our on/off ratio by a substantial amount. Burning off mCNTs through electrical breakdown can also be used to reduce their concentration. This is performed by increasing the current between the source and drain electrodes with zero gate voltage. Though this method is effective, it can lead to a large reduction in current drive [10].

4 CONCLUSION

CNT transistors are fabricated using two solution-based deposition methods. Their electrical characteristics are analyzed and compared with the focus on their on/off ratios and film conductivity. The results obtained from our experiments with CNTs provide crucial information on how CNTs can be used in future research and practical devices. It is particularly important to understand the electrical characteristics exhibited by different fabrication methods. The on/off ratio is of primary concern in micro/nano-scale electronics to reduce the power wasted from leakage current. This ratio has proven to be a higher value when using the self-assembly method of fabrication. Further research will be conducted to optimize the deposition process to obtain primarily sCNTs for electronic applications.

5 ACKNOWLEDGEMENT

J.L. Juhala acknowledges the support from the Sigma Xi Grants-in-Aid of Research (GIAR) (G20110315157329).

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