Effects of Random Work Function Fluctuations in Nanoszied Metal Grains on Electrical Characteristic of 16 nm High-κ/Metal Gate Bulk FinFETs

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ABSTRACT

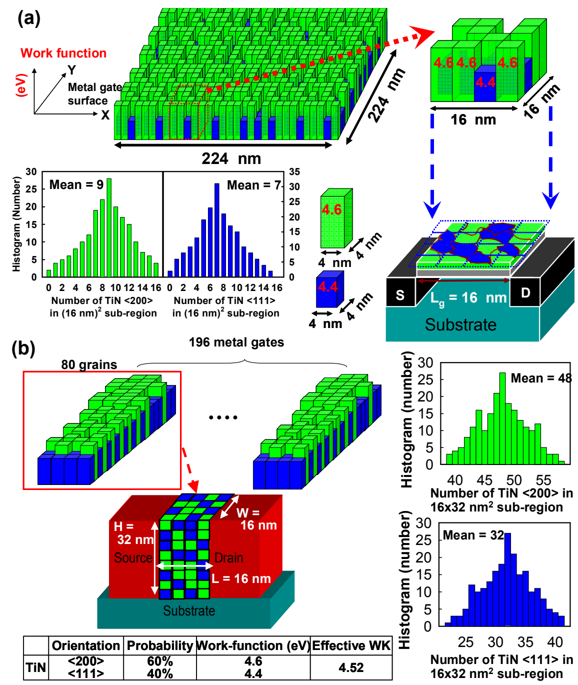
In this work, the work function fluctuation (WKF) induced variability in 16-nm-gate planar MOSFET and bulk FinFET is for the first time explored and compared. Based upon an experimentally calibrated 3D device simulation, the newly developed localized WKF (LWKF) simulation technique enables us to estimate the threshold voltage and DC baseband fluctuations of devices which accounts for the random grain's number and position effects simultaneously. The results show that the random work function, resulting from local nanosized metal grains in bulk FinFET, induced relatively small threshold voltage (V_{th}) fluctuation (about 2.5 times lower), compared with the result of planar device.

Keywords: High-κ/metal gate, Work function fluctuation, 3D device simulation, Localized work function fluctuation simulation technqiue, Threshold voltage fluctuation, On/Off state current fluctuation, Potential profile, and current distribution

1 INTRODUCTION

High-κ/metal gate (HKMG) is a key technology for sub-28-nm CMOS generations [1-2] due to reducing intrinsic parameter fluctuation, leakage current, gate resistance, phonon scattering, and no Fermi-level pinning. However, resulting from different process conditions, using HKMG approach may introduce random work functions (WKs) on device's metal gate due to various grain orientations [3-6] which is uncontrollable during fabrication. The random grain orientations result in WKs' variation due to different surface density in the polarization charges. These critical problems for future ultralarge scale integration technology applications lead to significant V_{th}'s shift and device performance degradation.

In this study, based on experimentally calibrated 3D device simulation [7], WKF of 16-nm TiN/HfO_2 bulk FinFET [8-10] is investigated. Effects of individual WKF on device's DC characteristic are captured using LWKF simulation technique [1], where the random position and number of nanosized metal grains are for the first time modeled and examined and compared for both the bulk FinFET and planar MOSFET devices. Physical findings on WKF of HKMG devices are discussed accordingly. This paper is organized as follows. Section 2 briefs the simulation methods of LWKF. In Section 3, the random WKs induced fluctuations are estimated. Finally, we draw conclusions and suggest future works.



	Orientation	Probability	Work-function (eV)	Effective WK
TiN	<200> <111>	60% 40%	4.6 4.4	4.52

Figure 1: Schematic of (a) planar MOSFET and (b) bulk FinFET with random metal grain on the gate, where the size of metal grain are 4 x 4 nm^2 and only two kind of <200> (green color) and <111> (blue color) orientations are considered according toV the material property, as listed in Table. The plot of distribution of number of <200> and <111> orientations with 196 samples for planar MOSFET and bulk FinFET, where 16 and 80 randomly generated grains in gate regions of planar MOSFET and bulk FinFET, respectively.

2 THE LWKF SIMULATION TECHNIQUE

The devices we studied are the 16-nm-gate planar MOSFETs and bulk FinFET (width: 16 nm) with amorphous-based TiN/HfO_2 gate stacks and an EOT of 0.8 nm, where the parameter setting is according to ITRS roadmap for low operating power [11]. In contrast to the averaged WKF method [6,12] or compact model approach [3], our method directly partitions the area of device's metal gate into many sub-regions, where the size of sub-region is 4 nm. For example, as shown in Fig. 1(a), we randomly generate the WKs to each sub-region of TiN gate of planar MOSFET according to material's property, as listed in the

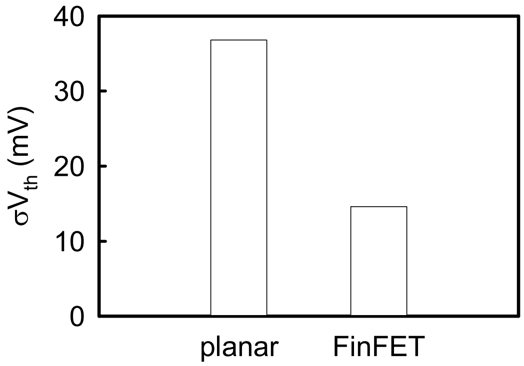


Figure 2: Plot of σV_{th} vs. planar MOSFET and bluk FinFET, respectively.

inset table, and then map them into planar MOSFET gate area for 3D device quantum transport simulation [1]. The total generated samples are 196. The material we used here is TiN gate and has 4.4 eV and 4.6 eV WKs for N-MOSFETs [6], where the distributions of number of <200> and <111> orientaions are plotted and the average number of TiN <200> and <111> orientations are 9 and 7, respectively. Similarly, the gate of bulk FinFET is partitioned into 80 sub-regions and the WKs are assigned according to TiN's property, where the height and width are 32 and 16 nm and the distributions of number of <200> and <111> orientations are illustrated, as shown in Fig. 1(b). And the numbers of <200> and <111> orientations are 48 and 32, respectively. The accuracy of device simulation was calibrated with measured data for 15/20 nm CMOS device in our early work [7].

3 Results and Discussion

Based on localied WK method, the σV_{th} induced by random WKs is properly estimated for planar MOSFET and bulk FinFET, respectively, where the fluctuation in bulk FinFET is 2.5 times smaller than planar MOSFET, as shown in Fig. 2. From plot of V_{th} versus different number of TiN <200> orientation, the distribution of V_{th} variation for planar MOSFET is wider than bulk FinFET, as shown in Fig. 3. Because the channel is only controlled by one gate, the random WK varition in planar MOSFET is significant. The bulk FinFET with three gate suppresses the fluctuation induced by random WKs well, where the differences of maximu and minimal V_{th}s are 0.24 and 0.07 V for planar MOSFET and bulk FinFET, respectively. The effect of random grain number and position is further investigated. Due to random grain position effect, the device with the same number of <200> orientation has different V_{th}. For example, the case 1 with large number of 4.6 eV of WK resulting in higher band profile near the source has higher V_{th}, as shown in dash box, where the higher or lower WK will raise and lower the band profile. The case 2 with larger number of 4.4 eV of WK resulting in

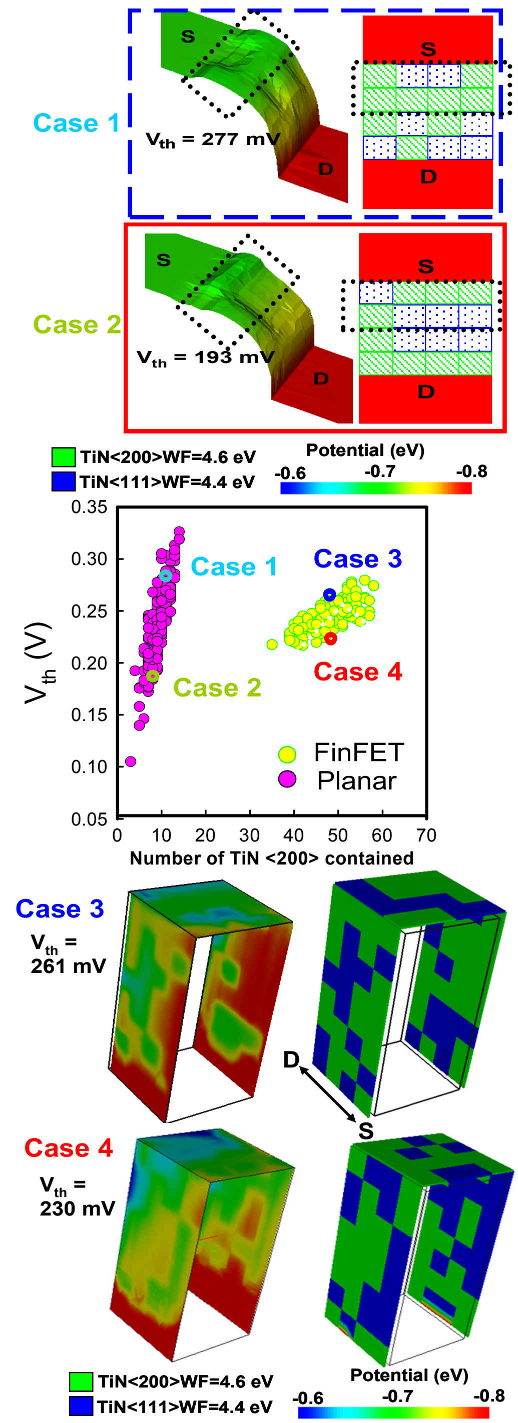


Figure 3: The distribution of V_{th} versus number of <200> orientation for planar MOSFET and bulk FinFET, respectively. The case 1 and case 2 are planar MOSFET with same number but different position of <200> orientation, and case 3 and case 4 are bulk FinFET with the same number but different position of <200> orientation due to grain position effect.

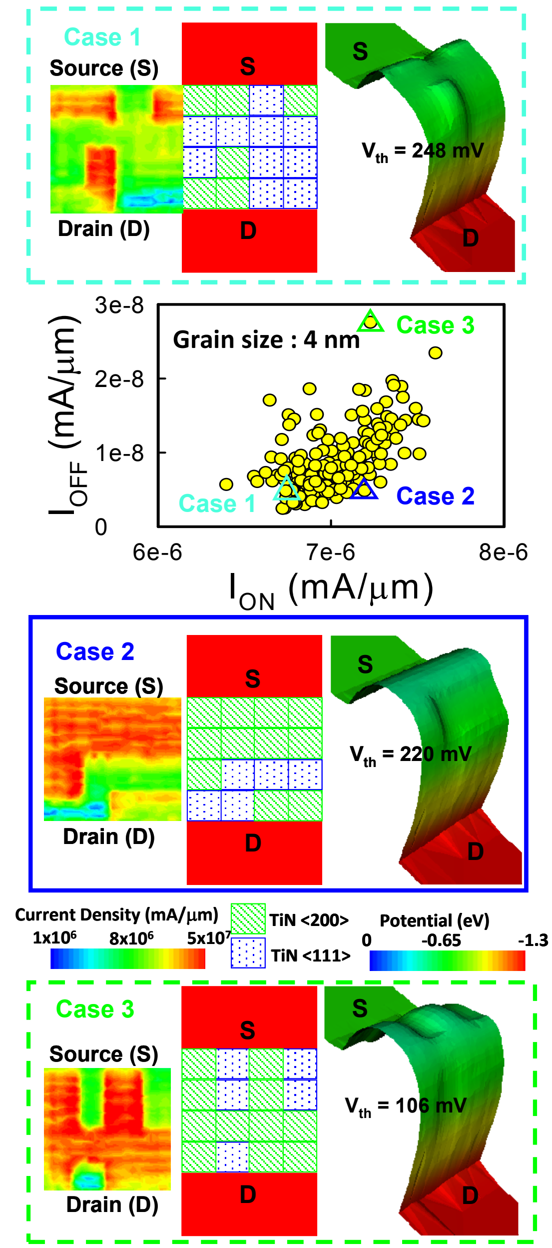


Figure 4: The plot of I_{off} versus I_{on} for planar MOSFET, where the case 1 and case 2 are the fluctuated cases with similar I_{off} but different I_{on} due to grain number effect; the case 2 and case 3 are the fluctuated cases with similar I_{on} but different I_{off} due to grain position effect.

lower band profile near the source has lower V_{th}, then increases the leakage current. These phenomena occurred in planar MOSFET are due to random grain position effect. For bulk FinFET, although the larger gate area with large number of grain orientations, the better controllability suppresses the V_{th} fluctuation induced by random WK.

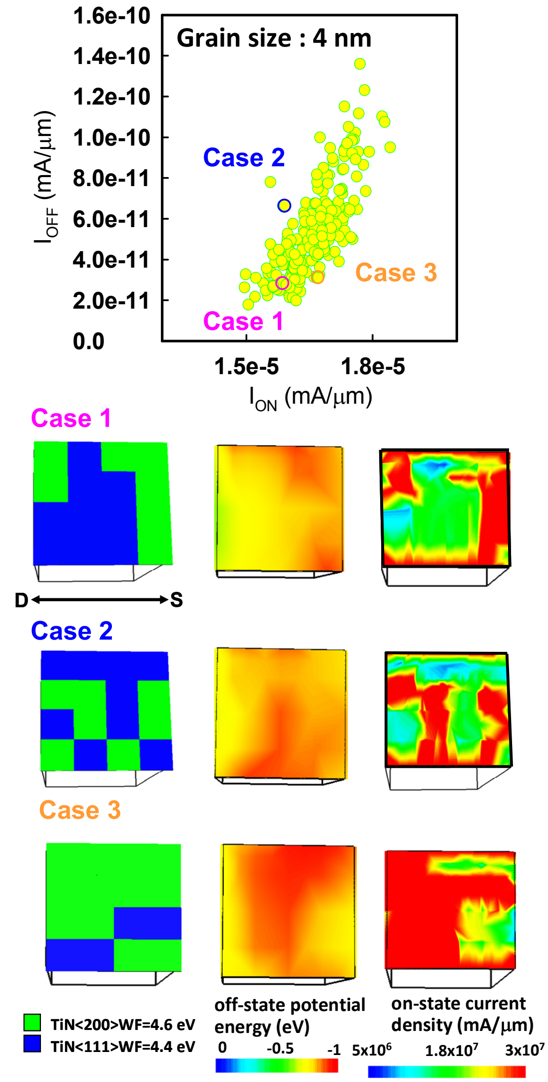


Figure 5: (b) The plot of I_{off} versus I_{on} for bulk FinFET, where the case 1 and case 2 are the fluctuated cases with similar I_{on} but different I_{off} due to grain position effect; the case 2 and case 3 are the fluctuated cases with similar I_{off} but different I_{on} due to grain number effect.

For example, the case 3 with larger number of 4.6 eV of WK near the source has higher potential profile, as shown in red color. The case 4 with larger number of 4.4 eV of WK near the source has lower potential, as shown in yellow and green colors. From plot of on-state current (I_{on}) vs. off-state current (I_{off}), the effect of grain number and position for planar MOSFET and bulk FinFET are investigated clearly, respectively. For planar MOSFET structure, the case 2 with larger number of 4.6 eV of WK has larger current density, compared with case 1, where the red color indicates higher current density. Compared with case 3, the case 2 with larger number of 4.6 eV of WK near source raises the band profile and results in higher V_{th}, even they have similar I_{on}. For bulk FinFET structure, the plot of I_{off} vs. I_{on} shows larger I_{on} and smaller I_{off}, compared with planar MOSFET. And the difference of current density of bulk FinFET is smaller than that of planar MOSFET, where the ranges are 5×10^6 - 3×10^7 and 1×10^6 - 5×10^7 mA/μm, respectively. For grain position effect, the case 2 has larger I_{off} than the case 1 even they have the same number of 4.6 eV of WK. Because the case 1 with larger number of 4.6 eV of WK has larger V_{th} resulting in lower I_{off}, the case 2 with lower WK near source has larger I_{off}. Similarly, due to grain number effect, the case 1 and case 3 have similar I_{on} but different I_{off}.

4 CONCLUSIONS

In this paper, we have explored the impact of WKF in planar MOSFET and bulk FinFET, respectively. The device has different V_{th} even they have the same number of <200> orientation owing to random WK's position effect. Similarly, the device number of random 4.4 and 4.6 eV of WK has different V_{th} owing to random WK's number effect. Compared with planar MOSFET, a 60% ((0.0368-0.0146) / 0.0368 x 100%) reduction of σV_{th} induced by WK fluctuation is observed for bulk FinFET.

ACKNOWLEDGEMENT

This work was supported in part by Taiwan National Science Council (NSC) under Contract NSC-99-2221-E-009-175 and by TSMC, Hsinchu, Taiwan, under a 2009-2010 grant.

REFERENCES

[1] H.-W. Cheng, F.-H. Li, M.-H. Han, C.-Y. Yiu, C.-H. Yu, K.-F. Lee, and Y. Li, "3D Device Simulation of Work Function and Interface Trap Fluctuations on High-κ/Metal Gate Devices," in: IEDM Tech. Dig., pp. 378-382, 2010.

[2] X. Chen, S. Samavedam, V. Narayanan, K. Stein, C. Hobbs, C. Baiocco, W. Li, D. Jaeger, M. Zaleski, H. S. Yang, N. Kim, Y. Lee, D. Zhang, L. Kang, J. Chen, H. Zhuang, A. Sheikh, J. Wallner, M. Aquilino, J. Han, Z. Jin, J. Li, G. Massey, S. Kalpat, R. Jha, N. Moumen, R. Mo, S. Kirshnan, X. Wang, M. Chudzik, M. Chowdhury, D. Nair, C. Reddy, Y. W. Teh, C. Kothandaraman, D. Coolbaugh, S. Pandey, D. Tekleab, A. Thean, M. Sherony, C. Lage, J. Sudijono, R. Lindsay, J. H. Ku, M. Khare, and A. Steegen, "A Cost Effective 32 nm High-κ/Metal Gate CMOS Technology for Low Power Applications with Single-Metal/Gate-First Process," in Digest of Technical Papers, 2008 Symposium on VLSI Technology, 88-89, 2008.

[3] X. Zhang, J. Li Grubbs, M. Deal, M. Magyari-Kope, B. Clemens, B.M. Nishi, Y, "Physical Model of the Impact of Metal Grain Work Function Variability on Emerging Ual Metal gate MOSFETs and its Implication for SRAM Reliability," in: IEDM Tech. Dig., 57-60, 2009

[4] K. Ohmori, T. Matsuki, D. Ishikawa, T. Morooka, T. Aminaka, Y. Sugita, T. Chikyow, K. Shiraishi, Y. Nara, K.Yamada, "Impact of Additional Factors in Threshold Voltage Variability of Metal/High-k Gate Stacks and its Reduction by Controlling Crystalline Structure and Grain Size in the Metal Gates," in: IEDM Tech. Dig., 409-412, 2008.

[5] L. Brunet, X. Garros, M. Cassé, O. Weber, F. Andrieu, C. Fenouillet-Béranger, P. Perreau, F. Martin, M. Charbonnier, D. Lafond, C. Gaumer, S. Lhostis, V. Vidal, L. Brevard, L. Tosti, S. Denorme, S. Barnola, J.F. Damlencourt, V. Loup, G. Reimbold, F. Boulanger, O. Faynot, A. Bravaix, "New Insight on VT Stability of HK/MG Stacks with Scaling in 30nm FDSOI Technology," in: VLSI Symp. Tech. Dig., 29-30, 2010.

[6] H. Dadgour, K. Endo, V. De, and K. Banerjee, "Modeling and Analysis of Grain-Orientation Effects in Emerging Metal-Gate Devices and Implications for SRAM Reliability," in: IEDM Tech. Dig., pp. 705-708, 2008.

[7] Y. Li, S.-M. Yu, J.-R. Hwang and F.-L. Yang, "Discrete Dopant Fluctuations in 20-nm/15-nm-Gate Planar CMOS," IEEE Trans. Electron Devices, vol. 55, no. 6, pp. 1449-1455, June, 2008.

[8] Y. Liu, T. Matsukawa, K. Endo, M. Masahara, S.-i. O'uchi, K. Ishii, H. Yamauchi, J. Tsukada, Y. Ishikawa, and E. Suzuki, "Cointegration of High-Performance Tied-Gate Three-Terminal FinFETs and Variable Threshold-Voltage Independent-Gate Four-Terminal FinFETs With Asymmetric Gate-Oxide Thicknesses," IEEE Trans. Electron Devices, vol. 47, no. 12, pp. 2320–2325, Dec. 2000.

[9] Y. X. Liu, K. Endo, M. Masahara, E. Sugimata, T. Matsukawa, K. Ishii, H. Yamauchi, T. Shimizu, K. Sakamoto, S. O'uchi, T. Sekigawa, and E. Suzuki, "Advanced FinFET Technology: TiN Metal-Gate CMOS and 3T/4T Device Integration," in: Proc. IEEE Int. SOI Conf., 219-220, 2005.

[10] Kedzierski, J.; Ieong, Meikei; Nowak, E.; Kanarsky, T. S.; Zhang, Ying; Roy, R.; Boyd, D.; Fried, D.; Wong, H.-S. P., "Extension and Source/Drain Design for High-Performance FinFET Devices," IEEE Trans. Electron Devices, vol. 50, 952-958, 2010.

[11] Y. Li, C.-H. Hwang, T.-Y. Li, M.-H. Han, "Process-Variation Effect, Metal-Gate Work-Function Fluctuation, and Random-Dopant Fluctuation in Emerging CMOS Technologies," IEEE Trans. Electron Devices, vol. 57, no. 2, pp. 437-447, February, 2010.

[12] H.-W. Cheng and Y. Li, "Random work function variation induced threshold voltage fluctuation in 16-nm bulk FinFET devices with high-k-metal-gate material," in: Proc. IEEE The 14th Int'l Workshop on Computational Electronics (IWCE), 4 pages, 2010.