

Integrated Phase-Change Memory Devices using Bi₂Te₃ Nanowires

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ABSTRACT

Bismuth telluride (Bi₂Te₃) and its alloys are considered to be the best available materials for near room-temperature thermoelectric applications. Moreover, because low-dimensional thermoelectric materials are expected to have a higher figure of merit due to quantum confinement effects, Bi₂Te₃ nanowires have been studied extensively. However, their memory switching behavior has never been studied in Bi₂Te₃ nanowires. Here, we report for the first time on reversible memory switching effects in Bi₂Te₃ nanowires fabricated using anodized aluminum oxide (AAO) membranes. We find that Bi₂Te₃ nanowires show a reversible crystalline-amorphous phase change induced by temperature or electric field, similar to that reported for chalcogenide materials (Ge-Sb-Te alloys, GST), and we demonstrate that Bi₂Te₃ nanowires show considerable promise as building blocks for phase change random access memory (PRAM).

Keywords: Bi₂Te₃ Nanowires, PRAM Nanodevices, Self-Assembly, Structure-Property Relationships, Data Storage.

1 INTRODUCTION

Phase-change materials are used in nonvolatile optical memory, such as in CDs and DVDs, and are now being actively investigated as media for use in universal solid-state memory devices that combine rapid read and write speeds, high storage density, and nonvolatility. The key feature of PRAM is the reversible phase transition of the phase-change material between the crystalline (low resistivity, SET) and amorphous (high resistivity, RESET) states, as caused by an electrical pulse.

A major obstacle to the achievement of high density PRAM devices is the large writing currents required to generate the thermal energy needed for a phase change, particularly during the crystal-to-amorphous phase transition in which a high current is required for melting. In order to reduce the writing currents, GST nanowires have been synthesized and shown to satisfy many of the attributes of universal nonvolatile memory devices. However, GST nanowires are usually synthesized using

vapor transport methods at high temperatures, and their large-scale assembly is not yet feasible. On the other hand, the Bi₂Te₃ nanowires that have been observed to exhibit comparable memory switching characteristics to GST nanowires can be fabricated at room temperature using AAO membranes. Furthermore, the vertical growth of nanowires on a substrate allows the high-density assembly of Bi₂Te₃ nanowires.

2 EXPERIMENT PART

2.1 Synthesis and Characterization of Bi₂Te₃ Nanowires

Bi₂Te₃ nanowires were prepared by electrodeposition of Bi₂Te₃ within the nanopores of AAO membranes. First, AAO membranes with a mean pore diameter of 70 nm were grown by anodizing high-purity Al plates. Next, for the electrodeposition, a gold (Au) film with 300-nm thickness was deposited onto one side of the AAO membrane. Bi₂Te₃ was electrodeposited into the nanopores of the AAO membrane at a constant voltage of -10 mV in an electrolyte composed of HNO₃ (1 M), Bi₂O₃ (0.01 M), and TeO₂ (0.01 M). The working, counter, and reference electrodes were a Au/AAO, Pt plate, and Ag/AgCl electrode (in a 3.5 M KCl solution), respectively.

Then, the Au film was removed by ion milling and the AAO membranes were completely dissolved by immersion in NaOH (6 M) for 1 h. Finally, the Bi₂Te₃ nanowires were collected and dispersed in ethanol.

2.2 Fabrication of the Individual Bi₂Te₃ Nanowire Devices and Measurements

Two types of individual Bi₂Te₃ nanowire devices were fabricated. The first device was fabricated on a Si substrate with a 200nm thick thermally grown SiO₂ layer and was used to measure the electrical properties of the nanowire. The 100nm thick Pt electrodes were defined by standard electron beam lithography and lift-off techniques. The completed devices were covered with a 50nm thick layer of SiO₂ to prevent the oxidation and evaporation of Bi₂Te₃.

The second device was fabricated on a transparent Si_3N_4 membrane and was used to perform the simultaneous electrical measurements and TEM analysis. In this case, the start substrate was a $500\mu\text{m}$ thick double polished $\langle 100 \rangle$ Si substrate with layers of Si_3N_4 (50 nm) on both the front and back sides. A pattern for the transparent membrane was made initially using photolithography on the back of Si wafers, centered and in 12 point non-bold type. The paper begins with the abstract and keywords followed by the main text. It ends with a list of references.

2.3 Fabrication of Bi_2Te_3 Memory Cell Arrays

First, Ti (10 nm), Au (5 nm), and Al (1 μm) films were deposited on a Si substrate with a thermally grown SiO_2 layer. AAO nanopores with 70nm diameters were then grown using a two-step anodization process. Next, polymethyl methacrylate (PMMA) windows ($2 \times 2 \mu\text{m}^2$) were patterned. The barrier layers within the nanopores of the AAO membrane inside the open windows were removed by exposing them to a 6 wt% H_3PO_4 solution at room temperature. Subsequently, the Bi_2Te_3 nanowires were grown by electrodepositing Bi_2Te_3 inside the pores of the AAO membrane. The length of the Bi_2Te_3 nanowires was controlled using careful monitoring the deposition current, which suddenly increased when the nanowires had infiltrated to the end of the nanopores. Finally, Pt electrodes were deposited on the top of the Bi_2Te_3 nanowires.

3 RESULTS AND DISCUSSION

3.1 Analysis the characteristics of Nanowire

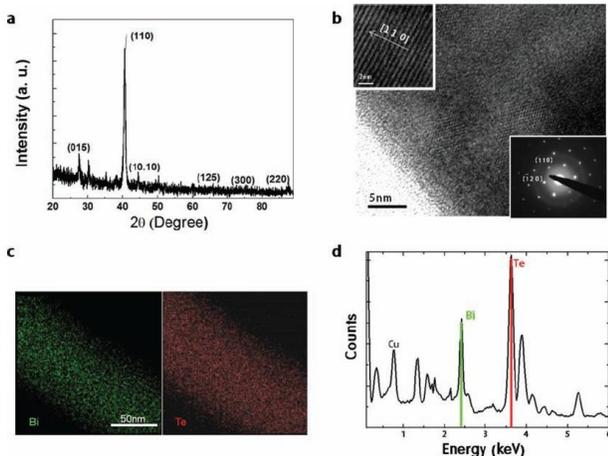


Figure 1. a) XRD pattern of Bi_2Te_3 nanowires. b) TEM image of the as-grown Bi_2Te_3 nanowire. The top right inset is a magnified HRTEM image taken from the area denoted by the rectangular box, and the bottom left inset is a SAED

pattern indexed for rhombohedral Bi_2Te_3 . c) STEM elemental mapping

images of the nanowire revealing the spatial distribution of the Bi and Te elements. d) EDS point scanning at arbitrary positions of the nanowire.

Bi_2Te_3 nanowires, as shown figure 1(a), when the Bi_2Te_3 nanowires form crystalline phase structure, this figure 1(a) was investigated by x-ray diffraction (XRD). The crystalline nanostructure of Bi_2Te_3 NWs in alumina were investigated by x-ray diffraction (XRD) employing $\text{Cu K}\alpha$ ($\lambda=1.54056 \text{ \AA}$) radiation. X-ray diffraction spectra of the as-growth Bi_2Te_3 nanowires confirms that the preferred orientation for the growth along the direction [110].

The high-resolution TEM(HRTEM) image obtained from the area designated in Figure 3c also shows clear lattice spacing with 0.152 nm, which corresponds to the (110) lattice planes of rhombohedral Bi_2Te_3 (Figure 1(d)). HRTEM image (Figure 1(c)) of a Bi_2Te_3 nanowire shows lattice fringes with spacing of 0.152nm corresponding to (011) crystal plane consistent with the XRD analysis .

3.2 The electrical measurements of Bi_2Te_3 devices

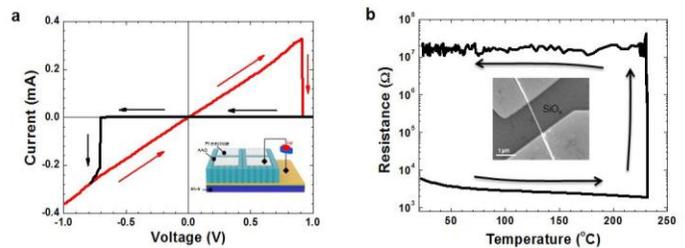


Figure 2. (a) Current-voltage (I-V) characteristics of vertically aligned Bi_2Te_3 nanowire array. The inset shows a schematic of the measurement setup. (b) Resistance - temperature characteristics measured for a Bi_2Te_3 individual nanowire device. The inset shows a FESEM image of the individual nanowire device used in the temperature dependence measurements.

To evaluate the data retention properties of Bi_2Te_3 nanowire devices, we measured the resistance as a function of time at different temperatures persisted for longer times at lower temperatures, but the transition to the low-resistance state occurred due to recrystallization. In addition, we also fabricated a Bi_2Te_3 individual nanowire device on a transparent Si_3N_4 membrane (Figure 3a) to perform simultaneous electrical measurements and TEM analysis. As expected, the as-grown nanowire had a linear I – V curve (Figure 3 b) and a crystalline structure (Figure 3 c). However, applying a voltage pulse (7 V, 40 ns) led to an increase in resistance from 0.61 k Ω to 7.5 M Ω , as denoted by the red squares in Figure 3 b. Figure 3 d shows a TEM image of the Bi_2Te_3 nanowire obtained after switching to the high-resistive state.

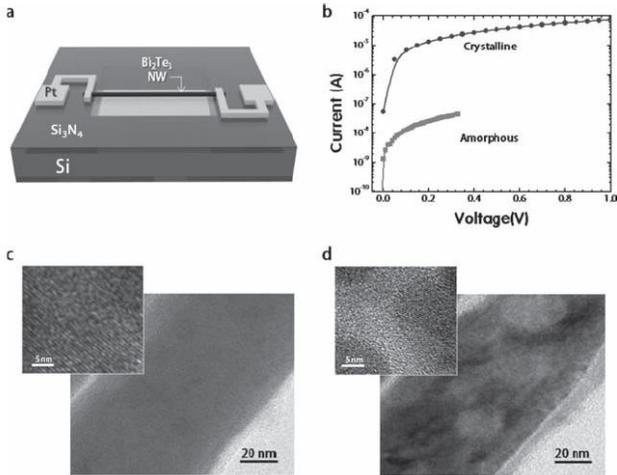


Figure 3. a) A schematic of a Bi_2Te_3 individual nanowire device fabricated on a Si_3N_4 transparent substrate. b) $I - V$ characteristics of the individual nanowire device before (black circles) and after (red squares) the application of a voltage pulse (7 V, 40 ns). HRTEM image of the nanowire c) before and d) after the application a voltage pulse (7 V, 40 ns). The insets show the high-magnification HRTEM images.

3.3 Electrical measurement of Bi_2Te_3 array device

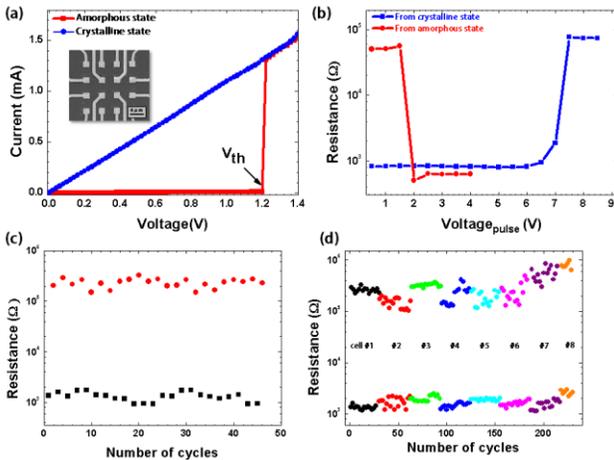


Figure 4. a) $I - V$ characteristics of a Bi_2Te_3 nanowire array device in the crystalline state (black circles). The $I - V$ characteristics after applying a voltage pulse (1 V, 1 μs) that leads to amorphization are shown as red squares. The inset shows the FESEM image of nanowire array devices. b) Resistance change of the nanowire array device as a function of writing pulses with different voltage pulses (amorphization:40ns; recrystallization:100ns), obtained for initially amorphous (red circles) and crystalline (black squares) phases. c) Endurance cycling test for the nanowire array device. The write/read/erase/read pulse sequence is applied continuously using writing (7 V, 40 ns) and erasing

pulses (2 V, 100 ns). d) Endurance cycling tests for eight nanowire memory cells.

To assess the suitability of Bi_2Te_3 nanowires for phase-change memory applications, we constructed a 4×4 array consisting of 16 Bi_2Te_3 nanowire memory cells (2 $\mu\text{m} \times 2 \mu\text{m}$) on a SiO_2/Si substrate (inset of Figure 4 a). Each memory cell exhibited an $I - V$ curve similar to that of the individual nanowire devices (Figure 4 a). Figure 4 b depicts the resistance variation measured for the memory cell as a function of the voltage pulses for the crystalline-to-amorphous (RESET) and amorphous-to-crystalline (SET) transitions. When the resistance was initially in the SET state, it increased sharply by over two orders of magnitude with voltage pulses (40 ns) greater than 7 V. When the resistance was initially in the RESET state, it dropped abruptly with voltage pulses (100 ns) greater than 2 V. It is interesting to note that the recording speeds (40 and 100 ns) were comparable or slightly faster than those for the GST nanowires.

All memory cells yielded similar resistance values for the SET and RESET states with an average resistance ratio of 100, which was sufficiently high to enable large-array operation. These results demonstrated that an array at least as large as 4×4 could be built by combining bottom-up synthesis (Bi_2Te_3 nanowires) with a conventional device fabrication technique (Pt electrodes) with consistent behavior in the array's memory cells.

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