Modeling of High Voltage Devices for ESD Event Simulation in SPICE

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ABSTRACT

A new ESD compact modeling using macro-modeling approach is introduced in this work for high voltage Lateral Double-diffused MOS (LDMOS) devices and high-voltage protection clamps. The objective is to address the distinctive device properties in high voltage devices and the ESD simulation requirements in high voltage mixed-signal applications. The LDMOS ESD model consists of a sub-circuit that is built on top of the standard (MOS20) model. On the other hand, the high voltage clamp, consisting of a thyristor-type device, is modeled using advanced bipolar junction transistor models. The simulation of these high voltage devices agrees well with TLP measurements.

Keywords: Compact model, simulation, ESD, LDMOS

1 INTRODUCTION

BCDMOS process technologies are key in enabling highly integrated mixed-signal applications for the automotive, medical and industrial sectors. Achieving satisfactory ESD (Electrostatic Discharge) performance in high voltage mixed-signal applications, however, is very challenging due to the pronounced sensitivity of the high voltage functional blocks compared with the low voltage circuits. Synthesized co-design approaches are required for robust ESD protection design and successful circuit optimization.

SPICE simulation has been demonstrated to be suitable for predicting the ESD performance of a design prior to manufacturing as well as diagnosing ESD failures after manufacturing in CMOS and BJT technologies [1, 2]. The circuit-level ESD event simulation can provide designers useful insight in the interaction between ESD and core circuit function and allows them to optimize their ESD protection design. A key requirement for such simulation is the availability of compact models that are accurate in the ESD operation regime. ESD capable compact models for high voltage core devices and complex protection clamps are not readily available in the industry. This requires the development of new methodologies that can enable the model implementation and subsequent system-level simulation of high voltage mixed signal applications.

Previously reported work in the literature on device modeling for ESD event simulation mostly focused on modeling the low voltage protection devices [1, 2]. High voltage devices have distinct properties that need to be addressed. LDMOS devices are increasingly used in a variety of analog as well as mixed-signal applications operating at voltages up to 200V or higher. The asymmetrical nature of LDMOS devices results in the devices snapback characteristics that is different from low voltage MOS devices. Moreover, the complexity of the high voltage ESD clamp devices also requires special consideration in the modeling approach.

Very few works on SPICE modeling efforts for LDMOS ESD simulation have been reported in the literature [3, 4]. The latter models have significant shortcomings that limit their usage. For example, the model reported in [4] is not a self-consistent one since two different sets of parameters are used for different operation regions. The special equation implementations required in those models often limit their availability and may have disadvantages on simulation speed and convergence.

In this article, a new ESD compact modeling approach using macro-models is introduced for high voltage LDMOS devices and high voltage protection clamps. This addresses the unique requirements in the high voltage devices. This macro modeling approach is based on standard circuit elements only and has been successfully applied in low voltage devices [1, 5]. The device models for those standard circuit elements are included in most commercial circuit simulators, which make the SPICE simulation for high voltage ESD protection more accessible to ESD and I/O circuit designers.

2 HV LDMOS DEVICES AND ESD PROTECTION

2.1 High Voltage NLDMOS devices

Figure 1 depicts a cross-sectional view of the n-type LDMOS device that is modeled in this work. The poly-gate is deposited on top of a thin 140A gate oxide and overlaps the field oxide as well. The N+ Source and P+ Back-gate (BG) diffusions are shorted together and are both enclosed by a P-Well diffusion. The latter along with a lightly-doped P-Field diffusion extends under the Poly-gate. The N+ Drain is separated from the N+ Source by the Poly-gate and the field oxide. The whole structure is formed on top of a Deep-N-Well diffusion. This LDMOS device structure is able to sustain a high voltage/low current per unit area between the drain- and source- terminal, while be driven by the low gate voltage signal provided by the internal control circuits, e.g., 5V in this technology. An added complication when integrating this type of device directly at outputs, however, is the device sensitivity to ESD-induced damage.

Currently the design of ESD protection for such application is typically achieved by trial and error and in decrement of performance, cost, and even functionality of the IC in emerging applications [6, 7]. Modeling this device for simulation in the ESD regime is of special interest for the optimum co-design of mixed-signal high voltage-tolerant circuits.
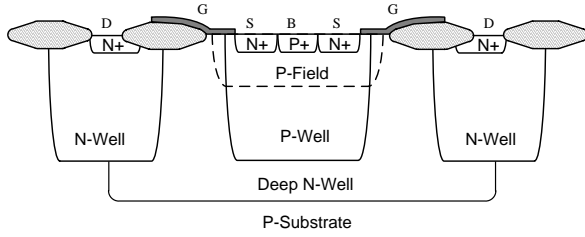

Fig. 1. Cross-sectional view of 20V LLDMOS device modeled for ESD simulations.

2.2 HV Operation ESD protection Clamp

Efficient protection devices for high voltage mixed-signal circuits are typically required in high voltage technologies for robustness purposes. This would be the case for instance for designs including relatively small (< 2000 μm) LDMOS devices as part of the output interface design. Fig. 2 shows a partial view of a new type of high voltage protection device that has been used for robust on-chip design in IC consumer electronics sectors [8].
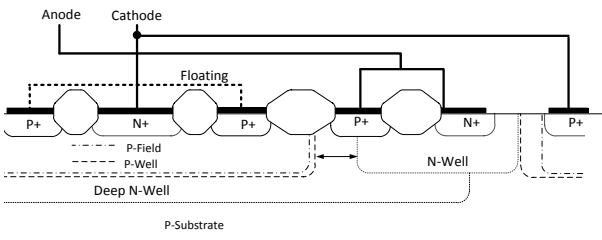

Fig. 2. Partial cross-sectional view of a high voltage protection clamp for BCD applications [8].

This high voltage protection device is symmetric in nature, with N+ diffusion islands distributed in the middle along the width of the device to define the cathode electrode. The cathode connects to the substrate P-Well, which creates the anode side of the built-in diode for reverse conduction. This latter P-Well region forms a ring around the device, serving as a large anode area of this diode. Connected to the anode electrode are the P+ diffusion regions that form the emitter of the embedded PNP device. The purpose of the array of wells on the anode side is to provide device stability during fast transients that can occur during normal operation. The N+ diffusion regions in the periphery also connect to the anode and serve as the base of the PNP and high voltage isolation ring to substrate. The P+ diffusions regions in the center of the device can be connected to the cathode in different ways to optimize performance of the device protecting the LDMOS.

The anode electrode of the device typically is contacting a bond pad handling a mixed-signal high voltage levels and the cathode electrode is contacting the reference bond-pad, typically a ground or a negative substrate voltage reference. When a random external stress appears between the two electrodes of the device, two conditions of bidirectional ESD discharge through the device take place. In a first case, when the voltage condition in the anode is lower than the cathode terminal, the built-in diode conducts in forward. For the second condition, when the voltage difference between the anode and cathode exceeds the center blocking junction formed around the center P-Well region, the device triggers a regenerative feedback process between the embedded NPN and PNP creating a low impedance discharge path.

3 SNAPBACK MODELING

3.1 Operation of LDMOS and HV Clamp

Similar to low voltage MOS devices, the high voltage LDMOS devices may exhibit snapback effect under ESD stress condition. However, there is difference between them as to be indicated in the TLP (Transmission Line Pulse) plot of LDMOS devices. The first being is that there is a significant current and voltage increase before the device snapbacks to a lower voltage. This implies that the parasitic bipolar transistor does not turn on until the applied voltage is significantly higher than the breakdown voltage of the Drain/BG junction. Another difference is that the trigger voltage (Vt1) has different dependence on the TLP pulse rise time. In our observation, the LDMOS Vt1 did not show a drastic change with the TLP pulse rise time.

This characteristic of the LDMOS is an artifact of its special device structure; namely the non-uniform channel doping and the lightly doped N-Well/Deep N-WN-Well drift region. In this device, the breakdown starts in the depletion zone of the N-Well-P-Well junction at high Drain-Source bias. As the Drain bias increases a significant voltage drop occurs across the depleted drift region. Consequently, the depletion region expands reaching the highly doped N+ Drain region. The conductivity of the N-Well region is subsequently modulated by the generated electron hole pairs and the impact ionization region shifts towards the N+/N-Well interface. As a result, the parasitic bipolar transistor turns on and the device exhibits snapback. The mechanism has been investigated by TCAD simulations in [3, 9].. As a result, there is a significant voltage offset between N-Well-P-Well junction breakdown and trigger voltage in the case of the LDMOS.

In the case of a thyristor-type high voltage clamp, the device can be decoupled into two separate bipolar transistors, namely a PNP and a NPN. This clamp device works in snapback mode as a result of the positive feedback triggered by the avalanche current in the Base/Collector junction of the NPN or the PNP transistors in which one BJT activates first and then subsequently turns on the second one. For HV clamps, atypical features important to

effective ESD protection include coupled bipolar action, customizable trigger and holding voltages. The trigger voltage is more determined by the first BJT while the second one has bigger impact on the holding voltage. The weaker the second BJT is, the higher the holding voltage.

3.2 Snapback Model for LDMOS

The BSIM model, which is normally used to describe LV MOS devices, is no longer adequate for LDMOS devices. Instead, MOS model MOS20 [10] is used to model LDMOS devices. MOS20 combines the MOSFET-operation of the channel region with that of the drift region under the thin gate oxide in a high-voltage MOS device. The main model equations are based on surface-potential formulations and valid over all operation regimes. The model includes important physical effects such as mobility reduction, velocity saturation, drain-induced barrier lowering, static feedback, channel length modulation and impact ionization. It only provides a model for the intrinsic MOSFET part. Junction charges, junction leakage currents, and parasitic bipolar transistors are not included.
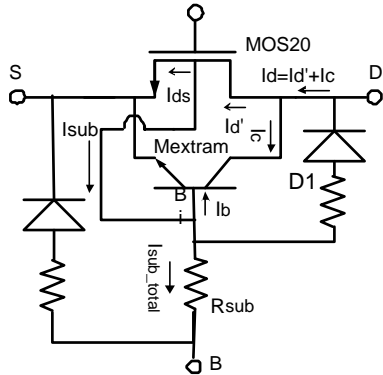
Fig. 3. Simplified Equivalent Circuit Schematic of the ESD model for LDMOS.

The LDMOS model under normal operation is a sub-circuit that consists of the main MOS component modeled by MOS20 and two diodes added respectively between the Drain and BG and between the Drain and Substrate. For the ESD snapback model, a NPN component for the parasitic Drain/BG/Source bipolar transistor and a resistor for the back gate resistance are added to the standard macro model. Fig. 3 shows the high-level schematic representation of the model. The BJT is modeled by an Analog Devices advanced proprietary model that is very similar to Mextram. The avalanche current, the key physical effect that causes snapback, is intrinsically included in the BJT model. The initial breakdown before the snapback is represented by the diode D1.

3.3 Snapback Model for HV Clamp

To model the snapback effect in the thyristor-like high voltage clamp, the compact model needs to include the NPN, the PNP, as well as account for the avalanche effect and the resistive voltage drops between the Emitter and Base nodes in the NPN and PNP respectively. The clamp is modeled by incorporating an advanced BJT model with two resistors. Fig. 4 shows a high level schematic representation of this model. A Mextram-like advanced BJT model is used. Besides the main NPN component, the model includes the parasitic PNP associated with substrate and the avalanche current between the Collector and Base. The BJT model includes both the avalanche and junction capacitance. The clamp model as shown in Fig.4 also can be implemented by one NPN and one PNP.
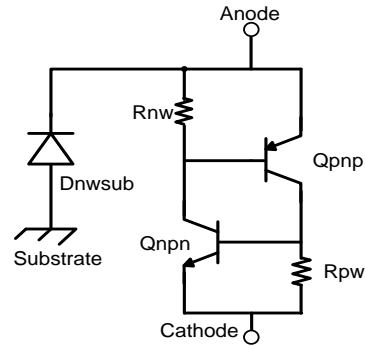
Fig. 4. Simplified Equivalent Circuit Schematic of the ESD model for the thyristor-like high voltage clamp.

4 MEASUREMENT AND SIMULATION

Simulation of the proposed high voltage LDMOS and HV clamp models has been verified against measurement data. Measurements were performed on devices built on 0.18μm and 0.35μm BCDMOS process technologies.

The snapback effect was measured using a Barth Model 4002 TLP tester. The TLP pulse width used was 100ns. The values of the rise time of the TLP pulses were 200ps, 2ns, and 10ns, respectively. Very fast TLP (VFTLP) testing was also performed with pulse widths of 10ns, 5ns, and 2ns, using a Barth Model 4012 VF TLP system.
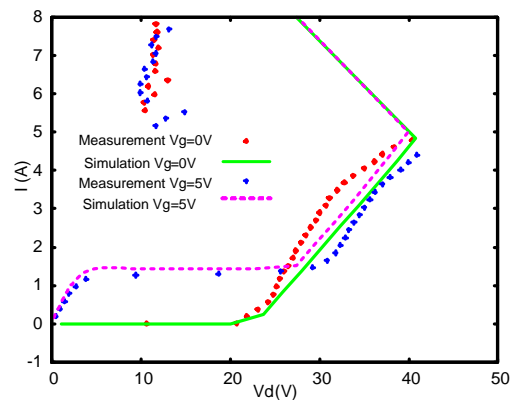
Fig. 5. TLP playback (t_{rise}=10ns) of a large LDMOS (W=5000um) device for different gate bias voltages

Fig. 5 shows the measured and simulated results for a large LDMOS device (W=5000μm) in the 0.35μm process for different gate bias voltages. Fig.6 gives the results of a small LDMOS device (W=200μm) in the same process for

different TLP pulse rise times. The snapback trigger voltage is independent from the rise time. The simulation matches the measurement well before snapback. After snapback, the devices were damaged, as indicated by leakage test. Similar results were also achieved in the 0.18μm process.

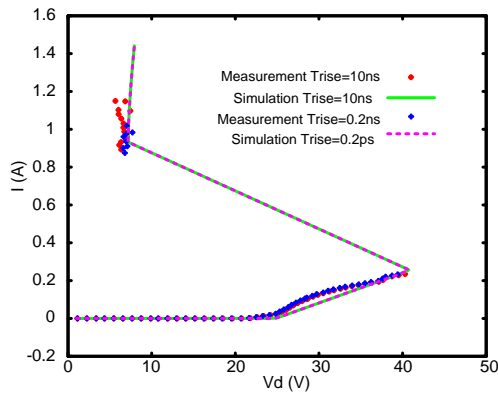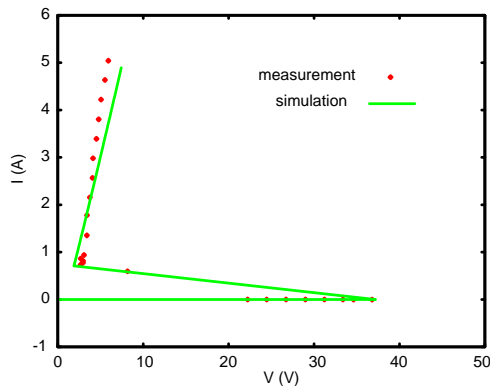Fig. 6. TLP playback of a small LDMOS (W=200μm) device for different TLP rise times (t_{rise}=200ps, 10ns)

Fig. 7. TLP playback (t_{rise}=10ns) of a low holding voltage clamp in the 0.35μm process

Fig. 7 and Fig. 8 show the results for the high voltage protection clamps in the 0.35 μm and a new set of high holding voltage in the 0.18 μm processes, respectively. The simulation of these high voltage clamp devices agree well with TLP measurements for both low and high holding voltage devices. Unlike the LDMOS devices, the trgger voltages of the clamps decrease as the TLP pulse rise is reduced. This effect is due to displace current (dV/dt) through the Collector/Base junction capacitance.

The simulation of very fastTLP (VFTLP) stress against measurement has also been carried out and agreement between measurements and simulations has also been achieved. This means that these high voltage clamps modeling approach works well to simulate the transient and quasi-static TLP measurements for multiple high voltage devices types when operated under different stress conditions. The new model enables circuit simulations for predicting ESD performance of mixed-signal high voltage designs prior to manufacturing and diagnosing post-fabrication ESD failures. Test simulation using these HV device models for circuit simulation under HBM (Human Body Model) and HMM (Human Metal Model) ESD events demonstrates it to be critical for the optimum co-design and failure diagnosis.
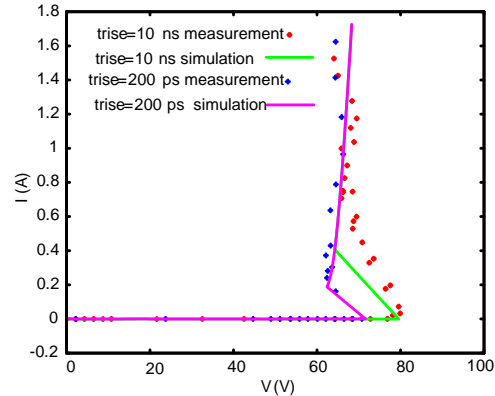

Fig. 8. TLP playback of a high holding voltage clamp in the 0.18μm process for different TLP rise times (t_{rise}=200ps, 10ns)

5 CONCLUSION

Modeling ESD behavior of high voltage LDMOS and thyristor-like clamp devices using a macro model approach is presented in this paper. The models consist of standard passive and active components without having to use a complex external dependent current source. The simplicity of this modeling approach facilitates the method easy implementation. The simulation results have shown agreement with measured TLP and VFTLP data as performed on 0.18μm and 0.35μm BCDMOS process technologies.

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