Process Variability Modeling for VLSI Circuit Simulation

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ABSTRACT

This paper presents a systematic methodology to develop statistical compact MOS models for advanced VLSI circuit simulation. Process variability in advanced CMOS technologies imposes a serious challenge for computer-aided VLSI circuit design. Therefore, statistical compact model has become indispensable for realistic assessment of the impact of random process variability on advanced VLSI circuit performance. This paper describes the major parameter set causing local and global process variability in nanoscale CMOS devices and presents a methodology to generate simplified statistical compact MOS models for VLSI circuit simulation.

Keywords: MOS compact models, process variability, local variations, global variations, modeling process variability, statistical compact model.

1 INTRODUCTION

In advanced CMOS technologies, process variability severely impacts delay and power variability in VLSI devices, circuits, and chips [1]–[6]. Typically, process variability includes local or intra-die variability and global or inter-die variability [3]–[6]. Local variability is the parametric fluctuations between identically designed MOSFETs within a short distance [3]–[6]. And, global variability refers to such fluctuations between identical MOSFETs separated by a longer distance or fabricated at different time [3]–[6]. Local variability is within a die, whereas global variability is from die to die, wafer to wafer, or lot to lot. Global variability causes a shift in the mean value of sensitive design parameters including channel length (L), channel width (W), layer thickness, resistivity, doping concentration (N_A), and body effect (K) [3]–[5]. Local variability introduces systematic variability in patterning and random variability in patterns [3]–[5]. Systematic variability includes the variability caused by optical-proximity correction, phase-shift masking, layout-induced strain, and well-proximity effects. Random variability includes random discrete doping (RDD), line-edge roughness (LER), line-width roughness (LWR), interface roughness, gate-oxide thickness (T_{ox}) variation, poly-silicon granularity, and high-k dielectric morphology with metal gates [3]–[5]. Systematic variability can be addressed through layout design and more controlled resolution-enhancement techniques. However, addressing the impact of random variability requires innovative process and circuit design techniques and statistical device models for accurate analysis of VLSI circuits [5], [6]. For technology nodes below 90 nm, the impact of random local variability on circuit performance is becoming increasingly important. The impact of local variability on yield in VLSI circuits such as SRAM necessitates the development of new design techniques. Hence, accurate characterization and modeling of local process variability for circuit simulations are imperative to accurately predict yield and evaluate the benefits of these new circuit design techniques. To achieve accurate circuit simulation results, local variability must be accurately modeled at the process temperature and voltage conditions that most affect the circuit yield. Similarly, global process variability must, also, be accurately characterized and modeled to accurately predict across the chip performance fluctuations in advanced VLSI circuits.

Traditionally, VLSI circuits are optimized using foundry supplied fixed corner models. Due to increasing amount of process variability constraints, a circuit optimized using such methodologies is more susceptible to random fluctuations. Therefore, statistical design methodologies have become indispensable for modern VLSI circuit design. And, statistical compact model addressing the impact of both local and global random variability is crucial for computer-aided design and analysis of advanced VLSI circuits. Statistical compact models are required for yield prediction during circuit simulations to mitigate the risk of yield loss in advanced VLSI circuits.

The objective of this paper is to present a systematic methodology to develop statistical compact MOS models for accurate design and analysis of advanced VLSI circuits. In order to achieve this goal, first of all, the major parameter set causing local and global process variability is determined. Then the procedure to model the local and global process variability is described. Finally, methodology to generate statistical compact MOS models to account for the impact of process variability in VLSI circuits is presented.

2 CRITICAL DEVICE PARAMETERS

In order to generate compact variability model for circuit simulation, first of all, the critical device parameters causing process variability are determined.

2.1 Local Process Variability

Local process variability or mismatch between identically designed transistors is caused by microscopic process that makes every transistor different from its neighbors. As a result, a device parameter P can be

considered as consisting of a fixed component P_0 and a randomly varying component P' resulting in different values of P for closely apart identical paired-transistors. The actual mismatch in P between identical-paired transistors is defined by ΔP. For a large number of samples, ΔP converges to a Gaussian distribution. Now, if P_i is the model parameter causing mismatch ΔP_i between the paired-transistors, then the variance of relative drain current, I_{DS} mismatch between paired-transistors is given by [7]:

$$\sigma^2_{\Delta I_{DS}/I_{DS}} = \sum_{i=1}^{N}\left(\frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial P_i}\right)^2 \sigma^2_{\Delta P_i} + \frac{2}{I^2_{DS}}\sum_{i=1}^{n}\frac{\partial I_{DS}}{\partial P_i}\frac{\partial I_{DS}}{\partial P_{i+1}}\rho\left(\Delta P_i, \Delta P_{i+1}\right) \quad (1)$$

where N is the number of randomly varying device parameters contributing to I_{DS} mismatch, $\sigma_{\Delta P_i}$ is the standard deviation in ΔP_i and $\rho\left(\Delta P_i, \Delta P_{i+1}\right)$ is the correlation between ΔP_i and ΔP_{i+1}. In order to model I_{DS} mismatch between paired-transistors, we need to compute the randomly varying device parameters ΔP_i. For any regional compact MOS models, the simplified expression for I_{DS} is given by [8]:

$$I_{DS} \cong \begin{cases} \left(\frac{W}{L}\right) I_0 \exp\left(\frac{V_{GS}-V_{TH}}{nkT}\right)\left[1-\exp\left(-\frac{V_{DS}}{kT}\right)\right]; & V_{GS} < V_{TH} \\ \left(\frac{W}{L}\right)\mu_{eff} C_{ox}\left(V_{GS}-V_{TH}-\frac{V_{DS}}{2}\right)V_{DS}; & V_{GS} > V_{TH} \end{cases} \quad (2)$$

where I_0, W, L, μ_{eff}, C_{ox}, and V_{TH}, are the and sub-threshold current, channel width, channel length, inversion-layer mobility, gate oxide capacitance, and threshold voltage, respectively; V_{GS} and V_{DS} are gate and drain voltage, respectively; and n, k, and T are the ideality factor of subthreshold slope, Boltzmann constant, and ambient temperature, respectively.

From (2), we find that the value of I_{DS} depends on the parameter set $\left\{V_{TH}, W, L, C_{ox}, \mu_{eff}, V_{GS}, V_{DS}\right\}$. Considering the mismatch due to process variations only, ΔP_i in (1) represents ΔV_{TH}, ΔW, ΔL, ΔT_{ox}, and $\Delta\mu_{eff}$. Again, V_{TH} can be expressed as $V_{TH} = \mathrm{f}\left(V_{T0}, K, \phi_S, V_{BS}\right)$, where V_{BS} is the applied bias at the bulk of MOSFETs and $V_{T0} = V_{TH}$ at $V_{BS} = 0$; whereas, K and ϕ_S are the body effect coefficient and channel surface potential, respectively. Here, V_{T0} models the mismatch (ΔI_{DS}) in I_{DS} due to the fluctuations in N_A in the inversion region of MOSFETs; whereas, K models the mismatch in $I_{DS}(V_{BS})$ due to the fluctuations in N_A in the depletion region under the gate. We know that $K = \mathrm{f}(N_A, V_{BS})$ and with the change in the value of V_{BS}, the width of the depletion layer under the gate changes. As a result, the amount of bulk charge, qN_A changes with the changes in V_{BS} as shown in Fig. 1 for a graded-retrograde (GR) channel doping profile [9]; where q is the electronic charge. Thus, the fluctuations in the vertical channel doping under the gate due to process variability contribute to the mismatch in $I_{DS}(V_{BS})$. Hence, $I_{DS}(V_{BS})$ mismatch between identical paired-transistors due to fluctuations in the vertical channel doping concentration must be modeled by K. Thus, the set of major device parameters contributing to the mismatch between identically designed transistors within a chip is $\left\{V_{T0}, W, L, T_{ox}, \mu_{eff}, K\right\}$. Here, $\Delta VT0$ models ΔI_{DS} due to RDD, ΔW and ΔL models ΔI_{DS} due to LER and LWR, ΔT_{ox} models ΔI_{DS} due to oxide thickness fluctuations, $\Delta\mu_{eff}$ models ΔI_{DS} due to mobility fluctuations caused by surface roughness and remote roughness scattering, and K models ΔI_{DS} due to fluctuations in the vertical channel doping concentration. Therefore, in order to model mismatch in VLSI circuits, the fluctuations in the critical device parameters due to microscopic process variations must be modeled accurately.

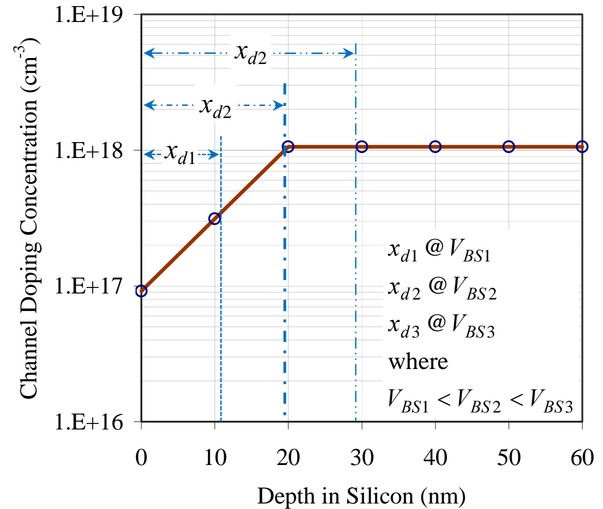

Fig. 1. A typical MOSFET channel doping profile from the silicon/silicon-dioxide interface at depth = 0 into the substrate; x_{d1}, x_{d2}, and x_{d3} are the depletion width due to the applied bias V_{BS1}, V_{BS2}, and V_{BS3}, respectively causing $V_{TH}(V_{BS})$ variations due to the fluctuations in vertical N_A.

2.2 Global Process Variability

Global process variability is caused by non-uniform processing temperature as well as fluctuations of implant doses across wafers and relative location of devices. The global variation shifts the average value of device performance. From (2), the global fluctuations, ΔI_{DS} can be described by the parameter set $\left\{V_{TH}, W, L, T_{ox}, \mu_{eff}\right\}$. In addition, ΔI_{DS} due to the fluctuations in the source-drain (S/D) implant dose across wafers can be modeled by variations in the S/D series resistance, R_{DS}.

Again, the gate delay, $\tau_{pd} \propto C_{load}$, where C_{load} is the load capacitance. Therefore, for accurate simulation of digital circuits, across the chip fluctuations in MOSFET gate capacitance (C_g) along with that in S/D junction capacitance (C_J) must be accurately modeled. The fluctuation in C_g is modeled by fluctuations in the gate overlap capacitance (C_{ov}) whereas, that in C_J is modeled by the area as well as S/D sidewall capacitances. For example, in BSIM4 compact MOS model, the fluctuations in the transient performance can be primarily described by the parameter set $\{C_{ov}, C_J\}$. Therefore, the set of major model parameters to account for the global variability in MOSFET devices is $\{V_{TH}, W, L, T_{ox}, \mu_{eff}, C_{ov}, C_j\}$.

3 CORNER MODEL PARAMETERS

3.1 Local Component

In section 2.1, we have described the randomly variable set of device parameters causing mismatch between identically designed transistors as $\{V_{T0}, W, L, T_{ox}, \mu_{eff}, K\}$. The corresponding BSIM4 MOS model parameters are $\{V_{T0}, XW, XL, T_{ox}, U0, K1\}$ [10]; where, XW and XL are the channel width and length offset parameters due to masking and photolithography, respectively and account for the mismatch due to LER and LWR; whereas, $U0$ and $K1$ accounts for the fluctuations in μ_{eff} and N_A with V_{BS}, respectively. The mismatch, $\Delta P_{i,mismatch}$ is described by standard normal distributions, $N(0, \sigma)$ where the variance, σ for each variable is calculated from a large number of samples using Pelgrom's law [11] and is described by $\sigma_{\Delta P_i} \cong A_{P_i} / \sqrt{WL}$ where A_{P_i} is a process dependent constant. For example, the variance in $VT0$ is given by:

$$\sigma_{\Delta VT0} \cong \frac{A_{vt}}{\sqrt{WL}} \tag{3}$$

Typically, mismatch $\Delta VT0$, ΔXW, ΔXL, ΔT_{ox}, $\Delta U0$, and $\Delta K1$ are represented by standard normal distributions $N(0,1)$. Therefore, we can show:

$$\Delta P_{i,mismatch} = \sigma_{\Delta P_i} N(0,1) \tag{4}$$

In (4), $\Delta P_{i,mismatch}$ represents fluctuations in P_i due to local process variability and is computed using Monte Carlo (MC) simulation for a large number of samples.

3.2 Global Component

In section 2.2, we have described the critical set of device parameters $\{V_{TH}, XW, XL, T_{ox}, \mu_{eff}, C_{ov}, C_j\}$ causing global process variability. The corresponding set of BSIM4 model parameters is {*VT0, XW, XL, TOX, U0, K1, RDSW, CGSO, CGDO, CGSL, CGDL, CJS, CJD, CJSWS, CJSWD, CJSWGS, CJSWGD*}. Here, {*CGSO*, *CGDO*, *CGSL*, *CGDL*} defines C_{ov}; {*CJS*, *CJD*} defines S/D junction area capacitance; and {*CJSWS*, *CJSWD*, *CJSWGS*, *CJSWGD*} defines S/D junction sidewall capacitance. For MC statistical modeling, the global variance, $\Delta P_{i,global}$ is, also, described by normal distribution, $N(0, \sigma)$. Typically, $\sigma \approx 3$ and is extracted from the statistical distributions of electrical test (ET) data for P_i measured from multiple dies, wafers, and lots over a period of time [5]. The variance in model parameter P_i due to global process variability can be modeled by:

$$\Delta P_{i,global} \cong \begin{cases} \sigma_i . N(0,3); & \text{for MC corner model} \\ \sigma_i ; & \text{for fixed corner model} \end{cases} \tag{5}$$

In (5), $\Delta P_{i,global}$ represents the fluctuations in P_i due to global process variability. Thus, the model parameter P_i due to both local and global process variability is given by:

$$P_i = P_{i0} + \Delta P_{i,mismatch} + \Delta P_{i,global} \tag{6}$$

where, P_{i0} is the value of the nominal model parameter and is extracted from the golden die of the golden wafer that represents the target device specifications of the target technology.

3.3 Corner Parameter Extraction

The local and global components of ΔP_i given by (4) and (5), respectively are extracted from ET data as shown in Fig. 2.

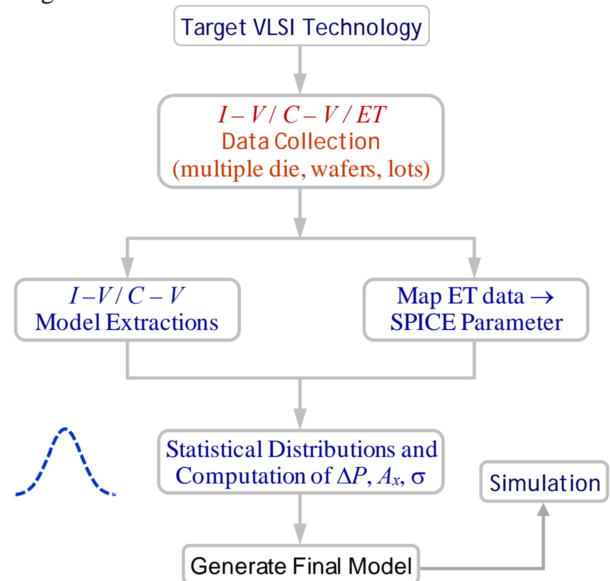

Fig. 2. Basic approach for statistical compact modeling. The database includes electrical device characteristics and production ET data. (The bell-shaped curve represents a typical ET data distribution).

In the basic modeling approach, ET data are collected from multiple devices, wafers, and lots over a long period of time. $I-V$ and $C-V$ characteristics can be used to

extract corner model parameters. However, this approach is time-consuming and therefore, ET data are, typically, used to generate statistical models. In the case of a new technology generation, the production data for statistical modeling is limited; therefore, systematic technology CAD (TCAD)-based process variability data can be generated for statistical corner modeling [12]–[15].

4 MODEL GENERATION

4.1 MC Statistical Model

Equation (6) is used to generate the corner models of the target technology. For MC statistical corner modeling, normal distribution is used to determine the value of σ for each randomly varying parameter described in section 3. From the statistical distribution of ET data, 3σ value is used to account for across the chip variations; whereas, 1σ value is used for mismatch modeling. Finally, (6) is implemented to generate corner models to simulate process variability of the target CMOS technology. Fig. 3 shows the random distributions of NMOS and PMOS $VT0$ and I_{DSAT} data obtained around their respective typical (TT) values as obtained by MC statistical model.

4.2 Fixed Corner with Mismatch Model

The MC simulation using both local and global random variables, described in section 3, is computationally intensive for advanced VLSI circuit simulation. Therefore, fixed corner models along with MC mismatch model can be efficiently used to analyze the advanced VLSI circuits. MC mismatch addresses the stochastic variations between paired-transistors; whereas, fixed corner model with appropriate value of σ_i can be used to address across the chip variations at the lower and upper boundaries [5]. Equation (6) is used to generate the fixed corner parameters of the target technology. A fixed value of $3 \le \sigma \le 6$ is used to account for global process variability. The MC mismatch is performed at the upper and boundaries of fixed corner model [5] as shown in Fig. 4.

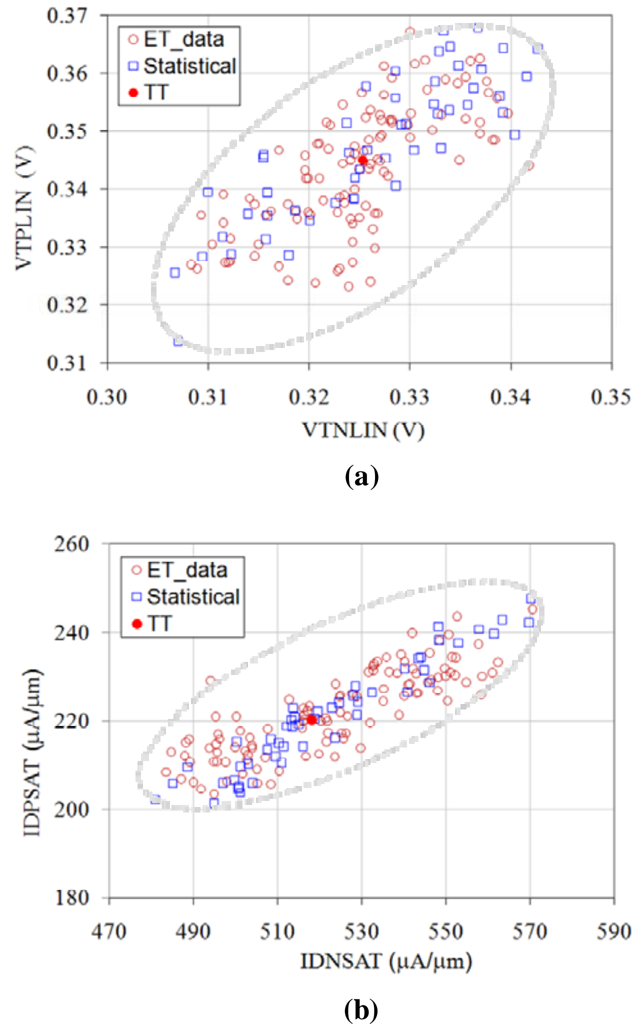

Fig. 3. Production data distribution, along with simulation data generated from the corresponding statistical MOSFET models: (a) V_{TNLIN} vs. V_{TPLIN} and (b) I_{DNSAT} vs. I_{DPSAT}. The models appropriately include the spread in electrical test ET data due to process variability; TT represents typical values of NMOS and PMOS model parameters.

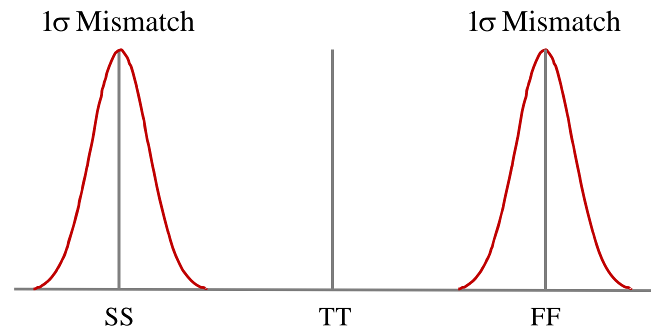

Fig. 4. Mismatch simulation around SS and FF corners to account for random process variability using fixed corner models; SS denotes slow NMOS and slow PMOS devices; FF represents fast NMOS and fast PMOS devices.

5 CONCLUSION

Process variability in advanced CMOS technologies imposes a serious challenge to advanced VLSI circuit design. Therefore, statistical corner models are extremely important for realistically assessing how process variability impacts circuit performance. In this work, we have generated statistical models and used them in rudimentary digital-circuit analysis to investigate delay variation in response to process variability. The simulation data shows that this statistical-modeling approach enables realistic prediction of the standard deviations of circuit performance and allows for tracking circuit performance due to process variability by monitoring ET data.

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