Chip Scale Focussed Electron Beam Induced Etching of a Silicon Nitride Membrane with Unique Beam Writing Strategies

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ABSTRACT

Many instances of focused beam induced processing have been reported in the literature, mostly concerning the use of ion beams for milling and patterning of materials [1-5]. FEBIP, or focused electron beam induced processing has received more attention with the last decade, though most of the work has been in the area of electron beam induced deposition (EBID). FEBIP has received new attention recently in the research community, one area being in the fabrication of nanopores in membranes for use in biosensing and nano-electronic applications. In this paper, we present our work using FEBIP to etch nanopores in silicon nitride membranes. We have utilized a vector-steered beam approach to reduce effects of charging of the membrane and of gas depletion in the etched region. We also discuss further ways to refine and automate the processing and the challenges to bring it to a wafer-level process.

Keywords: FEBIP, EBIE, electron beam, nanopores

1 INTRODUCTION

One of the more difficult challenges in the field of nanotechnology is the ability of the user to modify materials or structures on the nanometer scale. The continual scaling of semiconductor devices and the nanometer length scale characteristic of many biological processes has made this ability a necessity. One interesting area of structure development for devices has been in the creation of nanopores in membranes for the analysis of molecules in bio-sensing applications [6-8]. The literature references several techniques used in the formation of nanopores, including the use of high energy electron beams and focussed ion beams [9-12].

The use of FEBIP techniques for nanopore creation in silicon nitride membranes has recently been explored [13]. The FEBIP technique offers some advantages over the other nanofabrication techniques such as focussed ion beam processing or electron beam lithography.Some of the advantages include the reduced substrate contamination and damage in an electron beam process (*i.e.*, there is no gallium implantation or sputtering effects, as with focussed ion beam processes), high resolution resulting from the localization of the electron beam, and reduced process complexity (*i.e.*, there is no resist or hard mask as with electron beam lithography).

We explore the use of a vector-scanned electron beam, as compared to a steady-spot mode beam. This approach helps to reduce the effects of charge build-up in the membrane which can result in beam position instability during the patterning, as well as reducing the effects from gas depletion in the etched region. We briefly discuss ways to improve the nanopore creation and the challenges faced in attempting to bring the process to a wafer level.

2 PATTERNING OF THE NANOPORES

The set-up used to pattern the nanopores is shown in Figure 1. Silicon nitride membranes[1], 50 and 200 nm in thickness, were loaded into the chamber of an electron beam lithography system[2] with a gas injection system for FEBIE. Silicon nitride was chosen because of its relative inertness to both the electron beam and to the precursor gas, xenon difluoride (XeF_2). Initially, work was done on the 50 nm thick membranes to determine the best suited parameters for

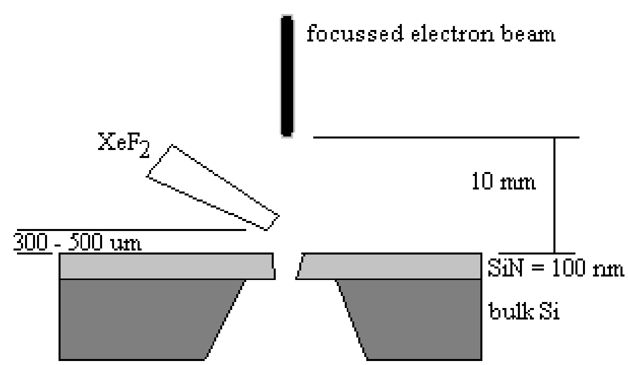

Figure 1: Schematic of the EBIE set-up used to pattern the nanopores.

etching the nanopores. System parameters (2 ≤ EHT ≤ 10 kV, 150 ≤ beam current ≤ 190 pA, 8E-6 ≤ system vacuum ≤

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2E-5 mbar) were varied to optimize the etching rate, nanopore shape, and to minimize charging effects. The XeF_2 was transported to the sample surface from the precursor reservoir via capillary lines and a nozzle block. The capillary lines and nozzle block were heated in increasing temperature to allow the gas to flow rapidly to the coincident point on the sample surface. During the course of this work, the electron beam was used in spot mode (e.g. held stationary), and also directed in a circular motion utilizing the vector-based patterning of the Raith *e_LiNE*. The dwelltime of the beam was also varied to minimize charge build-up and redeposition of material.

3 NANOPORE TOPOGRAHY

The nanopores were inspected using the *e_LiNE* system's scanning electron miscroscope mode. In order to ensure that no further etching would occur during imaging from residual XeF2 in the chamber, a plasma clean was performed on the chamber. Figure 2 shows typical result of a nanopore patterned by holding the electron beam in spot mode. It is evident that very little etching into the membrane has occurred. There is also clear evidence of drift in the position of the electron beam, a result of charging in the membrane. The electron beam was next scanned in a filled-circle fashion, with the results shown in Figure 3.

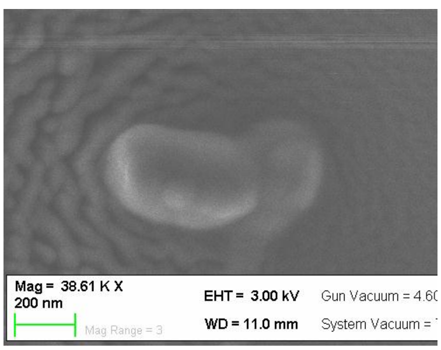

Figure 2: Nanopore patterning with the electron beam in spot mode

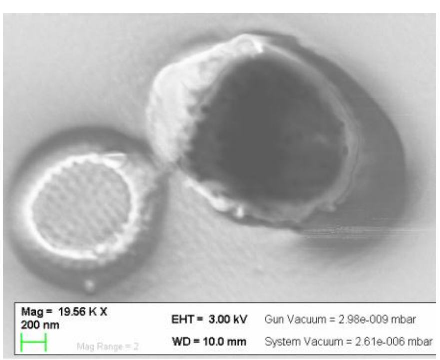

Figure 3: Nanopore patterned by rastering the electron beam in a circle

While the results achieved from patterning the beam in this mode show definite etching into the membrane, it is still clear that there is drift as well as material redeposition taking place during the patterning, with no clear break through the membrane, even after several hours of patterning in this mode.

In an attempt to minimize the effects of beam drift and material redeposition, the beam was directed in a doughnut shape, as illustrated in Figure 4, using the GDSII editor of the *e_LiNE* software suite to draw the pattern. The

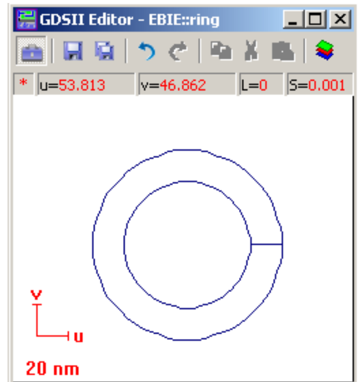

Figure 4: GDSII design of doughnut pattern

width of the ring can be varied which would control the amount of material being removed. Also, the width of the ring can be set to allow for some beam position drift to occur during the process. In our tests, we used 20nm for the width of the ring and the beam position drift was corrected after every 4000 rings. Furthermore, the start/finish points of repeated rings can be rotated to eliminate the possibility of material being left over at a specific angle. In contrast to the first two approaches, this patterning method should reduce the amount of material redeposition as a smaller area of material is actually being removed, thereby increasing throughput of this fabrication process. The center portion of the pore would simply fall away once the membrane has been completely penetrated. Figure 5 shows a sequence of

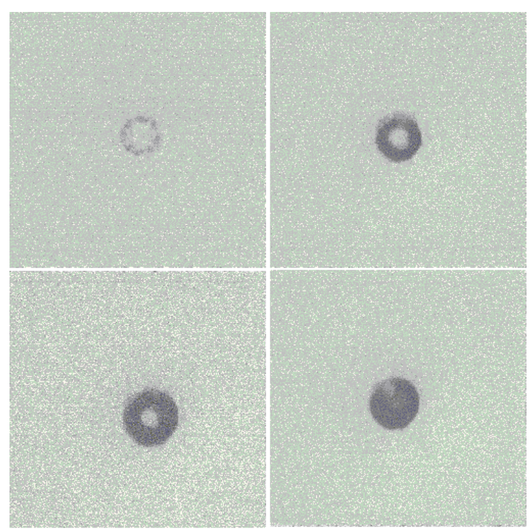

Figure 5: Nanopore patterning by rastering the beam in a doughnut ring shape

images which illustrate the formation of a nanopore using this approach. The process took approximately 10 minutes. Utilizing the highly accurate navigation feature of the laserinterferometer stage, imaging of the nanopores was done on both the front and backside of the membranes to show proof of actually breaking through the membrane and also of the profile achieved, *i.e.* the angle of the sidewalls. Figure 6 shows a front and backside view of one nanopore. The

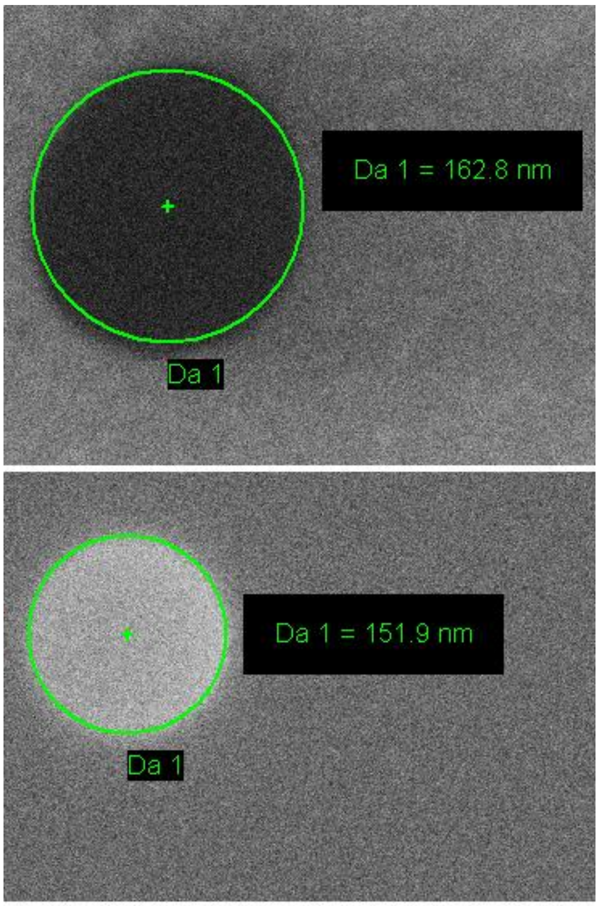

Figure 6: Images of a patterned nanopore - frontside (top) and backside (bottom)

measured dimensions of the nanopore openings indicates that the sidewall angle is almost 90 degrees. In the few instances that we inspected both sides of the membrane, we noticed no material in the proximity of the nanopore, thereby indicating that the material fell away completely and did not redeposit. This somewhat surprising result should be further confirmed and understood.

4 WAFER LEVEL PROCESSING

As the title of this manuscript suggest, the goal of this work was to use FEBIP to pattern nanopores on multiple silicon nitride membranes, *i.e.* at a wafer and "chip" level[3]. The same issues encountered with the patterning presented thus far (beam drift as a result of charging, reduction of redeposition), and in addition sample alignment and registration to each membrane, need to be addressed. A membrane window array[4] containing 49, 100 nm thick, silicon nitride membranes is commercially available and could be used for wafer level nanopore fabrication.

Wafer and chip registration and navigation is a critical issue for processing at the wafer level. The *e_LiNE* system has a laser-interferometer stage, with a positioning resolution of 2 nm, which is a prerequisite for this work.

To address the issue of sample registration, EBID (electron beam induced deposition) could be used to pattern alignment marks on the chip without damaging the membranes. These marks would be used to serve multiple purposes: establishment of a coordinate system on the chip to make navigation between the membranes easier, to aid in patterning placement of the nanopores on each membrane, and for drift correction. Figure 7 shows the GDSII layout of the membrane array, with alignment marks added

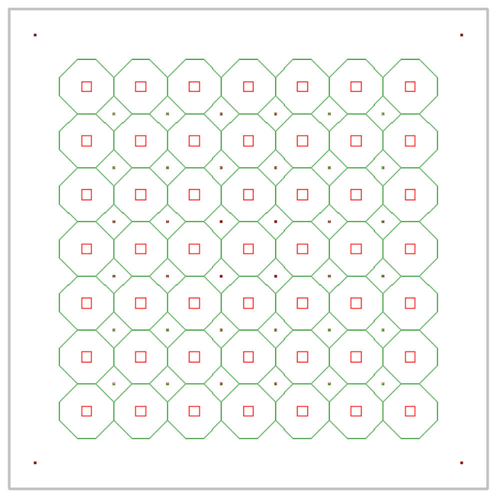

Figure 7: GDSII layout design of the membrane window array

in the four corners and in between each of the individual membrane die. Figure 8 shows the alignment mark design and image of a typical mark.

[3] At the time of this manuscript preparation, research work was still on-going.
[4] SPI Supplies, 569 East Gay Street, West Chester, PA 19381-0656, Ph: 610.436.5400, Fax: 610.436.5755

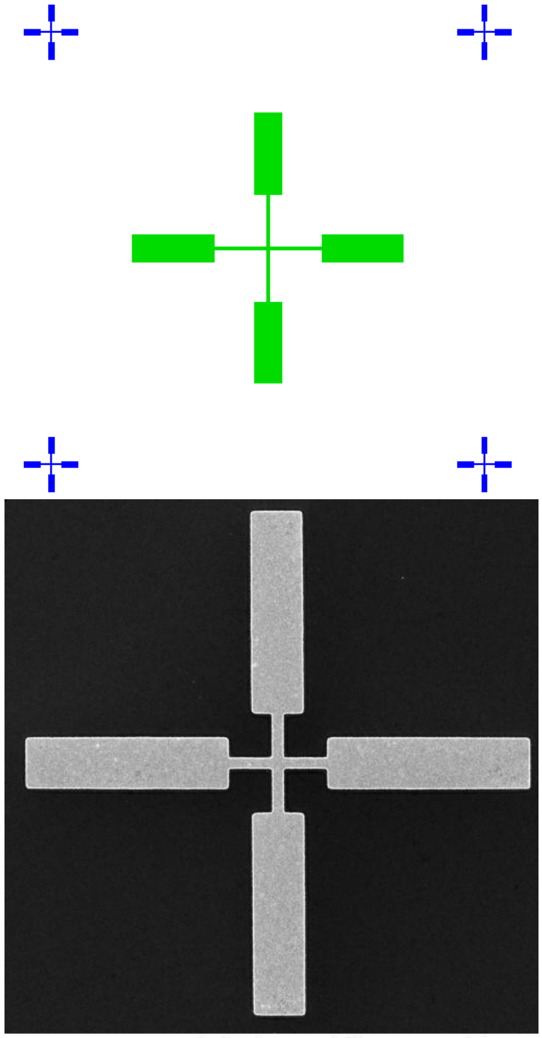

Figure 8: GDSII design layout of alignment mark for registration (top) and image of typical alignment mark (bottom)

An additional desire in the processing sequence is to automate the patterning of the nanopores on each membrane, instead of manually driving to each die, patterning, then moving to the next die and repeating. The alignment marks could also be used to aid in adjusting the coordinate system after driving and calibration of the beam deflection. The automated height sensing apparatus of the *e_LiNE* system could be used to keep the membrane in focus. Using a combination of macro and script commands, this process could be automated to pattern nanopores across multiple die without user interaction.

5 CONCLUSION

We have demonstrated the fabrication of nanopores on silicon nitride membranes using a vector-scanning electron beam lithography system. Utilizing a ring-shaped pattern helped to reduce the redeposition of material and to create precise, uniform nanopores. Work is ongoing with regards to patterning of nanopores on a wafer level and automating the process through the use of alignment and registration marks.

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