A Novel Silicon-based Wideband Nano Switch For RF Applications

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ABSTRACT

This paper presents a silicon-based wideband RF nano switch. The nano switch is fabricated on a tri-layer high resistivity silicon substrate using surface micromachining approach. Electron beam lithography (EBL) technique is adopted to define patterns. IC compatible deposition process is used to construct the metal structures. Silicon-based NEMS switch fabricated by IC compatible process can lead to a high potential of CMOS circuits integration to perform a cost effective system-on-a-chip solution. Details of the fabrication process and fabrication challenge optimizations are discussed in the paper. Simulation and measurement results along with analytical discussions are also presented.

Keywords: cantilever beams, CMOS integration, electron beam lithography, RF NEMS, nano switch, wideband.

1 INTRODUCTION

Future wireless communication system requires miniaturization, performance improvement, and ideally low power consumption. Complementary Metal Oxide Semiconductor (CMOS) devices have been increasingly implemented in digital and analogue devices for high frequency applications. CMOS devices provide a cost effective commercial solution in bulk productions. However during continually scaling the CMOS dimensions, challenges such as power dissipation, parasitic leakage current and short-channel effects are encountered [1]. Micro-Electro-Mechanical-Systems (MEMS) switches have been recently proposed as one of the promising technologies to partially replace the semiconductor counterparts. RF MEMS switches demonstrate advanced performances in terms of isolation, insertion loss, power consumption and size, which are desired in advance wireless communication system [2]. The emerging Nano-Electro-Mechanical-Systems (NEMS) technology is expected to inherit the advantage of RF MEMS and potentially enable revolutionary advances in future wireless communication.

NEMS devices are defined to have a characteristic length scale below 1μm (most strictly, 1-100nm) [3]. Two major perspectives motivate the research of RF NEMS switches: from electromagnetic aspect, a switch with reduced dimensions can propagate a smaller wave length corresponds to the switch size, hence to accommodate an associated higher frequency and wider bandwidth. from mechanical aspect, a reduction of the physical dimensions can theoretically lead to a reduction of switch actuation voltage, as well as an increasement of response time and switching frequency [4]. Additionally, switch with dimensional shrinking has reduced parasitic effects, therefore the switch is possible to exhibit good RF performance.

In this paper, the proposed RF nano switch is fabricated by surface micromachining approach. In order to achieve good RF performance, the nano switch is designed and fabricated on a tri-layer silicon wafer constructed with high resistivity <100> orientation silicon, thermal growth oxide and PECVD nitride. The <100> single crystal silicon is an industrial preferred base-material for integrate circuits (IC) and MEMS. For the four metal layers fabrication, standard lift-off process has been used to construct the switch structure. An IC compatible metal deposition process is employed, whereas a mask-less pattern definition process using electron beam lithography (EBL) is introduced. RF NEMS devices implemented according to industry standard materials and IC compatible process have high potential of integrating with CMOS circuits to perform a system-on-a-chip, hence cost effective advance wireless devices can possibly be produced in future.

Extensive studies indicated that bulk micromachining, shallow trench isolation techniques and suspended carbon nanotubes are used to fabricate nano switches mostly for memory applications [5]-[8]. However, very few report showing the developments of NEMS switches for RF applications. To the knowledge of the authors, it is the first time provides a wideband RF nano switch fabricated using surface micromachining technique in this work. The target operation frequency range is 0-50 GHz. In the following sections, RF nano switch design with simulation results are presented. Followed by switch fabrication process description and fabrication challenge optimization. Finally, measurement and results analysis are presented.

2 RF NANO SWITCH DESIGN

Physical model of the RF nano switch is designed based on a series in-line cantilever structure above a coplanar waveguide (CPW). Nano switch dimensions are decided in

considering minimum feature adjustment of fabrication process. Materials selections are trade-offs between high RF performance characteristic, material deposition process compatibility (with standard ICs process) and possibility of CMOS devices integration. CPW structure is employed in the design because of its advantage of accommodating wideband microwave propagation [9].

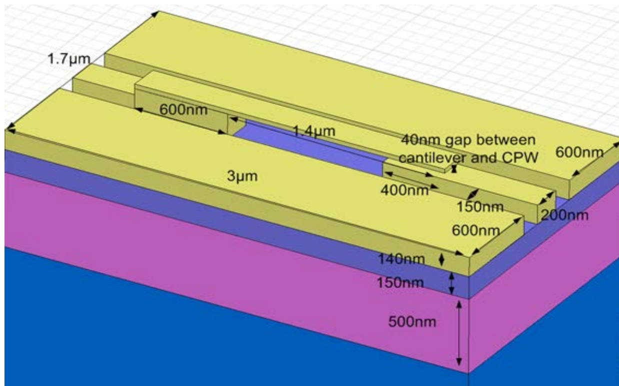

Figure 1: Physical model of the RF nano switch.

Fig.1. illustrates a complete geometry of the RF nano switch. Silicon material with resistivity of 10,000 ohm-cm and dielectric constant (ε) of 11.9 is chosen as substrate. 500nm silicon dioxide buffer layer is placed on top of the silicon; and 150nm silicon nitride is placed above the oxide as insulating layer. A chromium (Cr) based lower electrode with dimensions of 700nm×250nm×40nm is buried between the two dielectric layers. The CPW with ground\signal\ground dimensions of 600nm\200nm\600nm is placed above the nitride. It is built with 100nm gold (Au) on top of 40nm Cr, where the Cr is used as adhesive material. The gap between signal line and ground plane is 150nm for both sides. Finally, a cantilever beam with 1.4μm in length and an anchor with 600nm in length are placed above the signal line. Thickness of the cantilever beam is 30nm, the overlap and gap between beam and signal line are 400nm and 40nm respectively.

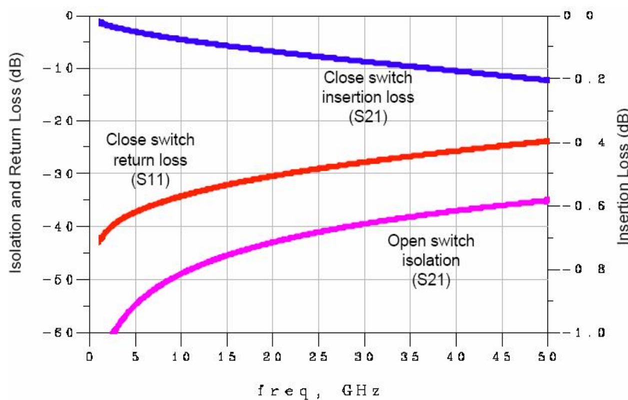

Figure 2: S-parameters simulation using HFSS.

S-parameters of the RF nano switch are simulated by Ansys HFSS. Analysis frequency range is 0-50 GHz, two wave ports are placed at the two ends of CPW signal line. Simulation results for open switch and close switch are illustrated in Fig.2. The simulated isolation, S21 of open switch, is above 35dB; whereas the insertion loss and return loss, S21 and S11 for close switch, exhibit better than 0.2dB and 25dB. The port-to-port simulation results indicate that the proposed RF nano switch has a potential to achieve good RF performance in the interconnection with nano devices that have identical CPW properties.

3 FABRICATION AND PROXIMITY EFFECT OPTIMIZATION

3.1 Fabrication Process Description

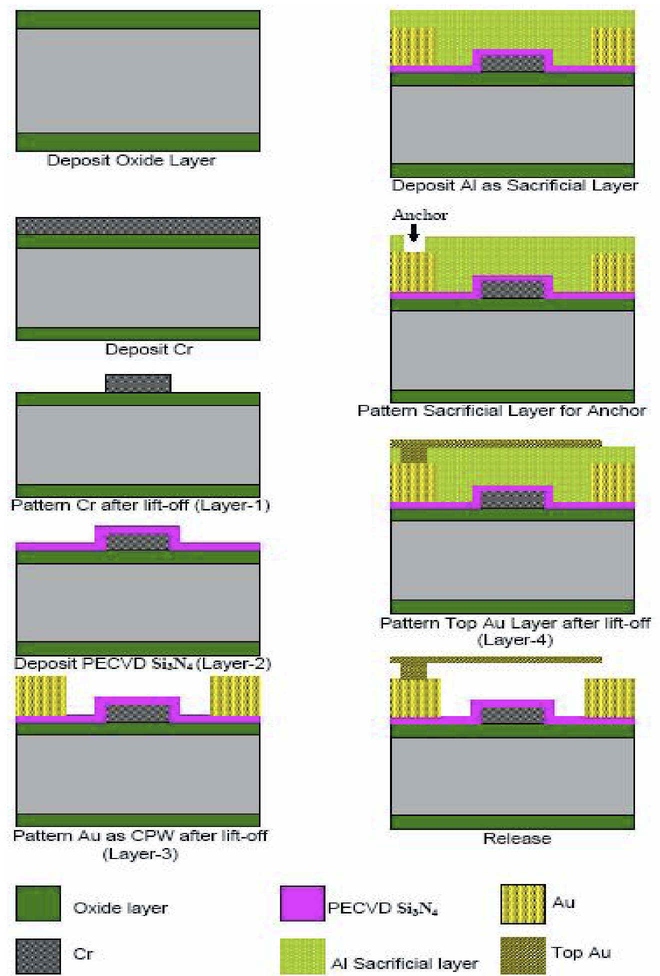

Figure 3: Fabrication process

The RF NEMS switch is developed using surface micromachining approach which consists of four metal layers and two dielectric layers on top of silicon substrate. The metal layers are achieved by standard lift-off process.

Evaporation process is employed for metal deposition and electron beam lithography (EBL) direct writing is introduced as mask-less pattern generator. Polymethyl methacrylate (PMMA) is coated as e-beam sensitive resist for EBL dose exposure. The dielectric layers are silicon nitride by plasma-enhanced chemical vapour deposition (PECVD) and silicon oxide by thermal oxidation. The complete fabrication process is illustrated in Fig.3.

First, a 500nm SiO2 is formed as buffer layer on the silicon substrate. Followed by forming chromium (Cr) based lower electrode and DC bias line using EBL pattern writing at 30KeV, 450μC/cm2 dose with spot 1 and spot 4 respectively. Thickness of this Cr metal layer (Layer-1) is 40nm. Then 150nm silicon nitride is deposited as insulating layer (Layer-2). Above the nitride, a 140nm Au/Cr metal layer (Layer-3) of CPW and bias line is constructed with 100nm Au sitting on top of 40nm Cr. CPW and bias line are patterned by EBL writing at 30KeV, 550μC/cm2 dose with spot 1 and 450μC/cm2 dose with spot 4 respectively. A SEM picture of the fabricated CPW structure with bias line is illustrated in Fig.4.

A 40nm aluminum (Al) is deposited as sacrificial layer and patterned by EBL. The anchor window is created by etching Al. Followed by a 30nm Au cantilever beam deposition with EBL patterned at 30KeV, 450μC/cm2 dose with spot 1. A SEM picture of the fabricated cantilever beam before release process is illustrated in Fig.5.

Finally, the cantilever structure is released by a combination process of wet etch and dry etch using reactive ion etching (RIE). The three-steps etching process begins with wet etch to remove over-left PMMA; followed by anisotropic etch using high power and low pressure plasma; finally, isotropic etching using low power and high pressure plasma is needed to release the structure. A SEM picture of complete view of the RF NEMS switch including bias pads is illustrated in Fig.6.

3.2 Proximity Effect Optimization

Electron beam lithography exposes electron beam on a resist surface during pattern writing. The major challenge encountered using EBL writing is proximity effect.

Proximity effect is caused by non-uniform distribution of exposure or scattering electrons that are received in the exposed area. This effect results in the dose delivered by e-beam not confining with the original shape and leads to a pattern variation. The variation of the exposure dose can be more significant when the defined area becomes relatively smaller.

A dose-shape correction method [10] is adopted to compensate the proximity effect. The principle of the correction method used in the fabrication is that EBL system writes at a constant dose and exposes from high

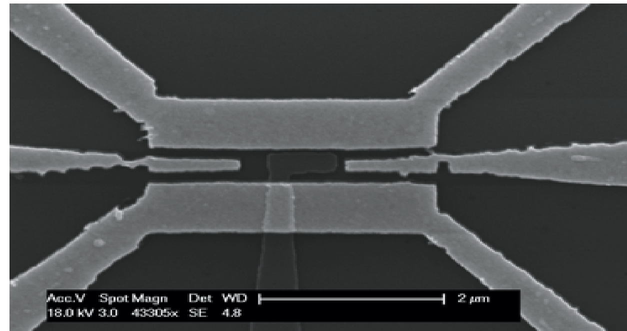

Figure 4: The fabricated CPW structure with bias line.

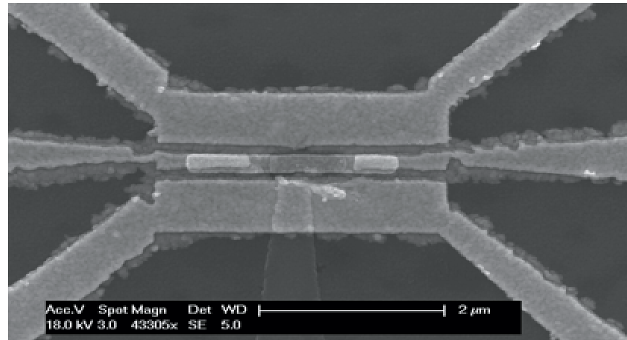

Figure 5: SEM of the deposited cantilever beam.

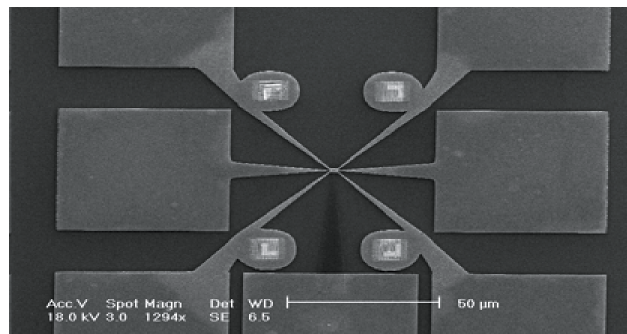

Figure 6: The fabricated CPW structure with bias pads.

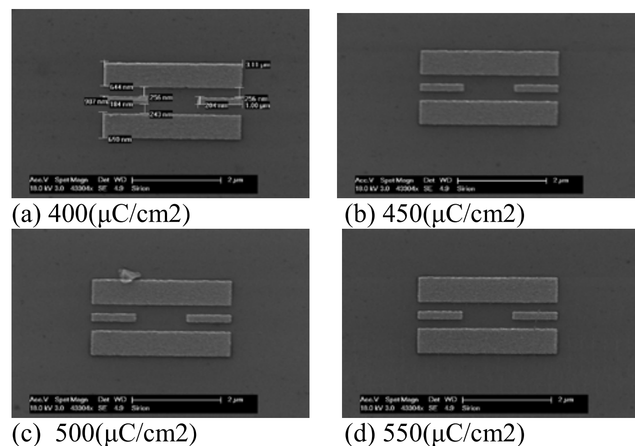

Figure 7: CPW structure under dose-shape correction.

resolution features down to the resolution limit to find the most suitable resolution feature for each dose writing. To achieve a perfect dose for each pattern, varied dose profiles are performed to decide a certain dose for a desired structure with precise dimensions. Finally, different features with different dose profiles are obtained by experimental repetition. A example of dose-share correction for CPW structure is illustrated in Fig.7.

4 MEASUREMENT AND DISCUSSION

A two port on-wafer-measurement has been performed using Agilent Technology PNA E8364C network analyzer and Cascade Microtech probe station. Analysis frequency range is 10MHz-50 GHz.

The measured S-parameters of the open switch is illustrated in Fig.8. The isolation, S21 of open switch, is better than 30 dB for the frequency range of interest. The measured S11 of open switch indicates about 10 dB signal loss in the measurement result.

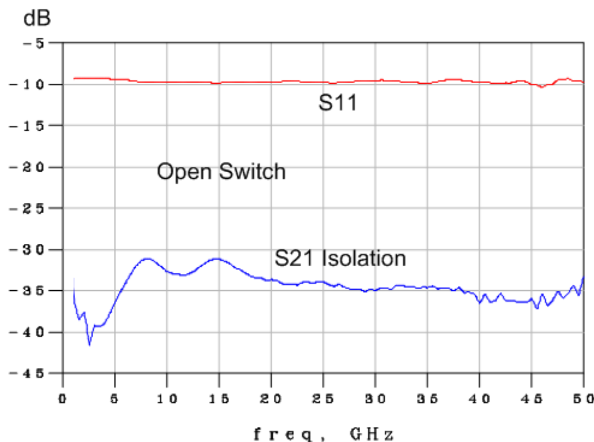

Figure 8: S-parameters measurement for open switch.

First of all, as stated in Section 2, the simulation is performed on the signal line terminals, simulation results indicate the nano device has a potential to achieve good RF performance in the case of coupling same scale nano devices with CPW that has identical properties. While in the measurement, as Fig.6. illustrated, a 200nm width transmission line is directly coupled to the bias pad, the large scale difference of the two joint devices can be one of the reasons that introduce signal loss. A more sophisticate measurement method for RF nano devices including signal path connection design is need to be investigated.

Second, the sacrificial layer is not completely released, this can affect the measurement results. Furthermore, CPW structure on thin dielectric layers can introduce signal leakage, the nano scale CPW characteristic is also need to be insepected.

Finally, the RF nano devices is fabricated on top of silicon which is semi-conductor that electromagnetic field can possibly penetrate into it. In order to achieve a better RF performance, nano scale isolation structure is proposed to be developed in future work to alleviate the signal loss and improve the performance.

5 CONCLUSION

A silicon-based RF nano switch fabricated by surface micromachining approach is presented. The switch was proposed for wideband applications. Simulation results indicate that the designed switch can potentially achieve good RF performance. Electron beam lithography is employed to develop a mask-less fabrication process with precise dimensions definitions. Measurement results indicated that improvements on nano scale signal coupling techniques and improvements on fabrication process for silicon-based low loss RF nano device are need to be investigated in future work.

REFERENCES

[1] J.D. Meindl, Q. Chen and J.A. Davis, "Limits on silicon nanoelectronics for terascale integration," *Proc. of Science Mag.*, vol. 29, pp. 2044-2049, 2001.

[2] V.K. Varadan, K.J. Vinoy and K.A. Jose, *RF MEMS and Their Applications*, New York: J. Wiley & Sons, 2003.

[3] W.C. Crone, "A brief introduction to MEMS and NEMS," *Springer Handbook of Experimental Solid Mechanics*, part A, pp.203-228, 2008.

[4] G.M. Rebeiz, *RF MEMS Theory Design and Technology*, New York: J. Wiley & Sons, 2003.

[5] J.E. Jang, S.N. Cha, Y. Choi, T.P. Butler, D.J. Kang, D.G. Hasko, J.E. Jung, J.M. Kim, and G.A.J, Amaratunga, "Nanoelectromechanical DRAM for ultra large scale integration (ULSI)." *Proc. of IEEE International Electron Devices Meeting (IEDM2005),* pp. 261-264, 2005.

[6] R.L. Badzey and G. Zolfagharkhani, "A controllable nanomechanical memory element," *Appl. Phys. Lett.,* vol. 85, pp. 3587-3589, 2004.

[7] T. Rueckes, K. Kim, E. Joselevich, G.Y. Tseng, C.L. Cheung, and C.M. Lieber, "Carbon nano tube based nonvolatile random access memory for molecular computing." *Proc. of Science Mag.*, vol. 289, pp. 94-97, 2009.

[8] M.S. Kim, W.W. Jang, J.M. Lee, S.M. Kim, E.J. Yun, K. Cho, S.Y. Lee, I.H. Choi, J.B.Y. Yong, and D.W. Kim, "NEMS switch with 30nm thick beam and 20nm thick air gap for high density non volatile memory applications," *Solid State Electronics*, vol. 52, pp. 1578-1583, 2008.

[9] K.F. Harsh, W. Zhang, V.M. Bright and Y. C. Lee, "Flip-Chip assembly for Si based RF MEMS." *Proc. of 12th IEEE Intl. Conf. on Micro Electro Mechanical Systems (MEMS' 99),* pp. 273-278, 1999.

[10] M. Simecek, A. Rosenbusch, T. Ohta and H. Jinbo, "A new approach of e-beam proximity effect correction for high resolution applications," Jour. of Appl. Phys., vol. 37, pp. 6774-6778, 1998.