Compact Models for sub-22nm MOSFETs

Y. S. Chauhan, D. D. Lu, S. Venugopalan, M. A. Karim, A. Niknejad and C. Hu

Department of Electrical Engineering and Computer Science
University of California, Berkeley, CA-94720, yogesh@eecs.berkeley.edu

ABSTRACT

FinFET and UTBSOI (or ETSOI) FET are the two promising multi-gate FET candidates for sub-22nm CMOS technology. The BSIM-CMG and BSIM-IMG are the surface potential based physical compact models for multi-gate MOSFETs. The BSIM-CMG model has been developed to model common symmetric double, triple, quadruple and surround gate MOSFET. The BSIM-IMG model has been developed to model independent double-gate MOSFET capturing threshold voltage variation with back gate bias. Both models have been verified by simulation /measurements and show excellent results for all types of real device effects like SCE, DIBL, mobility degradation, poly depletion, QME etc.

Keywords: BSIM-CMG, BSIM-IMG, FinFET, UTBSOI, MOSFET, Compact Model

1 INTRODUCTION

The continuous scaling of MOSFET channel length and oxide thickness has helped semiconductor industry to increase transistor density and reduce the cost per transistor. The conventional MOSFET structure has hit a limit as the short channel transistor loses gate control, thus increasing static leakage current [1]. Also the oxide thickness scaling has its own limitation as it results in exponential increase in gate tunneling current. Another problem in today's bulk MOSFET is random dopant fluctuation (RDF) in the transistor channel, which increases the variation in the device threshold voltage (V_{th}) [1]. Since the standard deviation of V_{th} due to RDF is inversely proportional to $\sqrt{WL}$, circuits with small device dimensions such as the SRAM cell is especially susceptible to RDF. Thus, a new approach is needed for further scaling in channel length without sacrificing off-state current. The FinFET [2] and and ultra thin body Silicon on Insulator (UTBSOI) FET [3] are the two promising candidates for next generation CMOS as multiple gates surrounding the channel provide significantly better electrostatic control compared to conventional planar MOSFET.

2 MULTI-GATE MOSFET

There are different flavors of multi-gate MOSFETs. Several examples are shown in Fig. 1. The best known example is FinFET [2]. The FinFET consists of a thin silicon body (fin) and a gate wrapping around its top and two sides. The ITRS considers it a candidate to replace planar MOSFETs for the aforementioned benefit of multi-gate transistor and because FinFET is relatively easy to fabricate. FinFETs can be made on either bulk or SOI substrates, creating the bulk FinFET (Fig. 1(a)) or the SOI FinFETs (Fig. 1(b)). In some FinFET processes the oxide hard mask on top of the fin is not removed, creating the double-gate FinFET (Fig. 1(c)). In double-gate FinFETs, the top surface of the fin does not conduct current, whereas in triple-gate FinFETs (Figs. 1(a) and 1(b)), the side surfaces and the top surface all conduct current. Another example of multi-gate MOSFET is the all-around or cylindrical gate device (Fig. 1(d)). It consists of a pillar-like body surrounded by the gate dielectric and the gate. The nanowire MOSFET [4] is an example of all-around gate devices. Depending on the fabrication process, the channel may be vertically [5] or horizontally oriented. Optionally, a FinFET can have two separated gates that are independently biased. This can be achieved by removing the top portion of the gate of a regular FinFET using chemical mechanical polishing, forming the independent double-gate FinFET (Fig. 1(e)) [6].

Independent double-gate MOSFETs (e.g. UTBSOI or ETSOI) may also be made as a planar device [7]. The planar double-gate SOI (Fig. 1(f)) is essentially a planar SOI MOSFET with a thin buried oxide (BOX). A heavily-doped region in silicon under the BOX acts as the back-gate. Unlike front-gate, the back-gate is primarily used for tuning the device's V_{th}. The buried oxide is usually thick such that the back-gate doesn't induce an inversion layer at the back surface. V_{th} tuning can be used to compensate for variability in IC manufacturing from chip-to-chip or even circuit-to-circuit within the same chip, which improves the IC speed and power consumption. It can also be used to dynamically raise or lower V_{th} circuit by circuit within a chip in response to the need for less leakage or more speed. This is a very effective means of managing power consumption. Recently, there has been tremendous progress in improving UTBSOI performance by using very thin silicon body and thin BOX [8].

3 BSIM-CMG and BSIM-IMG Models

It is likely that more than one flavor of multi-gate MOSFETs will be used in production. Therefore the compact model should ideally cover as many of these flavors as pos-

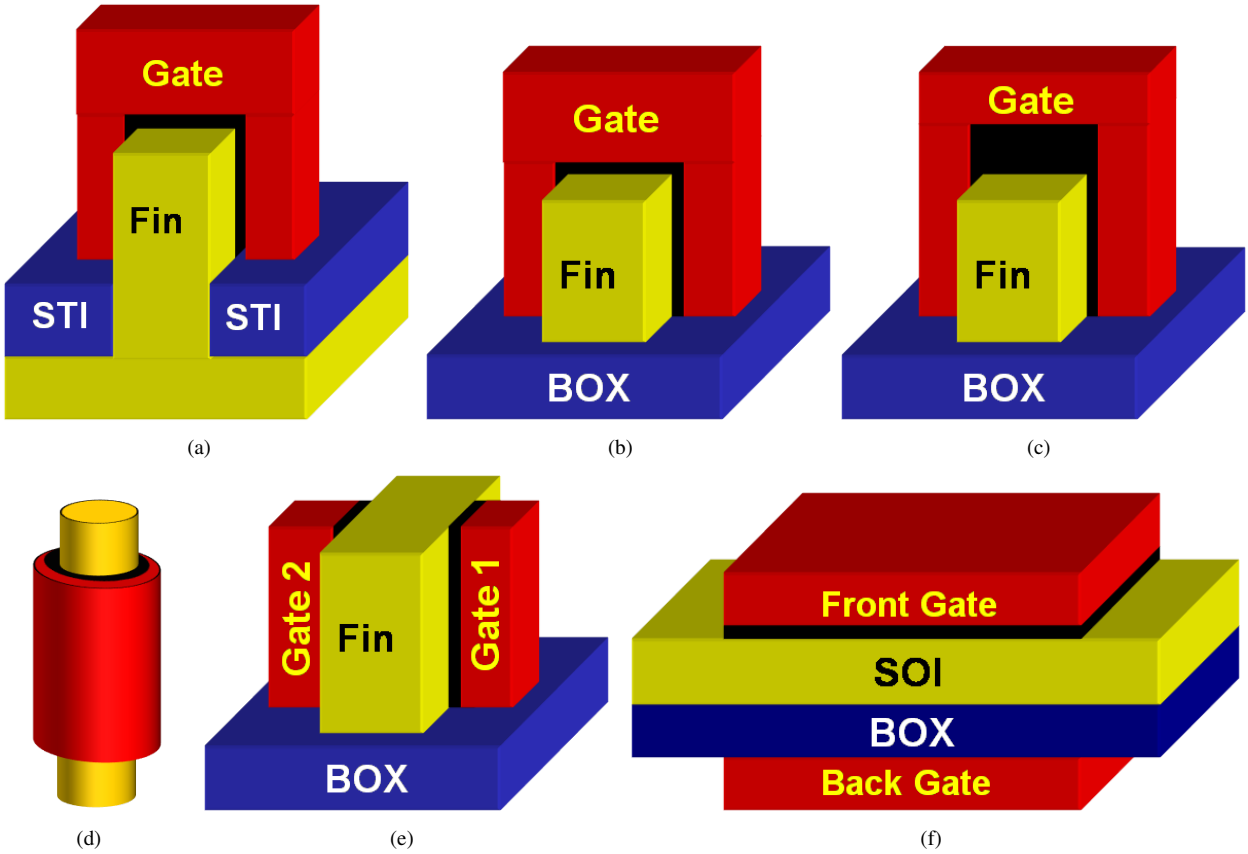


Figure 1: (a) Triple-gate FinFET on Bulk Si (b) Triple-gate FinFET on SOI (c) Double-gate FinFET on SOI (a) All-around Gate (e) Independent Double-gate FinFET on SOI (f) Planar Double-gate SOI

sible. We have classified multi-gate MOSFETs into two main categories: independent multi-gate (IMG) and common multi-gate (CMG) MOSFETs. IMG refers to independent double-gate MOSFET with two separate gates. The front- and back-gate stacks are allowed to have different gate workfunctions, biases, dielectric thicknesses and materials. Independent-gate FinFET (Fig. 1(e)) and the planar double-gate SOI (Fig. 1(f)) belong to this category. CMG refers to a special case where all the gates have identical workfunction, bias and dielectric thickness and material. Regular FinFETs and gate all-around MOSFETs (Figs. 1(a)- (d)) fall into to this category. Two separate compact models BSIM-IMG and BSIM-CMG have been developed in a single framework for IMG and CMG devices, respectively. BSIM-IMG has 4 or 5 terminals: front-gate, back-gate, drain, source and an optional substrate terminal. BSIM-CMG has one less terminal compared to BSIM-IMG because there is only one gate terminal.

3.1 BSIM-CMG MODEL

The BSIM-CMG is a surface potential-based model for a multi-gate MOSFET with undoped or doped body. The Poisson's equation with inversion carrier is perturbed by the body doping and a modification to the surface potential is derived. The analytical surface potential agrees well with TCAD double-gate device simulation for different doping concentration of the fin without any fitting parameter (Fig. 2).

The core I-V model in BSIM-CMG is based on the drift-diffusion formulation without using the charge-sheet approximation [9].

$$I_d = \mu \cdot \frac{W_{eff}}{L} \cdot \left[f(\psi_{s,s}) - f(\psi_{s,d}) \right] \tag{1}$$

where $f(\psi_{s,s(d)})$ is given by:

$$f(\psi_{s,s(d)}) = \frac{Q_{inv,s(d)}^2}{2C_{ox}} + 2\frac{kT}{q} Q_{inv,s(d)} - \frac{kT}{q}\left(5C_{si}\frac{kT}{q} + Q_{bulk}\right) \cdot \ln\left(5C_{si}\frac{kT}{q} + Q_{bulk} + Q_{inv,s(d)}\right) \tag{2}$$

$$Q_{inv,s(d)} = C_{ox} \cdot (V_g - V_{fb} - \psi_{s,s(d)}) - Q_{bulk} \tag{3}$$

$$Q_{bulk} = \sqrt{2qN_A\varepsilon_{si}\psi_{pert}} \tag{4}$$

BSIM-CMG has been verified with measurements of gate-all around (cylindrical-gate) FET and also on both SOI and bulk FinFET technologies. Fig. 3(a) and Fig. 3(b) show the model verification for cylindrical-gate FET structure for p- and n-type devices [5].

The SOI FinFETs were fabricated on a lightly doped 60nm thick film with 2nm SiO_2 dielectric and a strained TiSiN gate

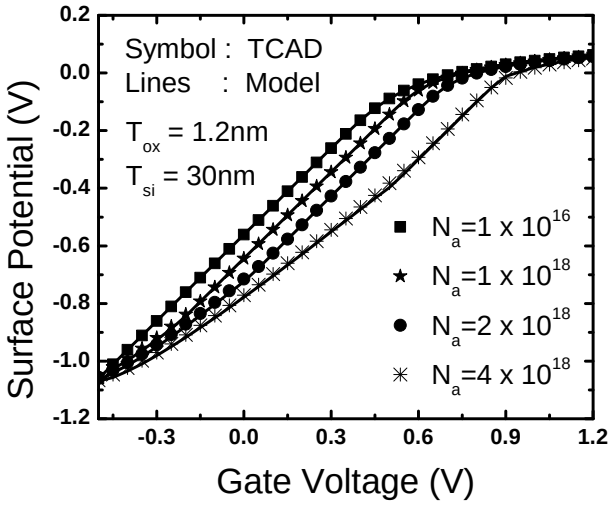


Figure 2: Surface potential versus gate voltage in symmetric double-gate FET for different body doping concentrations. (T_{si} = 30nm, T_{ox} = 1.2nm, Φ_g = 4.61eV)

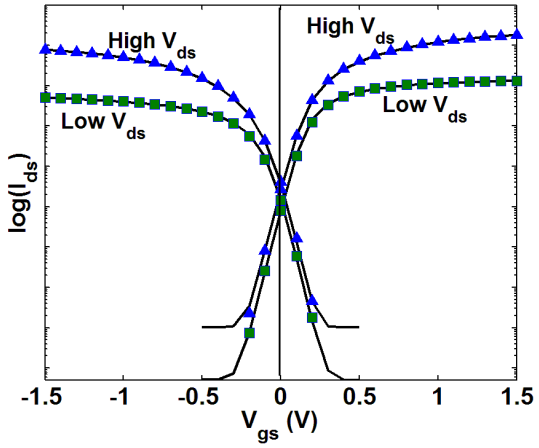
[10]. Measured devices had 20 parallel fins and each fin is 22nm thick.

A global extraction methodology is developed to fit devices with gate lengths ranging from 75nm to 1μm. Binning is not used to fit the data. Figs. 4 (a)-(d) show $I_d - V_{gs}$ for both n-type and p-type FinFETs in linear and saturation modes at different L's. Figs. 4 (e)(f) show threshold voltage roll-off with L and sub-threshold swing degradation. Good agreement between the model and data is achieved.

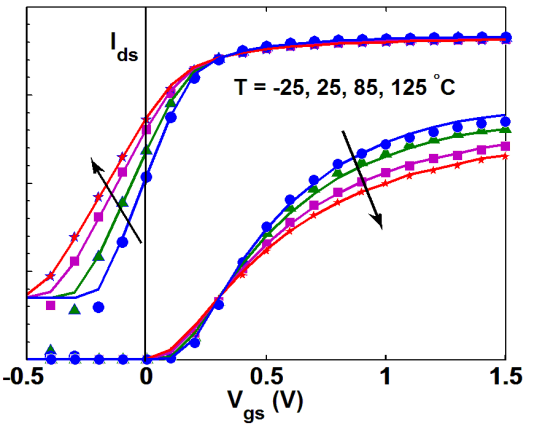
3.2 BSIM-IMG MODEL

BSIM-IMG is also a surface-potential based model, i.e. the I-V and C-V are expressed in terms of electric potentials at the silicon/oxide interfaces. Surface potentials are calculated at both the source and the drain end of the channel. The front and back sides are asymmetric: the two gate stacks may have different work functions (ϕ_{fg} , ϕ_{bg}), materials (metal or heavily doped semiconductor), dielectric thicknesses (T_{ox1}, T_{ox2}), and dielectric constants (ε_{ox1}, ε_{ox2}). We assume that the silicon body is lightly-doped as independent double-gate MOS- FETs will likely have a lightly-doped body to minimize RDF. Since IMG design provides a raised V_{th} with the back gate bias, it is particularly useful for transistors with lightly doped body (low V_{th}). To get an analytical closed form solution of surface potential, we assumed that the inversion carrier density at the back surface is much smaller than that at the front surface. Thus, BSIM-IMG model is valid when the back-side surface in in accumulation or depletion which is also the case with industrial UTBSOI devices [8].

Figs. 5(a)-(c) compare the calculated surface potential with TCAD. TCAD simulations are performed for long- channel devices. To show the intrinsic properties of the model we do not use any fitting parameters in the verification of



(a) $I_{ds} - V_{gs}$ for n and p-type CG-FET ($V_{ds} = -50$mV)



(b) $I_{ds} - V_{gs}$ for n-type CG-FET for different temperatures (V_{ds} = 50mV)

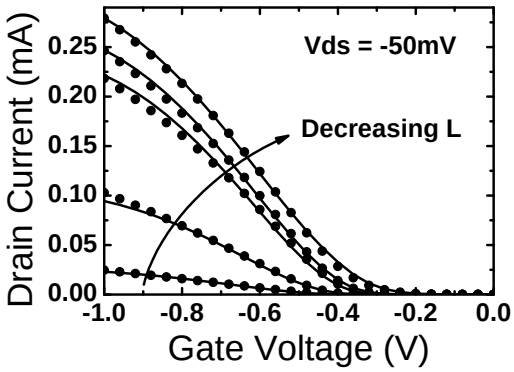
Figure 3: Vertically oriented cylindrical gate FETs were fabricated with moderate channel doping on a bulk substrate. The channel is 150nm tall and has a diameter of 80nm. Polysilicon gate and a 3*nm* SiO_2 gate-oxide were used. Model accuracy is shown here for both N- and P-FETs (Symbols: measured data and lines: model).

the core model. In Fig. 5(a), ψ_{s1} is plotted versus V_{fg} for different values of V_{ch}, showing good agreement. Each V_{ch} corresponds to a different position along the channel. Figs. 5(b) and 5(c) demonstrate the scalability of the model with T_{si} and T_{ox2}.

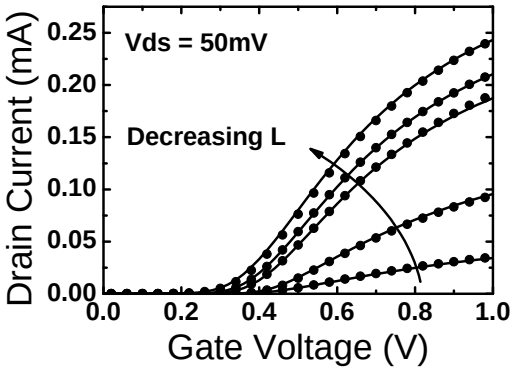
The drain current is derived based on the charge sheet approximation [11]:

$$I_{ds} = \mu \frac{W}{L} \left[\frac{Q_{is} + Q_{id}}{2} (\psi_{s1,d} - \psi_{s1,s}) + \frac{kT}{q} (Q_{is} - Q_{id}) \right] \quad (5)$$

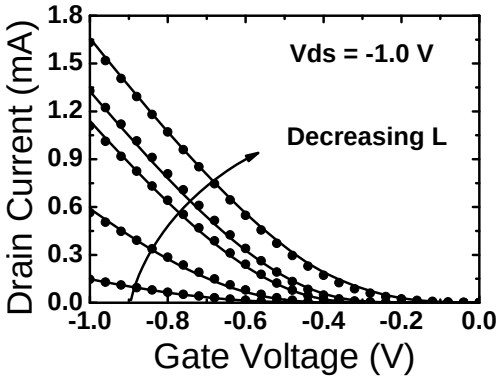
The surface potential and inversion charge in Eq. (5) are calculated using the approximation described in [11]. $\psi_{s1,s}$ and Q_{is} are calculated at $V_{ch} = 0$; $\psi_{s1,d}$ and Q_{id} are calculated at $V_{ch} = V_{ds}$.



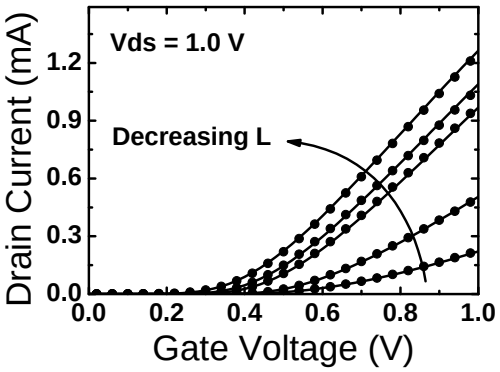
(a) $I_{ds} - V_{gs}$ for p-type FinFET ($V_{ds} = -50$mV)



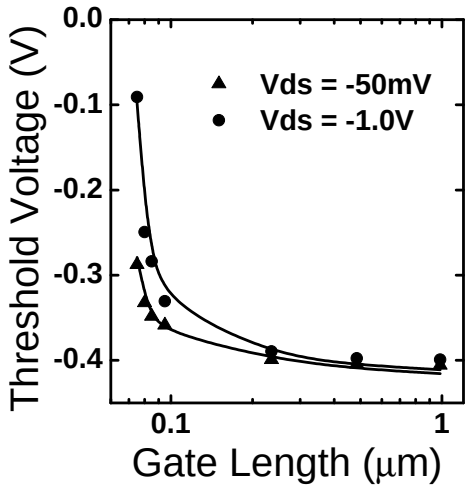
(b) $I_{ds} - V_{gs}$ for n-type FinFET ($V_{ds} = 50$mV)



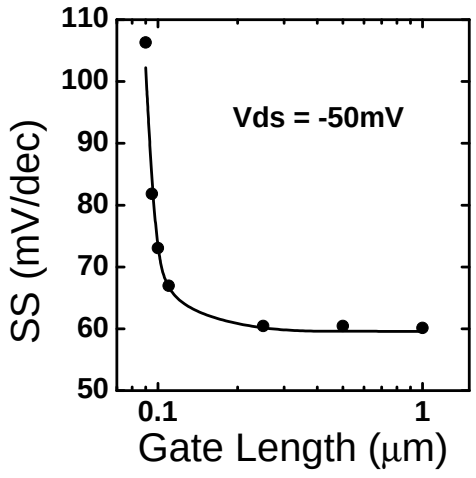
(c) $I_{ds} - V_{gs}$ for p-type FinFET ($V_{ds} = -1.0$V)



(d) $I_{ds} - V_{gs}$ for n-type FinFET ($V_{ds} = 1.0$V)

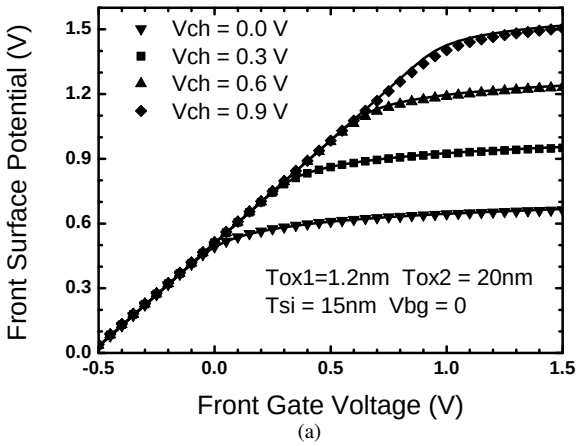


(e) $V_{th} - L$ for p-type FinFET

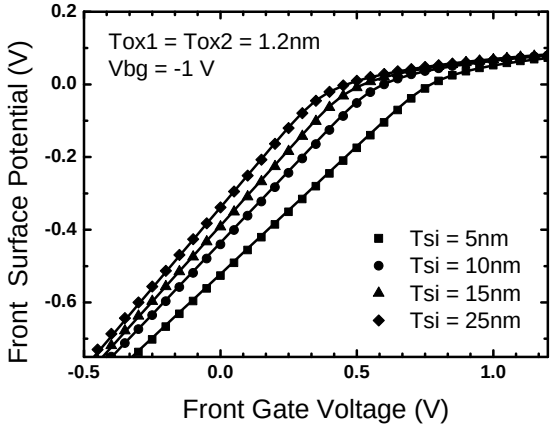


(f) Sub-threshold swing degradation

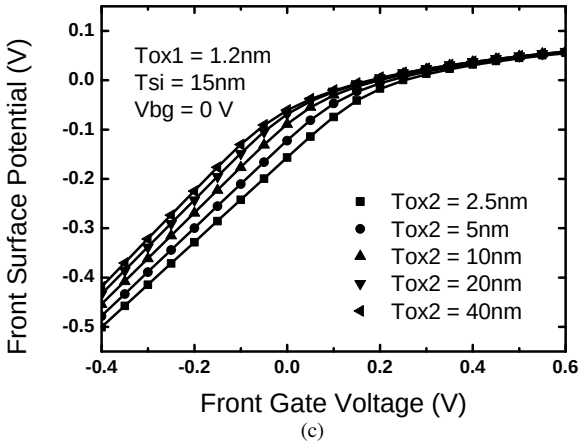
Figure 4: Global extraction results for n-type and p-type SOI FinFETs with 20 parallel fins. ($H_{fin} = 60$nm, $T_{fin} = 22$nm, $EOT = 2$nm, length $L = 75$nm, 85nm, 90nm, 235nm and 1μm; the body is lightly-doped (2×10^{15}cm^{-3})). Symbol: Measured data, Line: Model.



(a)



(b)



(c)

Figure 5: (a) Front surface potential versus front-gate bias with varying channel voltage. ($q\Phi_{g1} = q\Phi_{g2} = 4.4$eV) (b) Front surface potential versus front-gate bias with varying body thickness. ($V_{ch} = 0$, $\Phi_{g1} = 4.4$V, $\Phi_{g2} = 4.4$V) (c) Front surface potential versus front-gate bias with varying back-gate dielectric thickness. ($V_{ch} = 0$, $\Phi_{g1} = 4.17$V, $\Phi_{g2} = 5.29$V). (Symbols: TCAD; Lines: Model)

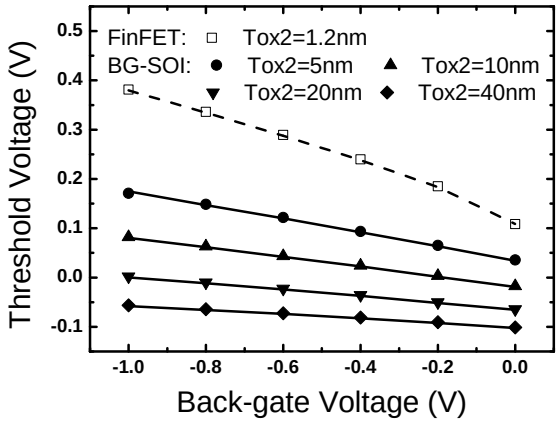


Figure 6: Threshold voltage versus front-gate bias with varying back-oxide thickness. Solid lines and closed symbols: asymmetric structure ($T_{si} = 15$nm, $T_{ox1} = 1.2$nm, $V_{ch} = 0$, $\Phi_{g1} = 4.17$V, $\Phi_{g2} = 5.29$V); dashed lines and open symbols: symmetric structure ($T_{ox1} = T_{ox2} = 1.2$nm, $T_{si} = 15$nm, $\Phi_{g1} = 4.4$V, $\Phi_{g2} = 4.4$V; Symbols: TCAD; Lines: Model). The threshold voltage is extracted using a constant current definition ($100nA \cdot W/L$).

Figs. 6 - 9 demonstrates the accuracy of the drain current model by comparing it to TCAD without using any fitting parameters and assuming a constant carrier mobility. In Fig. 6, V_{th} is plotted versus back-gate bias (V_{bg}) for independent double-gate devices with both symmetric and asymmetric structures. The model agrees well with TCAD for both cases. Larger slope for thin back-oxide devices is due to the stronger coupling from the back side. Fig. 7 shows I_{ds} versus front-gate bias (V_{fg}) for different T_{ox1}, demonstrating the scalability of the model to different dielectric thicknesses. Fig. 8 shows I_{ds} versus V_{ds} with different V_{fg}. Fig. 9 shows transconductance (g_m) versus V_{fg} at both low and high V_{ds}. In Fig. 9, the transconductance efficiency, g_m/I_{ds} is plotted versus V_{fg}. g_m/I_{ds} is an important design metric that characterize the maximum transconductance that the device can provide at a given bias current. At low V_{fg} it should saturate to a constant, whose value is given by

$$\frac{g_m}{I_{ds}} \approx \frac{\frac{d}{dV_{fg}} \exp\left(\frac{qV_{fg}}{nkT}\right)}{\exp\left(\frac{qV_{fg}}{nkT}\right)} = \frac{q}{nkT} \qquad (6)$$

4 Short-channel effects

The most important physical effect that influences the dependence of V_{th} on geometry (such as T_{si} or L) in short L devices is the short channel effect (SCE). This includes V_{th} roll-off at smaller gate lengths, drain induced barrier lowering (DIBL) and sub-threshold slope (SS) degradation. These phenomena are well-known in planar MOSFETs models and are widely-used for circuit simulation [12]:

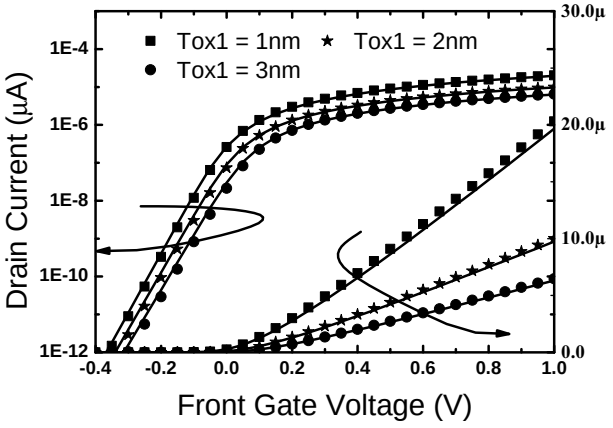


Figure 7: Drain current versus front-gate voltage for different front dielectric thicknesses. ($T_{si} = 15$nm, $T_{ox2} = 20$nm, $V_{bg} = 0$V, $V_{ds} = 50$mV, $\Phi_{g1} = 4.17$V, $\Phi_{g2} = 5.29$V; Symbols: TCAD; Lines: Model)

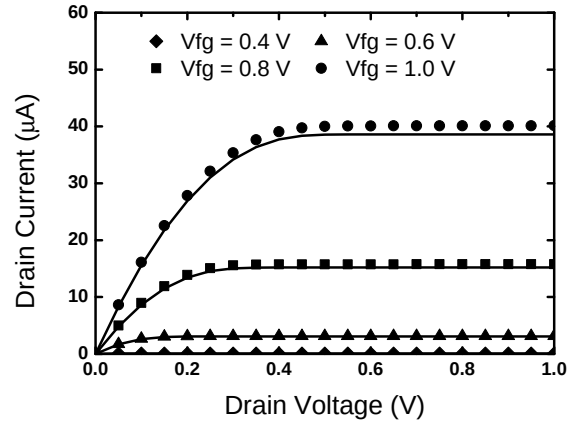


Figure 8: Drain current versus drain voltage for different front-gate bias. ($T_{si} = 15$nm, $T_{ox1} = T_{ox2} = 1.2$nm, $V_{bg} = -1$V, $\Phi_{g1} = 4.4$V, $\Phi_{g2} = 4.4$V; Symbols: TCAD; Lines: Model)

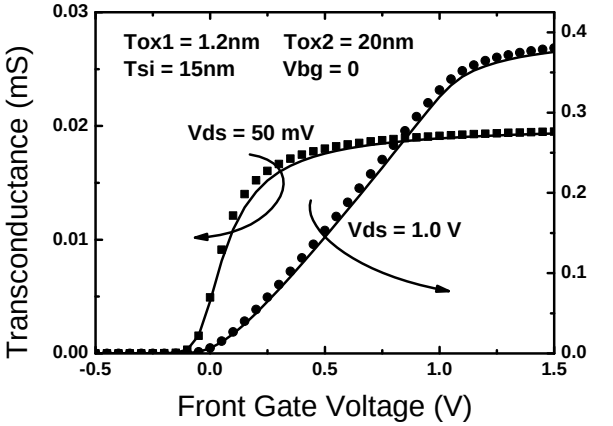


Figure 9: Transconductance versus front-gate voltage at $V_{ds} = 50$mV and $V_{ds} = 1.0$V. The transconductance in TCAD is extracted from small-signal simulations. ($T_{si} = 15$nm, $T_{ox1} = 1.2$nm, $T_{ox2} = 20$nm, $V_{bg} = 0$V, $\Phi_{g1} = 4.17$V, $\Phi_{g2} = 5.29$V; Symbols: TCAD; Lines: Model)

$$\Delta V_{th}(SCE) = -\frac{0.5 \cdot DVT0}{cosh\left(DVT1 \cdot \frac{L}{\lambda}\right) - 1} \cdot (V_{bi} - \phi_B - 0.45) \quad (7)$$

$$\Delta V_{th}(DIBL) = -\frac{0.5 \cdot ETA0}{cosh\left(DSUB \cdot \frac{L}{\lambda}\right) - 1} \cdot V_{ds} \quad (8)$$

$$C_{dsc} = \frac{0.5(CDSC + CDSCD) \cdot V_{ds}}{cosh\left(DVT1 \cdot \frac{L}{\lambda}\right) - 1} \quad (9)$$

$$n = 1 + \frac{CIT + C_{dsc}}{(2C_{si}) \parallel C_{ox}} \quad (10)$$

The capitalized quantities on the right hand sides of these expressions are adjustable parameters that allow the user to obtain a better fit to measured data.

It was found that for L being a given multiple of λ, the degree of short channel effect is more or less the same. As technology advances, λ is reduced and SCE starts at a shorter L. For bulk MOSFETs, λ is given as (assuming the junction depth X_j is large) [12].

$$\lambda = \sqrt{\gamma T_{ox} X_{dep}} \quad (11)$$

where $\gamma = \varepsilon_{si}/\varepsilon_{ox}$, T_{ox} is the oxide thickness and X_{dep} is the width of the depletion region. The scale length (λ) for multi-gate FETs is different from bulk MOSFETs and Eq. (11) must be modified [10], [11]. In BSIM-IMG, λ is derived with the assumption that the inversion carriers are located near at the front surface. On the other hand, BSIM-CMG assumes the inversion carriers concentrate around the center of the body (fin). Therefore λ for BSIM-IMG and BSIM-CMG are different even at $T_{ox1} = T_{ox2}$.

Most of the real device effect models are similar to BSIM4 model. Even if some of the real device models are not same as BSIM4, we have ensured that the parameter names are the same for easier extraction based on BSIM4 experience.

REFERENCES

[1] D. J. Frank et al., Proceedings of the IEEE, 89, 259-288, 2001.

[2] X. Huang et al., IEEE IEDM, 67-70, 1999.

[3] H.-S. Kim et al., Symposium on VLSI Technology, 143–144, 1995.

[4] K. Takayanagi et al., Journal of the Japan Society of Applied Physics International (JSAPI), 3, 3-8, 2001.

[5] S. Venugopalan et al., VLSI-TSA, 2011.

[6] D. Fried et al., IEEE Electron Device Letters, 25, 199-201, 2004.

[7] I. Y. Yang et al., IEEE Transaction on Electron Devices, 44, 822-831, 1997.

[8] O. Faynot et al., IEEE IEDM, 2010.

[9] J. R. Brews, Solid-Sate Electronics, 21, 345–355, 1978.

[10] M. V. Dunga et al., Symposium on VLSI Technology, 60-61, 2007

[11] D. D. Lu et al., Solid State Electronics, 2010.

[12] BSIM4 Manual, Available online - http://www-device.eecs.berkeley.edu/ bsim3/bsim4.html.