Hybrid CMOS/Nanodevice Circuits with Tightly Integrated Memory and Logic Functionality

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ABSTRACT

We propose hybrid CMOS/nanodevice circuits which have potentials to perform massively parallel high throughput computations and in particular suitable for pattern matching. The performance advantage of novel circuits is mainly due to very high density of nanoscale devices and very tight and synergetic integration of memory and logic functionalities. The tight integration is enabled by high communication bandwidth of area-distributed interface between the nano and CMOS subsystems, while the synergy is due to flexible resource allocation allowing to use nanodevices either as a ternary content addressable memory cell or to implement programmable logic/interconnect.

Keywords: Hybrid circuits, FPGA, CMOL, pattern matching, RRAM.

1 INTRODUCTION

Field programmable gate array (FPGA) circuits [1] allow for very efficient implementation of pattern matching in network intrusion detection, DNA sequence matching, database searching and network packet routing. However, even contemporary FPGAs cannot provide enough computational power for future demands. For instance, the inevitable development of 100 Gbps-scale data networks would make real time network intrusion detection impossible [2] even using the most optimistic assumptions for scaling of complementary metal-oxide semiconductor (CMOS) technology.

Earlier we have shown that the performance of FPGAs can be greatly improved with hybrid CMOS/nanodevice circuits of "CMOL" variety (Fig. 1) [3, 4]. In CMOL circuits (which stands for Cmos/MOLecular-scale nanodevices hybrids) the density advantages of emerging technologies, such as nanoimprint and resistive switching "memristive" nanodevices [5], are combined with versatility of CMOS technology. The simulation results have shown that even with very low (< 1%) utilization of nanodevices CMOL FPGAs could be up to two orders of magnitude denser and/or faster as compared to CMOS FPGAs with the same design rules for a wide range of benchmark circuits [3]. The recent experimental demonstration of CMOL FPGA-like circuits supports feasibility of the approach (Fig. 2) [6, 7].

In this paper we show that information processing tasks are uniquely suited for high fan-in gates of CMOL FPGA circuits, provided a certain modification to the circuits, and therefore could take efficiently advantages of higher density of nanoscale devices. In particular, we propose CMOL FPGAs based on single multifunctional flip-flop CMOS cell and discuss our preliminary performance results for pattern matching tasks. In the next section we review main features of CMOL circuits and present modified CMOL FPGAs in section 3. Discussion of performance of hybrid circuits and summary is presented in Section 4.

2 CMOL CIRCUITS

In CMOL memristive devices are integrated in the crossbar structures which are defined on top of the conventional CMOS substrate (Fig. 1). CMOS circuitry provides signal restoration and gain for logic circuitry and used to build decoders and sensing circuitry to program memristive devices. A unique feature of CMOL circuits is area distributed interface which enables high vertical bandwidth, and comes with potentially very low cost and low overhead. The area interface is enabled by (i) the crossbar array which is rotated by an angle $\alpha = \arcsin(1/\beta)$ with respect to the mesh of CMOS-controlled vias; and (ii) a double decoding scheme that provides a unique access to each crosspoint memristive device. More specifically, as Fig. 1 shows, two types of vias, one connecting to the lower (shown with blue dots) and the other to the upper (red dots) wire level in the crossbar, are arranged into a square array of "basic cells" with sides $2\beta F_{CMOS}$. Here $\beta > 1$ is a dimensionless number that depends on the cell size (i.e. complexity) in the CMOS subsystem. Note that with rotated crossbar array vias naturally subdivide the wires into fragments of length $2(\beta F_{CMOS})^2/F_{nano}$. The factor β is not arbitrary, but is chosen from the spectrum of possible values $\beta = (r^2 + 1)^{1/2} \times F_{nano}/F_{CMOS}$, where r is an integer so that the precise number of devices on the wire fragment is $r^2 - 1 \approx \beta^2 (F_{CMOS}/F_{nano})^2$.

The decoding scheme in CMOL is based on two separate address arrays (one for each level of wire in the crossbar so that there are a total of $4N$ edge channels to provide access to two different via controllers (one 'blue' and one 'red') in each of N^2 addressing cells in the CMOS plane (Fig. 1). In contrast to standard memory arrays, in CMOL each control and data line pair electrically connects the peripheral input/outputs to a via instead of a single

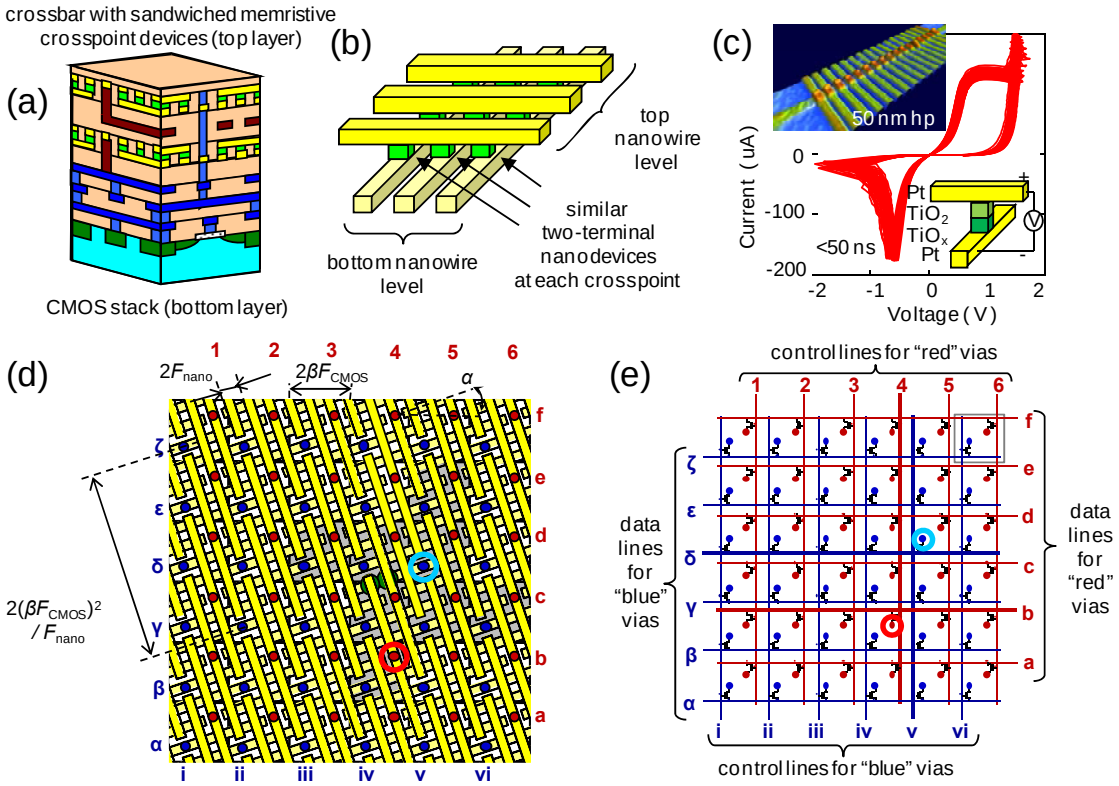

Figure 1. The basic idea of CMOL circuits [3, 4]: (a) hybrid circuit cartoon, (b) crossbar, (c) micrograph of array of thin film metal oxide memristive devices and typical switching *I-V*s [7], (d) top view of the crossbar structure showing α for $r = 3$, and (e) corresponding equivalent circuit diagram of the configuration logic in CMOS layer for the $N = 5$ primitive cell array. For clarity, panel d shows only two memristive crosspoint devices (green dots) which are used for the explanation in text.

memory element. In turn, each via is connected to a wire fragment in the crossbar. The two perpendicular sets of wire fragments provide unique access to any crosspoint device even for large values of β. For example, selecting pins δv and b4 (which are highlighted with blue and red circles, correspondingly) provides access to the leftmost of the two shown devices on Fig. 1d, while pins δv and c4 for the rightmost device.

3 PATTERN MATCHING WITH CMOL FPGA CIRCUITS

Our proposed circuits are based on uniform fabric of CMOS D-flip-flop cells in which flip-flop is interconnected with the crossbar with the help of four vias. In particular two output vias (shown with red circle) are connected to normal and complimentary outputs of flip-flop and two inputs ones (shown with blue circle) are connected to D input (Fig. 3d). Clock signals are assumed to be routed using CMOS subsystem and are not shown in Fig. 3. During programming, CMOS flip-flop is disabled in all cells, e.g., by having "eval" CMOS line set to low. As a result any crosspoint memristive device (shown with green circle on Fig. 3c) in a crossbar structure can be setup to on or off state with the help of CMOS pass transistors and CMOS data and select lines, i.e. utilizing double decoding scheme of CMOL which was described above.

After the programming stage, logic operations are implemented with dynamic diode logic formed by ON-state memristive devices and CMOS pass transistors, while signal restoration, inversion, and latching is performed by CMOS D-flip-flop (Fig. 3). (Note that in principle, static diode logic, similar to original CMOL FPGA [3], with better noise immunity but worse speed can be used instead). More specifically, the logical summation (i.e. Boolean "OR" operation) is performed in dynamic fashion in two stages during the clock period. During the first shorter stage the outputs of flip-flop in all cells are disconnected from corresponding crossbar wire using CMOS "eval" line. At the same time crossbar wire connected to the inputs and the outputs of flip-flop are precharged to high voltage using "select/pre" and "data/pre" CMOS lines. During the second stage, the "eval" signal is set to "high" voltage. This results in logical summation of the values from the cells connected to the particular crossbar wire with memristive devices turned to the ON state. At the rising clock edge, the value latched at the flip flop so that it can be used in unchanged or complimented form in the next clock cycle. Note that, though the operation performed on the crossbar wire is equivalent to OR Boolean operation, Boolean AND could

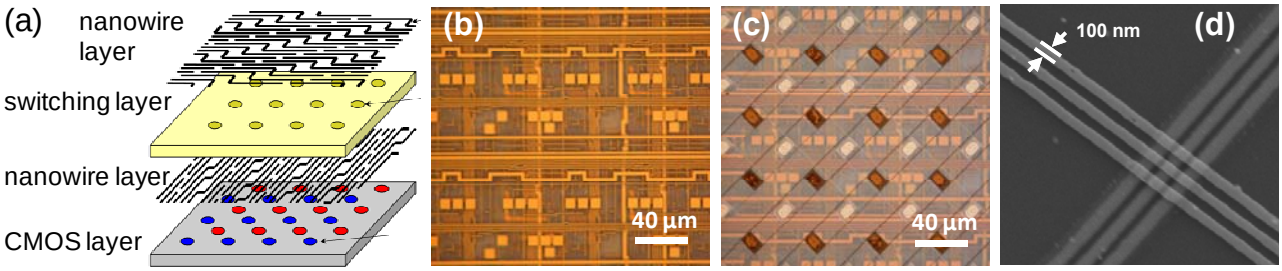

Figure 2. (a) Conceptual illustration of the memristor-CMOS hybrid architecture [6, 7]. (b) Optical micrograph of the as-received CMOS chip; (c) the hybrid chip with memristor crossbars built on top; and (d) scanning electron microscope image of a fragment of the memristor crossbar array (where 3 nanowires cross 3 other nanowires, forming 9 memristors) with junction areas of 100 × 100 nm^2.

also be performed in one cycle utilizing De Morgan's law due to the presence of complimentary outputs Q.

4 DISCUSSION AND SUMMARY

In proposed circuits one flip flop cell can perform pattern matching in just one clock cycle (Fig. 3). The maximum size of a pattern is determined by the number of memristive devices attached to two input nanowires of flip-flop cell, i.e. quasi vertical ones on Fig. 3c, which is equal to $2(r^2 - 1)$ for one crossbar layer. Note that the pattern matching operation is very similar to that of (ternary) content addressable memories (T/CAM). The quasi vertical nanowire is equivalent to a match line which is being charged or discharged depending on the voltage levels of quasi horizontal nanowires (signal lines of TCAM) and memristive devices (TCAM cells).

The universal flip-flop cells could be also configured to perform Boolean logic operations, e.g., to perform logical operation with the results of pattern matching operation and/or to stream data, e.g. by forming very deep pipelines. For example, given array of flip-flop cells one can configure every second row of cells to stream data, from left to right on Fig. 3, and have remaining cells to perform pattern matching. With such mapping the maximum pattern matching capacity per one flip-flop cell is $N_{bits} = 1/2 \times 1/2 \times 2(r^2 - 1)$. Here the first factor of 1/2 reflects the fact that only half of flip-flop cells is involved in pattern matching operation (the other half is used for streaming), and the second one that only half of the memristive devices can be used for pattern matching in the simplest case (i.e. only memristive devices programmed to connect to flip-flop cells which streams data). With such mapping the effective density of patterns stored and processed is just 1/4 of the maximum passive crossbar memory capacity.

We can also estimate the minimum clock cycle by assuming that all power is dynamic, because the static leakage could be neglected for the memristive devices with high on-off ratio. The maximum clock frequency f can be found from the equation $C_{wire}V^2 f_{max}/2 = p_{max} A_{cell}$, where V is a voltage swing, $C_{wire} \approx 4 \times 2F_{nano} \times r^2 \times C_{seg}$ is a total capacitance charged per cycle for one cell (i.e. of 4 nanowire segments with C_{seg} capacitance per unit length), p_{max} = 200 W/cm^2 is a typical manageable power consumption density, and $A_{cell} = 2 \times (2\beta F_{CMOS})^2$ is a flip-flop cell area. For example, assuming somewhat conservative values V = 1V, β = 10, K = 1 and using data from Ref. 3 for crossbar wire capacitance, $f_{max} \approx p_{max} F_{nano} / (C_{seg} V^2) \approx$ 100 MHz for F_{nano} = 3 nm and F_{CMOS} = 45 nm, and $f_{max} \approx$ 1 GHz for F_{nano} = 45 nm and F_{CMOS} = 130 nm. The pattern matching throughputs per unit area, defined as $N_{bits} f_{max}/A_{cell}$, corresponding to these two cases are 10^{19} and 10^{18} bits/s/cm^2 (Fig. 4), respectively, which is much higher than any reported state-of-the art concepts.

Also note that the proposed circuits could potentially offer much higher pattern capacity without any performance penalty. Because the number of storage elements in existing hardware-based pattern matchers is limited by the 2D chip area, they must be dynamically reconfigured to accommodate additional patterns that are beyond their storage capabilities. Dynamic reconfiguration is a relatively slow process, and if pattern matcher could not fit all the patterns the throughput for a fixed area will be considerably smaller than the ideal value. On the other hand, the bit capacity of the dynamic CMOL FPGA can be seamlessly increased by integrating more crossbar layers using the multilayer CMOL idea [4]. Thus, our architecture can support more patterns without any degradation in throughput.

In conclusion, we believe that the proposed circuits are very promising for pattern matching applications. It is worth mentioning that the current main challenge towards building such circuits is yield of today's memristive devices, even considering high intrinsic defect tolerance of CMOL FPGAs [3]. However, large scale industrial efforts on passive crossbar memories give hope that this issue might soon be resolved.

REFERENCES

[1] S. Hauck and A. DeHon, *Reconfigurable computing: The theory and practice of FPGA-based computation*, Morgan Kaufmann, 2008.

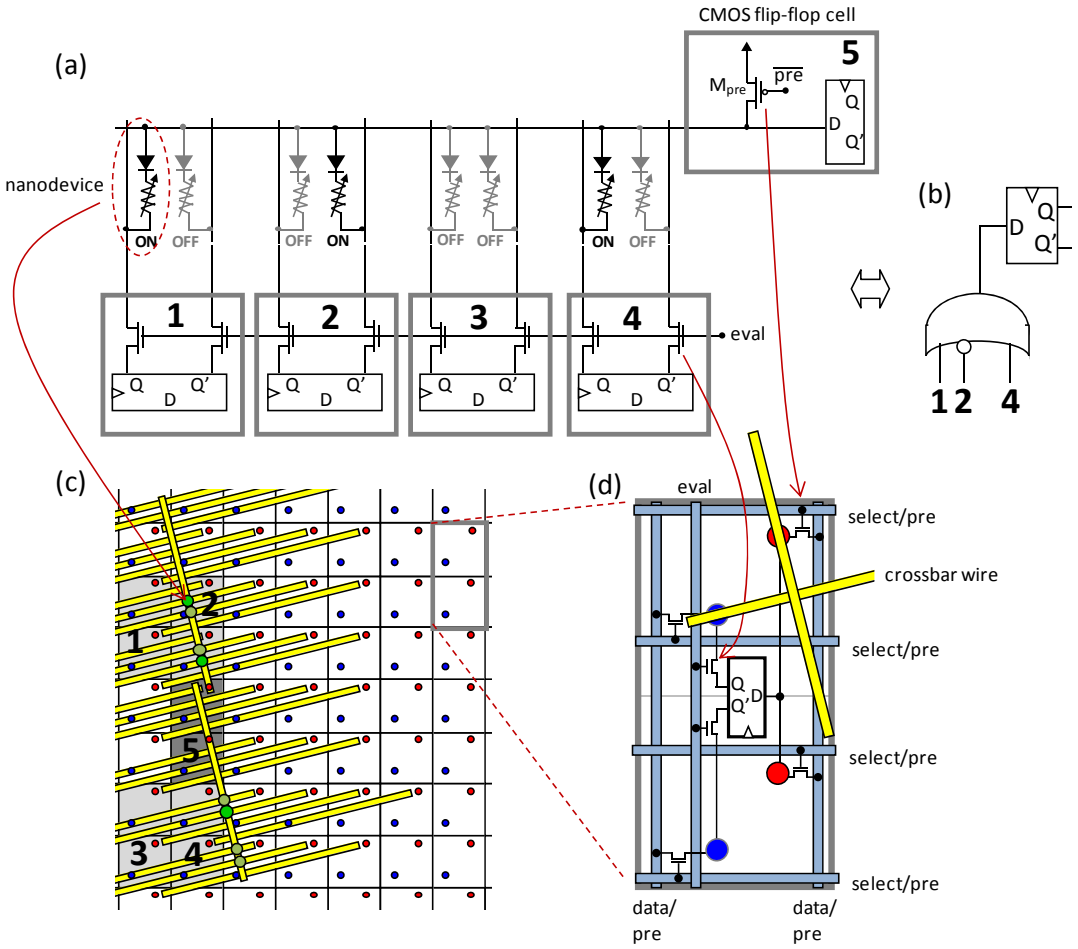

Figure 3. Dynamic CMOL FPGA logic: (a) Example of circuitry which is programmed to detect pattern "10X1" and (b) its equivalent functionality to (c) dynamic CMOL FPGA fabric which consists of (d) multipurpose D-flip-flop cells. Note that for clarity panel c only shows nanowires which overlap with input nanowires of cell denoted with number "5" and only those nanodevices which participate in the considered example. Bright and light green dots denote nanodevices in the on and off states, correspondingly.

[2] Y.H. Cho *et al.*, "Deep network packet filter design for reconfigurable devices," *ACM Trans. Embed. Computing Syst.,* vol. 7, p. 21:6-21:26, 2008.

[3] K.K. Likharev and D.B. Strukov, "CMOL: Devices, circuits, and architectures," *Lecture Notes in Physics*, vol. 680**,** pp. 447-477, 2006.

[4] D.B. Strukov and R.S. Williams, "Four-dimensional address topology for circuits with stacked multilayer crossbar arrays," *PNAS*, vol. 106 pp. 20155-20158, 2009.

[5] D.B. Strukov *et al.*, "The missing memristor found," *Nature,* vol. 453 pp. 80-83, 2008.

[6] Q.F. Xia*, et al.*, "Memristor-CMOS hybrid integrated circuits for reconfigurable logic," *Nano Letters,* vol. 9 pp. 3640-3645, 2009.

[7] D.B. Strukov *et al.,* "Hybrid CMOS/memristor circuits", in: *Proc. ISCAS'10* , art. 5537020, Paris, France, June 2010, pp. 1967-1970.

[8] D.B. Strukov *et al.*, "Prospects for 10^{19} bits/s/cm^2 pattern matching with CMOL FPGA circuits", submitted to ICCAD'2011

[9] International Technology Roadmap for Semiconductors, 2007 Edition, Available online at http://www.itrs.net.

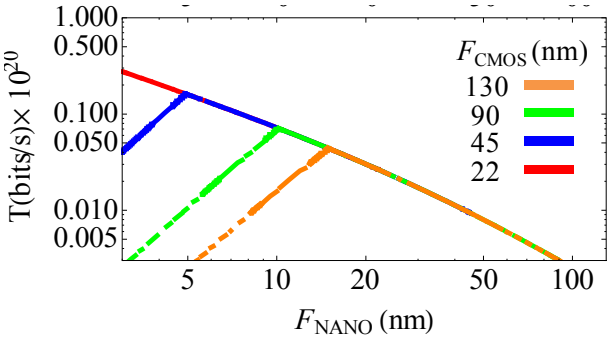

Figure 4. Pattern matching hroughput as a function of F_{nano} for several values of F_{CMOS} [8].