Single-walled Carbon Nanotube (CNT) Field Effect Transistor Device Modeling

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ABSTRACT

We have developed a surface potential based compact model for the single-walled semiconductor CNT field effect transistor (CNT-FET) shown in Figure 1. Our compact modeling results for surface potential, channel charge, gate capacitance and channel current are shown in Figures 2-5 respectively. The model comparison is done using the numerical results of [1-4]. The compact model is developed for circuit simulation application based on *graphene* material physics using a 1-D approximation.

Keywords: circuit simulation, compact device modeling, CNT-FET, SPICE

1 INTRODUCTION

There is a strong possibility of integration in the semiconductor industry of carbon based devices such as CNT field effect transistor (CNT-FET) on to a silicon platform beyond the dominant CMOS scaling, to achieve integrated circuits (ICs) with high performance and speed. As a result CNT-FET compact models will be required for hybrid (CMOS and CNT-FET) circuit simulation applications.

There has been extensive modeling work done for a CNT-FET that is shown in Figure 1. For example Prof. Wong's group at Stanford [1-4] has developed a semi-analytic model that determines the surface potential numerically, or represents it by an empirical equation [1, 2]. The work done by Prof. Pulfrey's group at University of British Columbia (UBC) is mainly a numerical [5-7] solution of the coupled *Poisson* and *Schrodinger* PDEs and it is not appropriate for circuit simulation application.

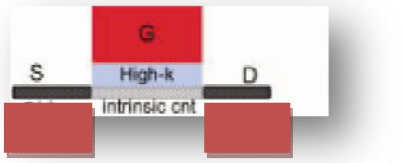

Figure 1: Single-walled CNT field effect transistor.

In this paper our compact models are developed based on the *graphene* material physics using a 1-D approximation for circuit simulation application.
The CNT-FET compact model derivation is given in Section 2 and the model simulation results with comparison of the numerical result, [1], are given in Section 3.

2 COMPACT DEVICE MODELS

The results from [4, 7] allow us to express the CNT-FET surface charge density, Q_{cnt}, in terms of the surface potential, ψ_s, as

$$Q_{CNT} = (V_{gs} - V_{fb} - \psi_s)C_{ins} \qquad (1)$$

where V_{gs} denotes the gate voltage, V_{fb} the flat band voltage, $C_{ins} = \dfrac{2\pi\varepsilon_{ins}}{\ln(\frac{t_{ins}}{R_t}+1)}$ dielectric capacitance, t_{ins} dielectric thickness, ε_{ins} dielectric permittivity and R_t CNT radius.

The nanotube radius can also be written as a function of nanoribbon width w [8, 11]:

$$R_t = w/2\pi \qquad (2)$$

where $w = a\sqrt{3}\sqrt{n^2 + m^2 + nm}$ and a=0.142nm is the carbon-carbon bond length. The chiral numbers n and m denote the number of unit vectors along the two directions in the honeycomb crystal lattice of the graphene.

For long tubes an integral representation of the charge density is also given in [4] using a density of states (DOS) calculation (also see [9]). The CNT charge density can be simplified using a first sub-band energy approximation [3]:

$$Q_{CNT} = \frac{q}{2} n_i e^{\frac{q\psi_s}{k_b T}} \left(1 + e^{\frac{-qV_{ds}}{k_b T}}\right) \qquad (3)$$

where n_i denotes the intrinsic carrier density, k_b the Boltzmann constant, T temperature, q electrical charge and V_{ds} drain-source voltage.

Equation (1) and (3) yield the surface potential as

$$\psi_s(V_{gs}, V_{ds}) = V_{gs} - V_{fb} - \frac{k_b T}{q} W'\left(\frac{q^2 n_i}{2k_b T C_{ins}}(1 + \alpha e^{\frac{-qV_{ds}}{K_b T}}) e^{\frac{q(V_{gs} - V_{fb})}{k_b T}}\right) \qquad (4)$$

where $W'(x)$ is the *Lambert* function which is a solution of $x = W' e^{W'}$ (see [10]). The parameter $\alpha = -13.8\bar{d}_t + 23.8$ is used as a fitting parameter and $\bar{d}_t$ is diameter of the nanotube per *nm* length.

The channel current of a ballistic CNT-FET, which is the net flux of forward and backward traveling carriers, can be derived using the first sub-band energy approximation [1].

$$I_{ds} = \frac{4k_b T q}{h}\left[\ln(1 + e^{\frac{2q\varphi_s - E_g}{2k_b T}}) - \ln(1 + e^{\frac{2q\varphi_s - 2qV_{ds} - E_g}{2k_b T}})\right] \qquad (5)$$

where $\varphi_s = \psi_s(V_{gs}, V_{ds} = 0)$, h is Planck's constant, and the energy band gap is $E_g = \frac{0.765(\text{ev.nm})}{d_t}$.

3 RESULTS AND DISCUSSION

Our compact modeling results for surface potential, channel charge, gate capacitance and channel current are shown in Figures 2-5 respectively.

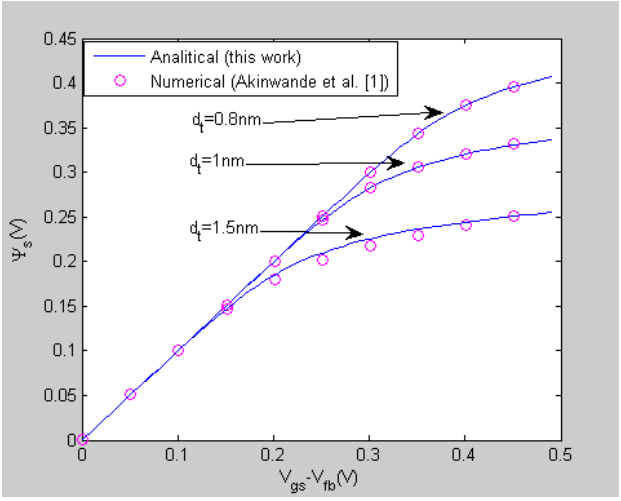

Figure 2: CNT-FET channel surface potential versus relative gate voltage V_{gs}-V_{fb} for nanotube diameter d_t=0.8, 1 and 1.5nm, high-K dielectric thickness t_{ins}=10nm with K=15 is used and V_{ds}=0V.

The model comparison is done using the numerical results of [1] and the model shows a good fit. In Figures 4 and 5 the approximation that was taken at large nanotube diameter d_t needs improvement and this leads to future modeling approaches.

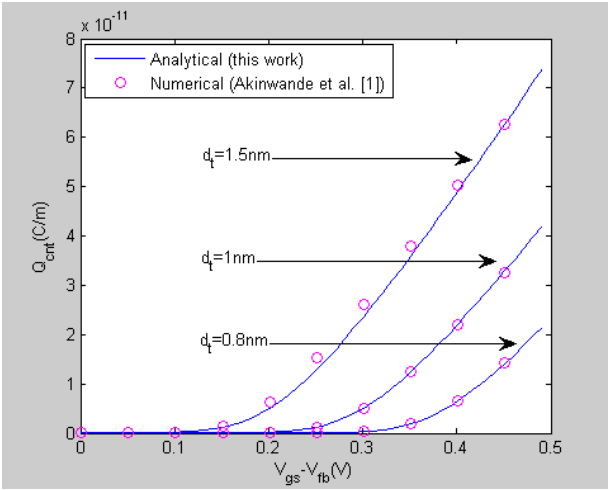

Figure 3: CNT-FET channel charge versus relative gate voltage V_{gs}-V_{fb} for nanotube diameter d_t=0.8, 1.0 and 1.5nm, high-K dielectric thickness t_{ins}=10nm with K=15 is used and V_{ds}=0V.

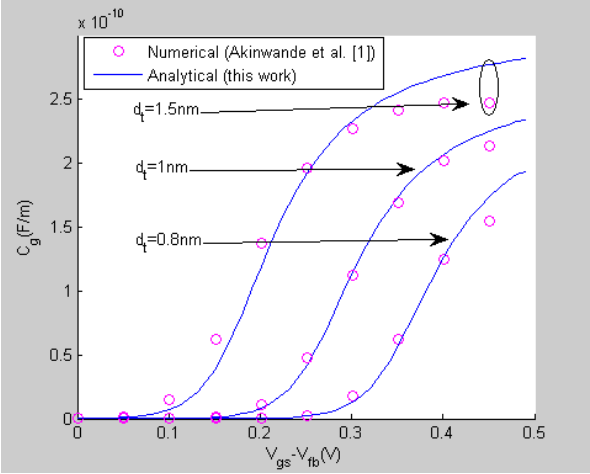

Figure 4: CNT-FET gate capacitance per unit length versus relative gate voltage V_{gs}-V_{fb} for nanotube diameter d_t=0.8, 1.0 and 1.5nm, high-K dielectric thickness t_{ins}=10nm with K=15 is used and V_{ds}=0V.

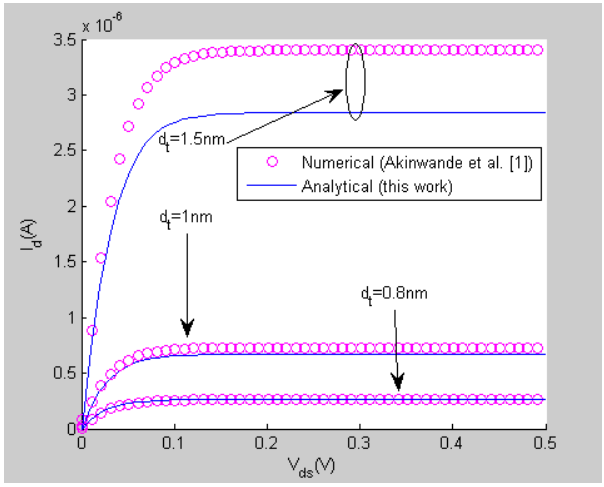

Figure 5: CNT-FET channel current versus drain-source voltage V_{ds} for nanotube diameter d_t=0.8, 1.0 and 1.5nm, high-K dielectric thickness t_{ins}=10nm with K=15 is used.

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