Analytic potential model for asymmetricunderlap gate-all-around MOSFET

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Abstract—An analytic potential model for undoped cylindrical gate-all-around (GAA) MOSFET with asymmetric gate underlap is developed in this paper. This model is derived by solving the Poisson's equation with the parabolic potential approximation, channel length transformation and conformal mapping. The analytic body center potential solution is presented. Compared with TCAD simulations, the proposed model shows good agreements, with different dimensions of the structure and varied bias conditions. The model here is appropriate for predicting the effect of gate misalignment or asymmetric gate underlap in GAA MOSFETs' design.

Keywords- *asymmetric; underlap; misalinment; gate-all-around;*

I. INTRODUCTION

Gate-all-around (GAA) or nanowire MOSFETs have been regarded as a promising technology for sub-10-nm CMOS devices, because of their good gate control capability over the channel [1]. As the fully-depleted gate-all-around (GAA) MOSFET's natural length [2] is shorter than the double-gate (DG) MOSFET's [3], GAA MOSFETs minimize the short channel effects (SCE). To decrease the channel volume, gate underlap structure has been applied for double-gate MOSFETs [4] and cylindrical gate-all-around MOSFETs [5]. The underlap structure results in a bias-dependent effective channel length L_{eff} that is long in the subthreshold region and short in the on-state [6]. The impacts of gate underlap structure have been discussed in [5], such as reducing SCE. Considering the asymmetric structures' advantage, double-gate MOSFETs with asymmetric drain underlap can reduce junction capacitance and has an optimization structure [7]. Additionally using a compact model that considers the fringing field effect, an analysis of the gate misalignment effect on the threshold voltage of DG ultrathin FD SOI nMOS devices is reported [8]. However, no analytical model for cylindrical GAA MOSFET with asymmetric gate underlap has been reported. In this paper, an analytic subthreshold potential model for asymmetric gate underlap cylindrical GAA MOSFETs is presented. The fringing field is derived by effective channel length transformation [9] and conformal mapping as done in [5]. This model is verified by the 3D numerical simulation tool TCAD.

II. ANALYTICAL MODEL FORMULATION

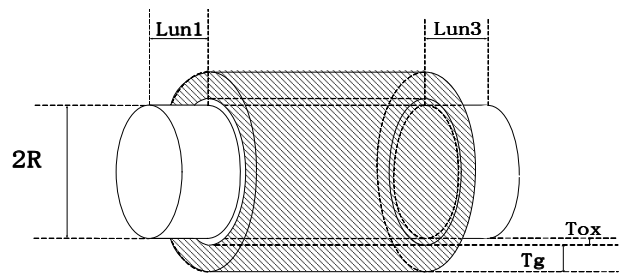

Fig.1. Three-dimensional schematic of an asymmetric gate underlap cylindrical gate-all-around MOSFET. Lun1 and Lun3 are the length of gate underlap next to source and drain respectively.

Conformal mapping is not directly applicable to GAA MOSFETs due to the 3-D cylindrical structure [5]. To solve this, a channel length transformation method has been developed in [9]. The effective underlap length L_{uneff1} and L_{uneff3} is expressed similarly by

$$L_{un1.eff} = L_{un1}\left(\lambda_{DG} / \lambda_{GAA}\right) \tag{1a}$$

$$L_{un3.eff} = L_{un3}\left(\lambda_{DG} / \lambda_{GAA}\right) \tag{1b}$$

$$\lambda_{DG} = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}}(1+\frac{\varepsilon_{ox}t_{si}}{4\varepsilon_{si}t_{ox}})t_{si}t_{ox}} \tag{1c}$$

$$\lambda_{GAA} = \sqrt{\frac{2\varepsilon_{si}t_{si}^2\ln(1+\frac{2t_{ox}}{t_{si}})+\varepsilon_{ox}t_{si}^2}{16\varepsilon_{ox}}} \tag{1d}$$

Where λ_{DG} and λ_{GAA} are nature lengths of a DG MOSFET [3] and a GAA MOSFET [2] respectively. The transformations (1) maps the 3D potential distribution in a cylindrical structure into 2D potential in a planar double-gate structure and it only applied to regions I and III.

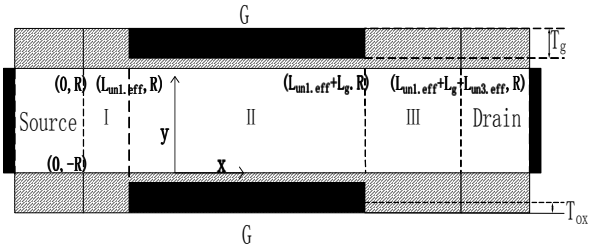

Fig.2. Schematic of a transformation of the 3D GAA structure into DG structure. Regions I and III are underlap regions. Device body (regions I, II, and III) is undoped.

In [2], a body center potential solution along the channel direction is assumed in region II

$$\phi_{C2}(x)=[Ce^{(x-L_{un1.eff})/\lambda_{GAA}}+De^{-(x-L_{un1.eff})/\lambda_{GAA}}]+(V_{gs}-\phi_{ms}) \quad (2)$$

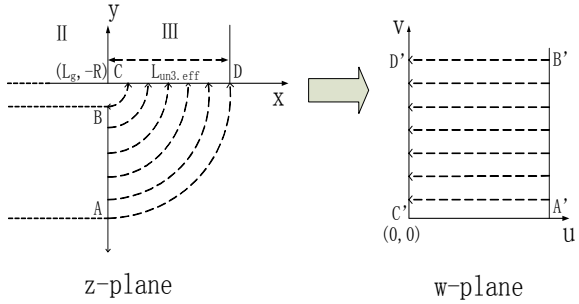

Fig.3. boundary of the sidewall region next to the edge of the underlap region before and after conformal mapping. AB is the gate right edge and CD is the Si-SiO$_2$ interface at the surface of region III. Z-plane is transformed to w-plane as done in [11]

After the transformations (1) and conformal mapping, in regions I and III, the gate underlap regions of the source and drain, the body center potentials are given similar forms by [10]

$$\phi_{c1}(x)=A[1-\frac{\alpha_1}{2}r_{c1}^2]+B[r_{c1}-\frac{\alpha_1}{6}r_{c1}^3]+(V_{gs}-\phi_{ms}) \quad (3a)$$

$$\phi_{c3}(x)=E[1-\frac{\alpha_3}{2}r_{c3}^2]+F[r_{c3}-\frac{\alpha_3}{6}r_{c3}^3]+(V_{gs}-\phi_{ms}) \quad (3b)$$

$$\eta_1=\frac{t_{ox}}{L_{un1.eff}}\sinh^{-1}[\cosh^{-1}(\frac{t_{ox}+t_g}{t_{ox}})]$$

$$\eta_3=\frac{t_{ox}}{L_{un3.eff}}\sinh^{-1}[\cosh^{-1}(\frac{t_{ox}+t_g}{t_{ox}})] \quad (3c)$$

$$\alpha_1=\frac{2\varepsilon_{ox}t_{ox}}{\varepsilon_{si}Rm\pi\eta_1^2} \qquad \alpha_3=\frac{2\varepsilon_{ox}t_{ox}}{\varepsilon_{si}Rm\pi\eta_3^2} \quad (3d)$$

$$r_{c1}=\eta(L_{un1.eff}-x)/t_{ox} \qquad r_{c3}=\eta(x-L_{un3.eff})/t_{ox} \quad (3e)$$

In which m is such that sin (mπ/2) =1 and is chosen to be 2 (by matching the simulation results). A-F are underdetermined constants and are computed by applying the continuity of the potential and electric field between adjacent regions. These six boundary conditions are given in [10]. But as the transformations (1), the two continuity of electric fields boundary conditions are changed by:

$$\left.\frac{d\phi_{c1}(x)}{dx}\right|_{x=L_{un1.eff}}\times(\frac{\lambda_{GAA}}{\lambda_{DG}})=\left.\frac{d\phi_{c2}(x)}{dx}\right|_{x=L_{un1.eff}} \quad (4a)$$

$$\left.\frac{d\phi_{c3}(x)}{dx}\right|_{x=L_g+L_{un3.eff}}\times(\frac{\lambda_{GAA}}{\lambda_{DG}})=\left.\frac{d\phi_{c2}(x)}{dx}\right|_{x=L_g+L_{un3.eff}} \quad (4b)$$

The six values are obtained by these boundary conditions as

$$C=\frac{V_x(g_1-g_3e^{-L_g/\lambda_{GAA}}+\frac{t_{ox}h_1}{\eta_1\lambda_{DG}}+\frac{t_{ox}h_3}{\eta_3\lambda_{DG}}e^{-L_g/\lambda_{GAA}})+V_{DS}(g_1+\frac{t_{ox}h_1}{\eta_1\lambda_{DG}})}{2(g_1g_3+\frac{t_{ox}h_1}{\eta_1\lambda_{DG}}\cdot\frac{t_{ox}h_3}{\eta_3\lambda_{DG}})\sinh(\frac{L_g}{\lambda_{GAA}})+2(\frac{g_1t_{ox}h_3}{\eta_3\lambda_{DG}}+\frac{g_3t_{ox}h_1}{\eta_1\lambda_{DG}})\cosh(\frac{L_g}{\lambda_{GAA}})} \quad (5a)$$

$$D=\frac{V_x(-g_1+g_3e^{L_g/\lambda_{GAA}}+\frac{t_{ox}h_1}{\eta_1\lambda_{DG}}+\frac{t_{ox}h_3}{\eta_3\lambda_{DG}}e^{L_g/\lambda_{GAA}})+V_{DS}(-g_1+\frac{t_{ox}h_1}{\eta_1\lambda_{DG}})}{2(g_1g_3+\frac{t_{ox}h_1}{\eta_1\lambda_{DG}}\cdot\frac{t_{ox}h_3}{\eta_3\lambda_{DG}})\sinh(\frac{L_g}{\lambda_{GAA}})+2(\frac{g_1t_{ox}h_3}{\eta_3\lambda_{DG}}+\frac{g_3t_{ox}h_1}{\eta_1\lambda_{DG}})\cosh(\frac{L_g}{\lambda_{GAA}})} \quad (5b)$$

$$A=C+D \qquad B=(D-C)\frac{t_{ox}}{\lambda_{DG}\eta_1} \quad (5c)$$

$$E=Ce^{L_g/\lambda_{GAA}}+De^{-L_g/\lambda_{GAA}} \qquad F=(Ce^{L_g/\lambda_{GAA}}-De^{-L_g/\lambda_{GAA}})\cdot\frac{t_{ox}}{\lambda_{DG}\eta_3} \quad (5d)$$

$$g_1=1-\frac{\alpha_1}{2}(\frac{\eta_1L_{un1.eff}}{t_{ox}})^2 \qquad g_3=1-\frac{\alpha_3}{2}(\frac{\eta_3L_{un3.eff}}{t_{ox}})^2 \quad (5f)$$

$$h_1=\frac{\eta_1L_{un1.eff}}{t_{ox}}-\frac{\alpha_1}{6}(\frac{\eta_1L_{un1.eff}}{t_{ox}})^3 \qquad h_3=\frac{\eta_3L_{un3.eff}}{t_{ox}}-\frac{\alpha_3}{6}(\frac{\eta_3L_{un3.eff}}{t_{ox}})^3 \quad (5g)$$

$$V_x=V_{bi}-V_{gs}+\phi_{ms} \quad (5h)$$

Then transformed these solved potential solutions into the original structure. These solutions after length transformed are corrected with different dimensions of structure and these are verified by 3-D numerical simulation in the following results section. As the relationship in [2], surface potential can be derived from center potential and then the asymmetric underlap cylindrical GAA MOSFET's subthreshold channel potential distribution is obtained.

$$\phi(r,x)=\phi_c(x)-\left\{\frac{\varepsilon_{ox}r^2[\phi_c(x)-\phi_{gs}]}{2\varepsilon_{si}R^2\ln(1+\frac{t_{ox}}{R})+2\varepsilon_{ox}R^2}\right\} \quad (6)$$

Where x is along channel direction and r is along radial direction.

III. RESULTS AND DISCUSSION

TCAD simulation is used to verify the results provided by the proposed model without advanced physical effects. The body of underlap regions and body regions are undoped and the spacer above the underlap region is assumed to be oxide.

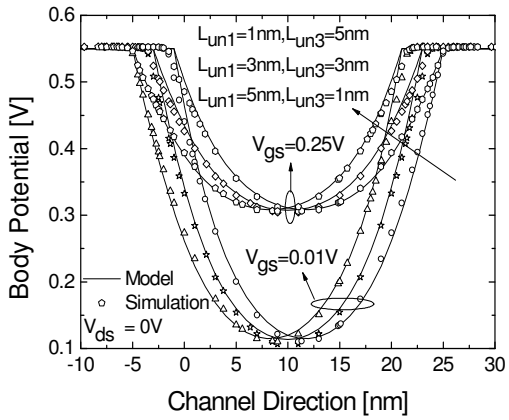

Fig.4. Body center potential for asymmetric gate underlap GAA MOSFET in channel direction with different lengths of gate underlap and gate bias compared with the TCAD 3-D numerical simulation.

In fig.4 great differences are observed between symmetric gate underlap GAA MOSFETs and asymmetric GAA MOSFETs. The lengths of underlap strongly influence the potential distribution in body regions. The minimum body potential is located in the middle of body region as expected. As an example, an asymmetric gate underlap cylindrical GAA MOSFET with R=7.5nm, t_{ox}=1.5nm, L_{gate}=20nm, H_{gate}=10nm is discussed in fig.4.

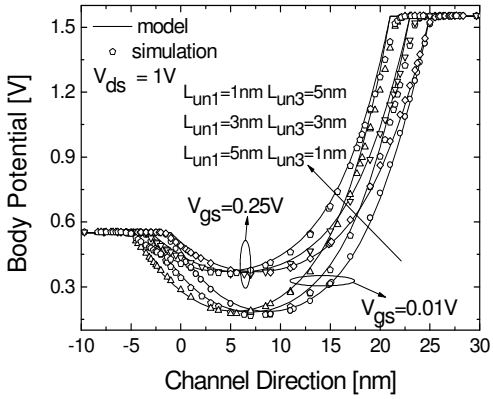

Fig.5. Body center potential for asymmetric gate underlap GAA MOSFET in channel with different lengths of gate underlap and gate bias compared with the TCAD 3-D numerical simulation under large V_{ds}.

Fig.5 shows that the different lengths of underlaps strongly influence the potential in region II. Some asymmetric gate underlap GAA MOSFET make the potential in region II more flat than symmetric gate underlap GAA MOSFET when V_{ds} is not negligible. Therefore the asymmetric gate underlap design GAA MOSFETs may have better performances in reducing SCE in large V_{ds}. The proposal model has a good agreement with 3-D numerical simulation. An asymmetric gate underlap cylindrical GAA MOSFET with R=7.5nm, t_{ox}=1.5nm, L_{gate}=20nm, H_{gate}=10nm is discussed in fig.5.

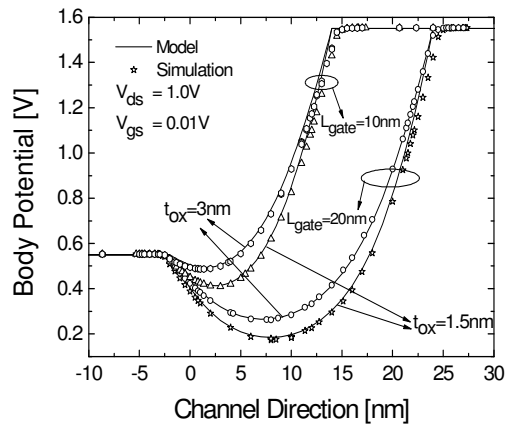

fig.6. Body center potential for asymmetric gate underlap GAA MOSFET in channel with different thickness of gate-oxide compared with the TCAD 3-D numerical simulation.

Fig.6 shows the model-predicted body center potential along the channel direction for asymmetric underlap with different thickness of gate-oxide. It can be seen that minimum potential decreases with the decrease t_{ox}. Error is made in the drain underlap region when tox is thick. An asymmetric gate underlap cylindrical GAA MOSFET with R=7.5nm, L_{un1}=2nm, L_{un3}=4nm and H_{gate}=10nm is discussed in fig.6.

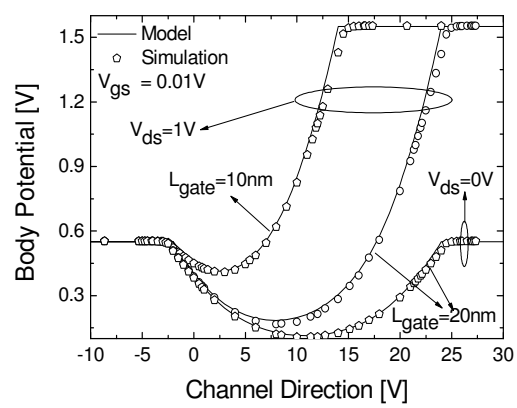

Fig.7. Body center potential for asymmetric gate underlap GAA MOSFET in channel with different lengths of over region (region II) and drain voltage compared with the TCAD 3-D numerical simulation.

Fig.7 shows the model-predicted body center potential along the channel direction for asymmetric

underlap with different length of overlap region. It is observed in fig.7 the minimum body potential increase when length of gate decreases. From the figure, potential increase with V_{ds} increasing and we can predict large V_{ds} can lead to DIBL effect. An asymmetric gate underlap cylindrical GAA MOSFET with R=7.5nm, L_{un1}=2nm, L_{un3}=4nm, H_{gate}=10nm and t_{ox}=1.5nm is discussed in fig.7.

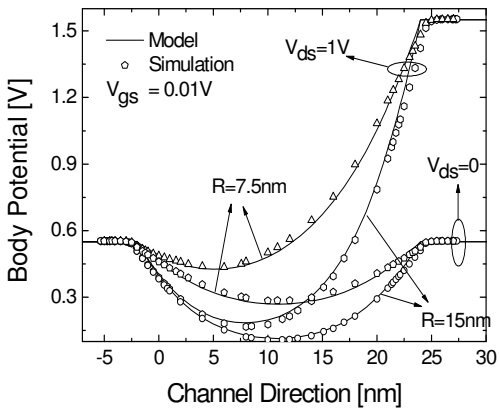

Fig.8. Body center potential for asymmetric gate underlap GAA MOSFET in channel with different lengths of radius of body and gate voltage bias compared with the TCAD 3-D numerical simulation.

Fig.8 shows the model-predicted body center potential along the channel direction for asymmetric underlap with different radius of body region. It is observed the error increases in the middle of channel when the radius of body decreases. An asymmetric gate underlap cylindrical GAA MOSFET with L_{gate}=20nm, L_{un1}=2nm, L_{un3}=4nm, H_{gate}=10nm and t_{ox}=1.5nm is discussed in fig.7.

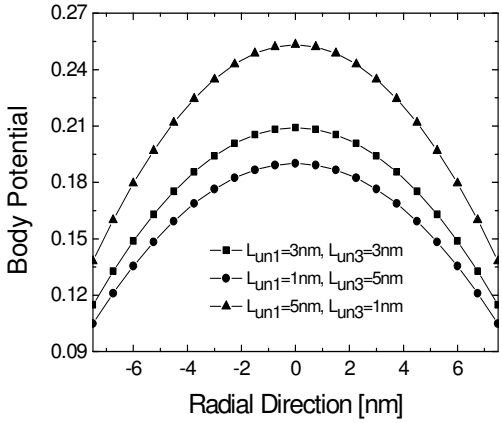

Fig.9. Body center potential for asymmetric gate underlap GAA MOSFET in radial direction with different lengths of underlap.

Fig.9 shows the model-predicted body center potential along the radial direction for asymmetric underlap with different lengths of gate underlap. In fig.9 great differences can be seen in body potential with varied lengths of gate underlap and the biggest difference appears in the middle of channel, which shows that gate misalignment has obvious effects on cylindrical GAA MOSFETs.

IV. CONCLUSION

In this paper, an analytic subthreshold potential model for undoped GAA MOSFET with asymmetric gate underlap is established. Using the parabolic potential approximation, channel length transformation and conformal mapping, an analytic body center potential expression is derived. Compared with TCAD numerical simulation with different length of underlap, thickness of gate-oxide, length of overlap region and bias conditions, the proposed model is verified in all body regions. For the merits of high efficiency and accuracy, the proposed model is appropriate for predicting the effect of gate misalignment or optimization design for asymmetric gate underlap GAA MOSFETs.

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REFERENCES

[1] Conlige JP. “Multiple-gate SOI MOSFETs”, Solid State Electron 2004; 48(6): 897–905.

[2] Auth CP, Plummer JD. “Scaling Theory for Cylindrical,Fully-Depleted, Surrounding-Gate MOSFET’s”, IEEE Electron Dev Lett 1997; 18(2): 74–6.

[3] Suzuki K, Tosaka Y, Tanaka T, Horie H, Arimoto Y. “Scaling Theory for Double-Gate SO1 MOSFET’s” IEEE Trans Electron Dev 1993; 40(12): 2326–2329.

[4] Bansal A, Paul BC, Roy K. “Modeling and Optimization of Fringe Capacitance of Nanoscale DGMOS Devices” IEEE Trans Electron Dev 2005;52(2): 256–262.

[5] Zhang L et al. “Analytical solution of subthreshold channel potential of gate underlap cylindrical gate-all-around MOSFET.” Solid State Electron , 54(2010): 806-808.

[6] Trivedi V, Fossum JG, Chowdhury MM. “Nanoscale FinFETs With Gate-Source/Drain Underlap” IEEE Trans Electron Dev 2005;52(1): 56–62.

[7] Ashish Goel et al. Device Research Conference, 22-24 June 2009, page 57- 58

[8] Elvis C. Sun, James B. Kuo , “A Compact Threshold Voltage Model for Gate Misalignment Effect of DG FD SOI nMOS Devices Considering Fringing Electric Field Effects” IEEE Trans Electron Dev, 2004; 51(4): 587-596

[9] Burli H, Kolberg S, Fjeldly TA, Iñíguez B. “Precise Modeling Framework for Short-Channel Double-Gate and Gate-All-Around MOSFETs” IEEE Trans Electron Dev 2008;55(10): 2678–2686.

[10] Bansal A, Roy K. “Analytical Subthreshold Potential Distribution Model for Gate Underlap Double-Gate MOS Transistors” IEEE Trans Electron Dev 2007; 54(7): 1793–8.

[11] S.-C. Lin, J. B. Kuo, K.-T. Huang, and S.-W. Sun, “A Closed-Form Back-Gate-Bias Related Inverse Narrow-Channel Effect Model for Deep-Submicron VLSI CMOS Devices Using Shallow Trench Isolation” IEEE Trans. Electron Dev, 2000; 47(4): 725–733.