Characteristics Sensitivity of FinFET to Fin Vertical Nonuniformity

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ABSTRACT

Characteristic variation of FinFET due to Fin vertical nonuniformity is simulated in this paper, based on the compact device model. This vertical nonuniformity is generated during the real etching process and induces Fin thickness variation along the height direction. Therefore, the characteristics, such as threshold voltage, sub-threshold slope, on state current, off state current and total channel resistor are investigated influenced by Fin height and deviation angle. The impact of the deviation angle on both digital and analog circuit performance is also predicted.

Keywords: FinFET device, process fluctuation, vertical nonuniformity, performance variation

1 INTRODUCTION

Although FinFETs are theoretically acclaimed for their substantial advantages over bulk MOSFETs [1-9], i.e., the ultra thin body helps the device provide good gate controlling ability and SCEs immunity, they are yet to be widely used in industry. One of the reasons is the high sensitivity to structure parameter fluctuation, especially when FinFETs have aggressively shrunk down to nanometer scale. The process variation and dopant fluctuation are two significant factors relative to threshold voltage dissipation.

Recently, much work has been done on the parameter fluctuation in regular structures [10-14], little of which with nonideal process factors involved [15, 16]. Some side effects caused by nonideal formation during processing will take place calling for new understanding of the device characteristics, new concepts of the device designs and new ideas of the devices innovations.

2 CURRENT CALCULATION IN NONIDEAL FINFET

The schematic structure of nonideal FinFET is shown in Fig.1. Considering the actual photo-resist etching process, it is usually to obtain a Fin-body with a deviational angle instead of rigorous rectangle cross section. As illustrated in Fig.2, when a Fin thickness is transferred from design value to real geometry, the cross section after the photo-resist etching is more likely to exhibit a deviation angle (θ) which is usually symmetric at both sides of the Fin. This vertical nonuniformity has a strong impact on the device characteristics by deviating the body thickness and channel width from original design scale, especially in small scale. Assume the Fin thickness is transferred through the mask ideally as designed, the thickness of the top (Ttop) therefore equals to the design value. Specifically, Ttop=10nm, the height of Fin Hfin=20nm, the thickness of the bottom Tbott =Ttop+2Hfin /tanθ, channel length Lg=1μm and channel width W≈2Wfin=2Hfin /cosθ.

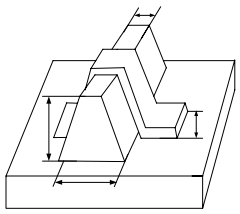


Figure 1: The schematic structure of nonideal FinFET with vertical nonuniform Fin.

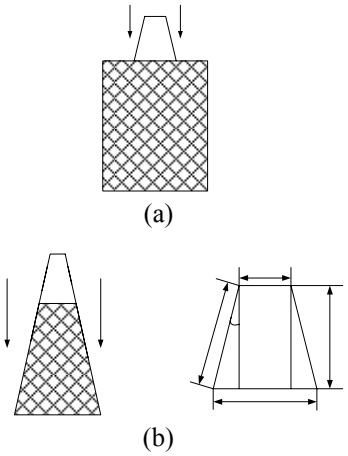


Figure 2: (a) Photo-resist etching process induced Fin vertical nonuniformity and (b) Geometric parameters of the Fin: Ttop and Tbott is the thickness at the top and bottom of

Fin, respectively, Hfin is the height of Fin and θ is the deviation angle.

For the convenience of calculation, the Fin height is divided into a large number (i.e. N=500) of small units, as shown in Fig.3. Therefore, a nonideal FinFET is described in a stack of small Double-Gate (DG) MOSFETs of different body thickness connected in parallel. The channel width of each small DG MOSFET Wfin/N and the body thickness in the No.N unit Tunit, which equals Ttop+2nHfin/N/tanθ, are assumed unified thanks to the small θ and large N. Based on the DG MOSFET compact model [17], the current of each DG MOSFET unit is estimated. The total current is expressed as the sum of these unit currents.

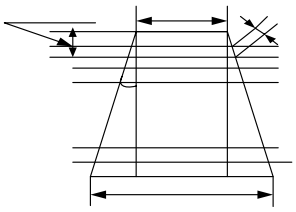
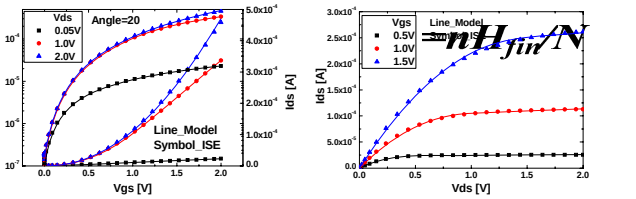


Figure 3: FinFET is divided into N unit DG MOSFETs.

3 RESULTS AND DISCUSSION

Device Performance

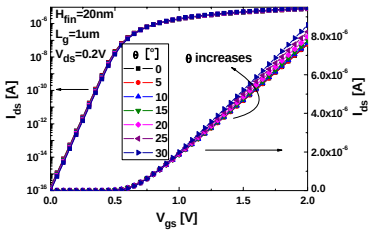
Fig.4 shows the Ids-Vgs and Ids-Vds characteristics when θ is fixed in 20°. The symbols are extracted from ISE simulation. And the lines are what the model presents. As the Fig shows, the model is reliable by strictly matching the simulation data.



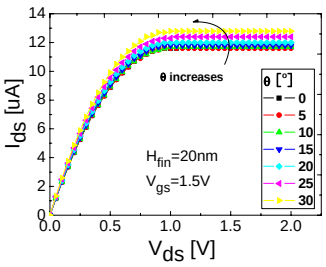
(a) (b) θ

Figure 4: (a)Ids-Vgs and (b) Ids-Vds with θ fixed in 20°.

Fig.5(a) shows the drain current (Ids) versus gate voltage (Vgs) characteristics. And Fig.5(b) shows the drain current (Ids) versus drain voltage (Vds) characteristics. Both figures indicate the current difference with θ shifted from 0° to 30° and Hfin fixed at 20nm respectively. Currents stay almost identical in the sub-threshold region while increase with θ in the linear and saturation regions.



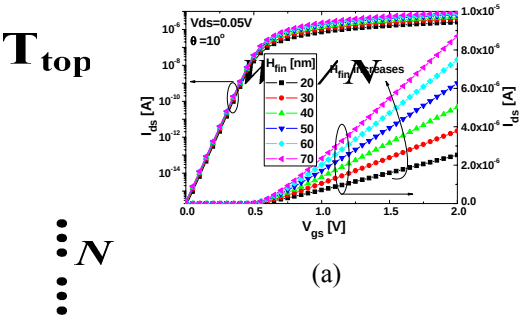
(a)



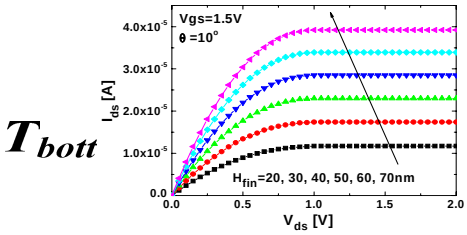
(b)

Figure 5: (a) Ids versus Vgs and (b) Ids versus Vds characteristics with θ ranged from 0° to 30°.

Ids versus Vgs and Ids versus Vds characteristics with Hfin shifted from 20nm to 70nm and θ fixed at 10° are simulated in Fig.6. Similar to the conclusion in Fig.5, it's also difficult to distinguish the current difference in the sub-threshold region. In the linear and saturation regions, the currents increments are obvious as Hfin grows. Compared to Fig.5, the impact of Hfin variation is greater than θ on the increment ratio of the linear and saturation current.



(a)

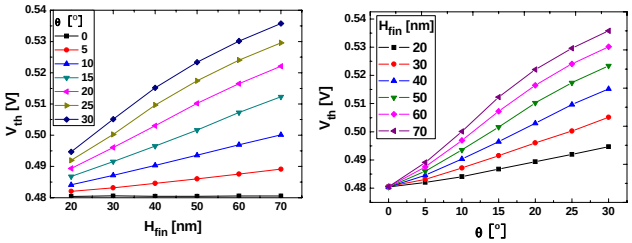


(b)

Figure 6: (a) Ids versus Vgs and (b) Ids versus Vds characteristics with Hfin shifted from 20nm to 70nm.

The threshold voltage (Vth) is extracted using constant current (CC) method by defining

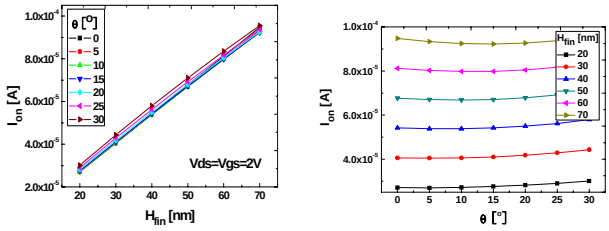
Ids_cc=300nA*Wtotal/Leff [11,12]. In FinFET, Wtotal≈2Wfin while Ids_cc is the current obtained with the Fin of ideal rectangle. Fig.7(a) and (b) show the Vth's sensitivity to the variation of Hfin and θ. When θ equals 0°, which indicates the Fin has the rigorous rectangle cross section, Vth barely changes with Hfin. As θ increases, Vth rises with higher Hfin and tends to saturation at large θ. Comparing Fig.7(b) with Fig.7(a), Fig.7(b) sees Vth grow up more rapidly with enlarged θ even with Hfin fixed at the original design value.



(a) (b)

Figure 7: Threshold voltage versus (a) Hfin (20~70nm) and (b) θ (0°~30°)

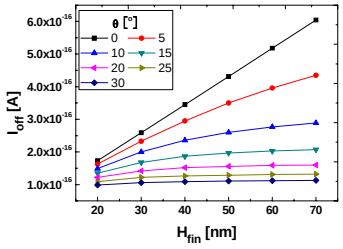
The On-state current Ion is defined as drain-source current when Vgs= Vds=Vdd=2V, where Vdd is the power supply voltage [15]. Fig.8(a) shows the relationship between Ion and Hfin with θ fixed in certain value. As Fig.8(a) shows, Ion grows linearly with Hfin, less sensitive to θ variation. It is furthermore demonstrated in a more explicit curve group as in Fig.8(b). The relative insensitivity to θ is confirmed.



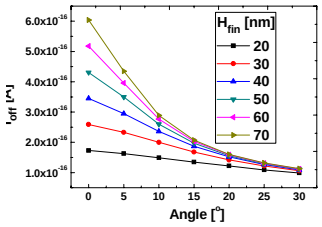
(a) (b)

Figure 8: Ion versus (a) Hfin (20~70nm) and (b) θ (0°~30°).

The Off-state (Ioff) is also a significant parameter for estimating the device performance. Ioff is defined as drain-source current when Vgs=0V and Vds=Vdd=2V. Fig.9(a) shows the relationship between Ioff and Hfin with θ fixed. Ioff is observed rapidly increase with Hfin when θ is small while gradually slowing down when θ is large. As Fig.9(b) shows, Ioff decreases with increasing θ, the smaller θ is, the larger Ioff dissipation is. Compared to Ion, Ioff is more affected by θ.

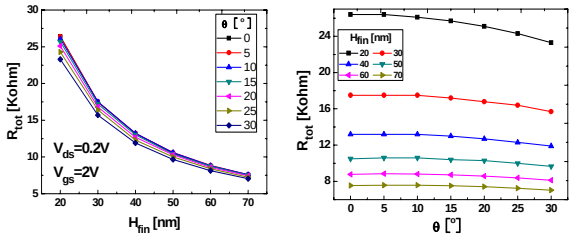


(a)



(b)

Figure 9: Ioff versus (a) Hfin (20~70nm) and (b) θ (0°~30°).



(a) (b)

Figure 10: Total channel resistance versus (a) Hfin (20~70nm) and (b) θ (0°~30°).

Rtot (=Vds/Ids) is defined as the channel resistor in the linear region with small Vds [18-20]. As shown in Fig.10(a), the decrease of Rtot follows a power law relationship with increasing Hfin, while less sensitive to θ. A more explicit is given in Fig.10(b), which shows that Rtot exhibits a slight drop with increasing θ, especially under the condition of large Hfin.

Circuit Performance

We evaluate the deviation angle's impact on circuit in both digital circuits and analog circuits.

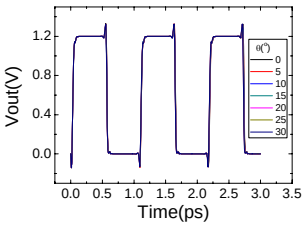


Figure 11: Vout of a 20-stage ring oscillator with different θ (0°~30°).

Fig.11 shows the first 2.5 periods of a 20-stage ring oscillator Vout performance. The period of Vout is of the order of e-12, while the time delay, taking 0° and 10° for instance, is of the order of e-14. In other words, for every 10°, there is 1% time difference in each period, which is accumulative in subsequent periods.

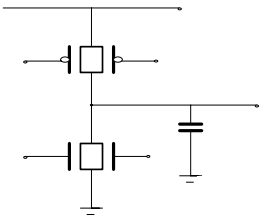


Figure 12: Analog Amplifier circuit.

Fig.12 shows the analog amplifier circuit in which the FinFETs are tested. Fig.13 presents the Vout/Vin-Freq. characteristics when the devices are in ideal situation. Notice that the ideal Vout is 3.4772V in dc operating point.

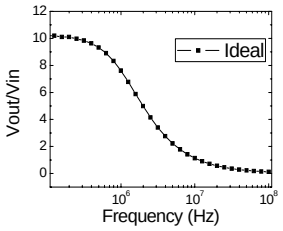


Figure 13: Ideal Vout/Vin-Freq. characteristics

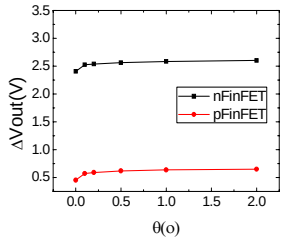


Figure 14 : Vout dc point variation (ΔVout)-θ.

In this analog circuit, pFinFET is effectively a resistance, while nFinFET offers the amplifying function mostly. In this case, the circuit performance is more sensitive to the nFinFET dimension. As in Fig.14, a slight θ change causes the device state shift away from saturation region, which leads to the whole circuit disfunction.

4 CONCLUSION

This paper investigates the sensitivity of FinFET characteristics to the Fin vertical nonuniformity. FinFET is divided into mass of parallel connected unit DG MOSFETs which contribute to the total current respectively. In summary, (1) Fin height variation gives stronger impact on Ids-Vgs and Ids-Vds characteristics than deviation angle. (2) The increment of Vth is smaller with Hfin than with θ. (3) Ion increases linearly with Hfin while insensitive to θ variation. (4) Ioff rises rapidly at small θ and slows down at large θ. (5) The decrease of Rtot follows a power law relationship with the increasing Hfin, while less sensitive to θ. (6) Considering the structure sensitivity analog circuits have, compared to digital circuits, the device Fin vertical nonuniformity is fatal to analog circuits, especially to what are highly sensitive to device dimensions.

5 ACKNOWLEDGEMENT

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REFERENCES

[1] Digh Hisamoto et al, IEEE Transaction on Electron Devices, Vol.47, No.12, 2000, pp.2320–2325.
[2] B. Yu, L. Chang et al，Dig, 2002, pp.251–254.
[3] E. Nowak et al，Dig, 2002, pp.411–414.
[4] Wen-Shiang Liao et al, lEEE 43rd Annual International Reliability Physics Symposium, 2005, pp.541-544.
[5] R. Fernándeza et al，Microelectronics Reliability, Vol.46, 2006, pp. 1608–1611.
[6] Colinge JP, Solid-State Electronics, Vol.48, 2004, pp.897-905.
[7] Yang-Kyu Choi et al，IEDM, 2003, pp.761-763.
[8] Mingchun Tang et al，IEEE Transaction on Electron Devices, Vol.56, No.7, 2009, pp.1543-1547.
[9] Daniel Tekleab et al, IEEE Transaction on Electron Devices, Vol.56, No.10, 2009, pp.2291-2296.
[10] Tetsu Ohtou et al, IEEE Electron Device Letters, 2007, Vol.28, No.8, pp.740-742.
[11] Yu-Sheng Wu et al, IEEE Transactions on Nanotechnology, Vol.7, No.3, 2008, pp.299-304.
[12] Yu-Sheng Wu et al, IEEE Transaction on Electron Devices, Vol.55, No.11, 2008, pp.3042-3047.
[13] Bipul C. Paul et al, IEEE Transaction on Electron Devices, Vol.54, No.9, 2007, pp.2369-2376.
[14] Hari Ananthan et al, IEEE Transaction on Electron Devices, Vol.53, No.9, 2006, pp.2151-2159.
[15] Hans J. Mattausch et al, IEEE Electron Device Letters, Vol.30, No.8, 2009, pp.873-875.
[16] Toshifumi Irisawa et al, IEEE Transaction on Electron Devices, Vol.56, No.8, 2009, pp.1651-1658.
[17] Lining Zhang et al, MIXDES 2008, June 21-23 Poznan, Poland, 2008, pp.367-372.
[18] Takashi Matsukawa et al, IEEE Electron Device Letters, Vol.30, No.4, 2009, pp.407-409.
[19] Dominique Fleury et al, IEEE Electron Device Letters, Vol.30, No.9, 2009, pp.975-977.
[20] Junsoo Kim et al, IEEE Transaction on Electron Devices, Vol.55, No.10, 2008, pp.2779-2784.