# Underlap Channel Nanoscale Dopant-Segregated Schottky Barrier SOI MOSFET for Low-Power Mixed Signal Circuits

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## ABSTRACT

In this paper, underlap channel dopant-segregated Schottky barrier (DSSB) SOI MOSFET has been proposed, in which the increased effective channel length ($L_{eff}$) due to underlap channel at both source/drain (S/D) sides reduces the leakage currents, short-channel effects and the parasitic capacitances as compared to overlap channel DSSB SOI MOSFET. Although in strong inversion the voltage drop across the underlap lengths at S/D reduces the drive current of the proposed device, in weak inversion defined at $I_D$ = 5 μA/μm at $V_{DS}$ = 0.5 V the analog figures of merit (FOM) of this device are improved. Further, the mixed-mode simulation results of CMOS inverter and the ring-oscillator circuits show that, at lower supply voltage (i.e.$V_{DD}$ = 0.5 V), both power dissipation (PD) and the delay in the case of proposed device are reduced as compared to overlap device. Thus, the improved analog FOM and reduced PD and the delay at lower supply voltage makes the proposed underlap device suitable for low-power mixed-signal circuits.

***Keywords***: Schottky barrier, underlap channel, mixed-signal circuits, SOI MOSFET, low-power

## 1 INTRODUCTION

Silicided S/D silicon-on-insulator (SOI) is an emerging technology due to its compatibility with conventional CMOS fabrication flow and the reduced S/D series resistance ($R_{SD}$) at thin-film [1]. However, the requirement of zero Schottky barrier (SB) at the metal-semiconductor (M-S) junction formed between metal S/D and the channel is a major problem in this technology. Recently, it has been shown that, by using the low-SB silicide materials such as $ErSi_{1.7}$ for n-channel MOSFET (NMOS) and PtSi for p-channel MOSFET (PMOS) and by segregating a thin highly doped Si layer at the M-S junction, the reduced SB width at this junction improves the drive current [2]. This leads to a promising device structure known as dopant-segregated Schottky barrier (DSSB) SOI MOSFET. Significant work has been carried out on this device through experiments [2]-[4] and by simulations [5]-[7]. However, the mixed-signal circuit performance of this device has not been explored to the best of our knowledge.

Further, inspite of reduction in short-channel effects (SCEs) due to thin-film and reduced $R_{SD}$ due to metal S/D, the parasitic capacitances due to gate-to-S/D (G-S/D) overlap and the gate induced drain leakage (GIDL) due to inter-band tunneling and trap-assisted tunneling increases the delay and the standby power dissipation of this device. To address this problem, non-overlapped G-S/D (commenly known as underlap channel) DSSB SOI MOSFET has been proposed in this work, in which the combined advantages of DSSB SOI MOSFET (reduced $R_{SD}$ at thin-film, CMOS compatibility and reduced thermal budget) and G-S/D underlap structure (reduced GIDL, reduced parasitic capacitances and bias dependent effective channel length) [8] makes the proposed underlap device suitable for low-power mixed-signal CMOS circuits.

The organization of rest of the paper is as follows, Section 2 presents the device structures and the simulation methodology used in this work. Section 3 compares the DC performance, analog FOM and the CMOS logic circuit performance of overlap and underlap channel DSSB SOI MOSFETs. Finally the conclusion is given in Section 4.

## 2 DEVICE STRUCTURES AND SIMULATION SETUP

The device structures and the parameters used in two-dimensional MEDICI simulator [9] are shown in Fig. 1 and Table 1 respectively. The doping densities used in the body-region, substrate and the segregation layer of NMOS and PMOS are same with only change in the type of Si. The range of physical gate length ($L_G$) and the gate oxide thickness have been considered as per the ITRS-2009 high performance logic technology specifications [10]. The dopant segregation length ($L_{DSL}$) is defined as the distance between the M-S junction edge and the p-n junction edge where the doping in the segregation layer drops to

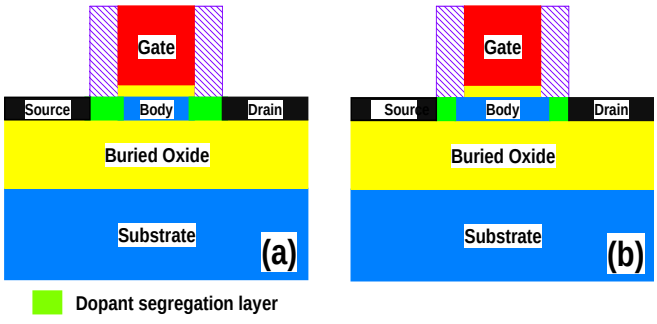


Figure 1: (a) Overlap channel and (b) proposed underlap channel DSSB SOI MOSFETs used in simulations.

| Parameter | Unit | Parameter Value |
|---|---|---|
| Physical gate length ( $L_G$) | nm | variable |
| Gate oxide thickness ( $T_{ox}$) | nm | 1 |
| Silicon film thickness ( $T_{Si}$) | nm | 8 |
| Buried oxide thickness ( $T_{BOX}$) | nm | 50 |
| Substrate thickness ( $T_{substrate}$) | nm | 100 |
| Spacer thickness ( $T_{spacer}$) | nm | 10 |
| Doping in segregation layer ( $N_{DSL}$) | $cm^{-3}$ | $1\times10^{20}$ |
| Channel doping ( $N_{ch}$) | $cm^{-3}$ | $1\times10^{15}$ |
| Underlap channel length ( $L_{UN}$) | nm | 5 |
| Overlap channel length ( $L_{OV}$) | nm | 1 |
| Electron SB height for NMOS ($\Phi_{bnN}$) | eV | 0.3 |
| Hole SB height for NMOS ($\Phi_{bpN}$) | eV | 0.82 |
| Electron SB height for PMOS ($\Phi_{bnP}$) | eV | 0.82 |
| Hole SB height for PMOS ($\Phi_{bpP}$) | eV | 0.3 |
| Supply voltage ( $V_{DD}$) | V | 1 |
| Saturation threshold voltage ( $V_{TSAT}$) | V | 0.2 |

Table 1: Device parameters used in MEDICI simulations.

$1\times10^{15}$ $cm^{-3}$. In order to form the G-S/D underlap and overlap structures the $L_{DSL}$ has been varied by changing the lateral doping straggle in the segregation layer [6]. The $L_{DSL}$ of 5 nm at the S/D of the proposed device and 11 nm at the S/D of overlap channel DSSB SOI MOSFET forms an underlap channel of length 5 nm and an overlap channel of length 1 nm at the S/D of the proposed underlap and overlap channel DSSB SOI MOSFETs respectively.

Since the carriers in the channel are mainly transported due to drift-diffusion and at the M-S junction are by tunneling, both drift-diffusion and SB tunneling models have been incorporated along with the mobility models. Further, to capture the GIDL effect band-to-band tunneling and trap-assisted tunneling models from the MEDICI have been enabled. To extract the analog FOM and to evaluate the performance of common-source (CS) amplifier, the small-signal ac analysis by considering source as a ground terminal has been carried out for both overlap and underlap channel DSSB SOI MOSFETs.

## 3 RESULTS AND DISCUSSION

### 3.1 DC Performance

Fig. 2(a) shows $I_D$ vs $V_{GS}$ characteristics in linear and log scale for overlap and underlap channel NMOS/PMOS

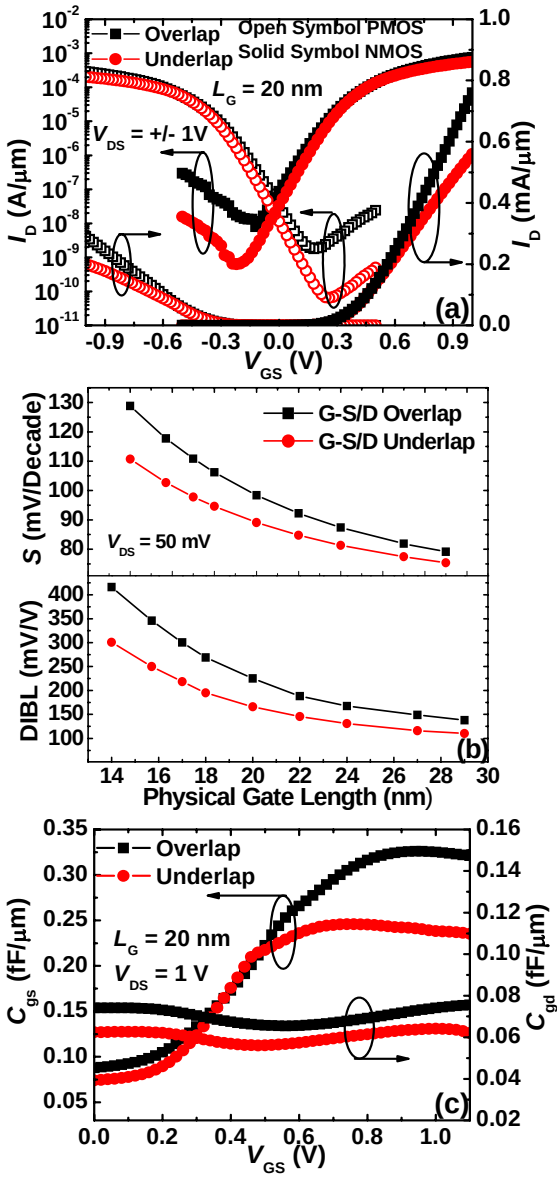


Figure 2: (a) $I_D$ vs $V_{GS}$ characteristics, (b) variation of $S$ and DIBL with $L_G$ and (c) variation of $C_{gs}$ and $C_{gd}$ with $V_{GS}$ for overlap and underlap channel DSSB SOI MOSFETs.

devices. From the figure it can be seen that, although due to underlap at S/D the voltage drop across the underlap lengths reduces the drive current in both NMOS and PMOS underlap devices, the increased $L_{eff}$ due to underlap channel reduces the off-state leakage and the GIDL of these MOSFETs as compared to overlap channel DSSB SOI MOSFETs. Further, the increased $L_{eff}$ in the proposrd underlap device reduces the subthreshold swing ($S$) and the drain induced barrier lowering (DIBL) of this device as compared to overlap channel DSSB SOI MOSFET (See Fig. 2(b)). Furthermore, from Fig. 2(c) it can be seen that, due to null overlap capacitance in an underlap device the parasitic capacitances namely gate-to-source ($C_{gs}$) and gate-to-drain ($C_{gd}$) are also significantly lower as compared to

overlap channel DSSB SOI MOSFET. Thus, the reduced off-state leakage, GIDL, $S$, DIBL, $C_{gs}$ and $C_{gd}$ makes the proposed underlap device suitable for future scaling.

## 3.2 Analog Performance

The key FOM which determines the analog circuit performance of a MOSFET are the transconductance ($g_m$), output conductance ($g_d$), intrinsic gain ($g_m/g_d$) and the transconductance generation factor ($g_m/I_D$) [11]-[12]. Since $g_m$ represents the amplification delivered by the device and $I_D$ represents the power dissipated to obtain that amplification, $g_m/I_D$ can be considered as a quality factor for analog applications [12]. Further, from the models of long channel MOSFET theory it has been shown that, $g_m/I_D$ is a strong function of $S$ [11]. From Fig. 3(a) it can be seen that in weak inversion region both $g_m/g_d$ and $g_m/I_D$ are significantly improved in the proposed device as compared to overlap channel DSSB SOI MOSFET. This is mainly because of the increased $L_{eff}$ which reduces both $S$ and $g_d$ of the proposed device. However, in strong inversion region the increased $R_{SD}$ due to voltage drop across the underlap lengths reduces $g_m$ and hence $g_m/g_d$ and $g_m/I_D$ of the proposed underlap device. Moreover, inspite of reduced $g_m$ due to increased $R_{SD}$ in strong inversion region defined at $V_{DS} = V_{GS} = 1$ V, in weak inversion region defined by varying $V_{GS}$ to achieve $I_D = 5$ µA/µm at $V_{DS} = 0.5$ V, $g_m$ in the case of proposed underlap device is higher as compared to overlap channel DSSB SOI MOSFET (See Fig. 3(b)).

To evaluate the analog circuit performance of both underlap and overlap n-channel DSSB SOI MOSFETs in weak and strong inversion regions small-signal AC analysis of CS amplifier has been carried out. The results of this implementation show that, although in strong inversion region the improved $g_m$ improves the gain-bandwidth product (GBP) of CS amplifier based on overlap channel DSSB SOI MOSFET, in weak inversion region due to reduced $g_d$ and the parasitic capacitances the GBP in the case of proposed underlap device is larger as compared to overlap device. This clearly shows that, the proposed underlap channel DSSB SOI MOSFET is a suitable candidate for low-power analog circuits.

## 3.3 CMOS Logic Performance

In order to evaluate the CMOS logic performance of an overlap and underlap channel DSSB SOI MOSFETs mixed-mode device/circuit simulations have been carried out using the MEDICI simulator. To obtain the symmetrical voltage transfer characteristics and to maximize the noise margins the width of PMOS transistor has been taken twice as that of the NMOS transistor. Further, to achieve the lower short-circuit PD the input pulse applied at the first inverter stage has been selected in such a way that, it has smaller rise and fall times as compared to inveter rise and fall times [13]. To measure the average PD, a small-circuit as shown in Fig. 4(a) has been used, in which the capacitor $C_1$ integrates the

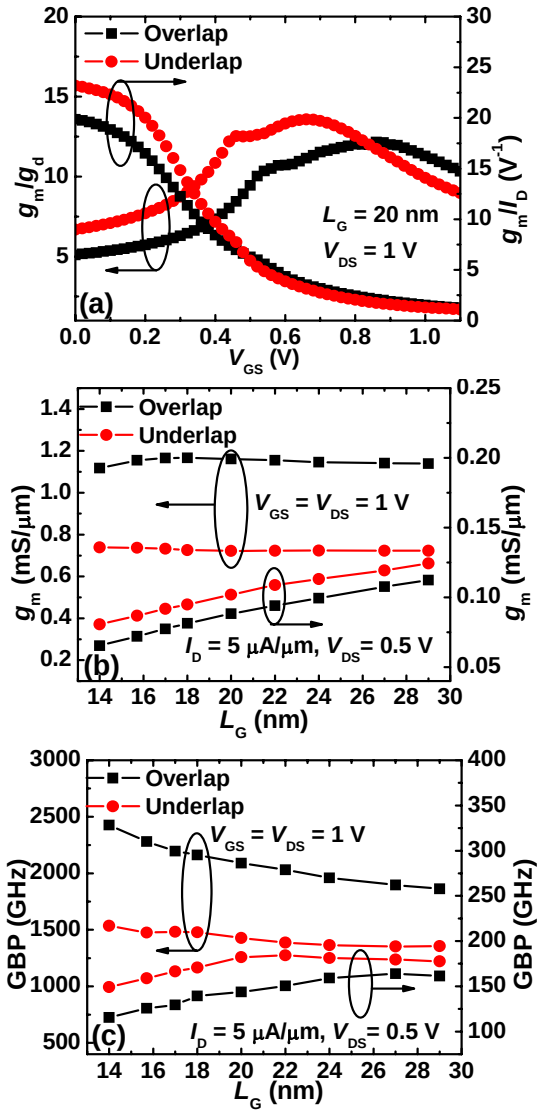


Figure 3: (a) Variation of $g_m/g_d$ and $g_m/I_D$ with $V_{GS}$, (b) variation of $g_m$ with $L_G$ and (c) variation of gain-bandwidth product (GBP) with $L_G$ for overlap and underlap channel DSSB SOI MOSFETs.

switching current ($I_{SW}$) passing through the second inverter stage and the current-controlled-current-source (CCCS) whose gain ($K$) is unity measures the average PD [13]-[14]. The resistance $R_1$ has been used for DC convergence and is chosen as high as possible to minimize the leakage.

From Fig. 4(b) and Fig. 4(c) it can be seen that, inspite of reduced parasitic capacitances in the proposed device, the reduced $I_{ON}$ due to increased $R_{SD}$ at higher supply voltage (i.e. $V_{DD} = 1$ V) increases the delay in the CMOS inverter based on this device as compared to overlap channel DSSB SOI MOSFET based inverter. However, due to reduced GIDL and the subthreshold leakage in the proposed underlap device, PD in the CMOS inverter based on this device reduces as compared to overlap channel DSSB SOI MOSFET based CMOS inverter.

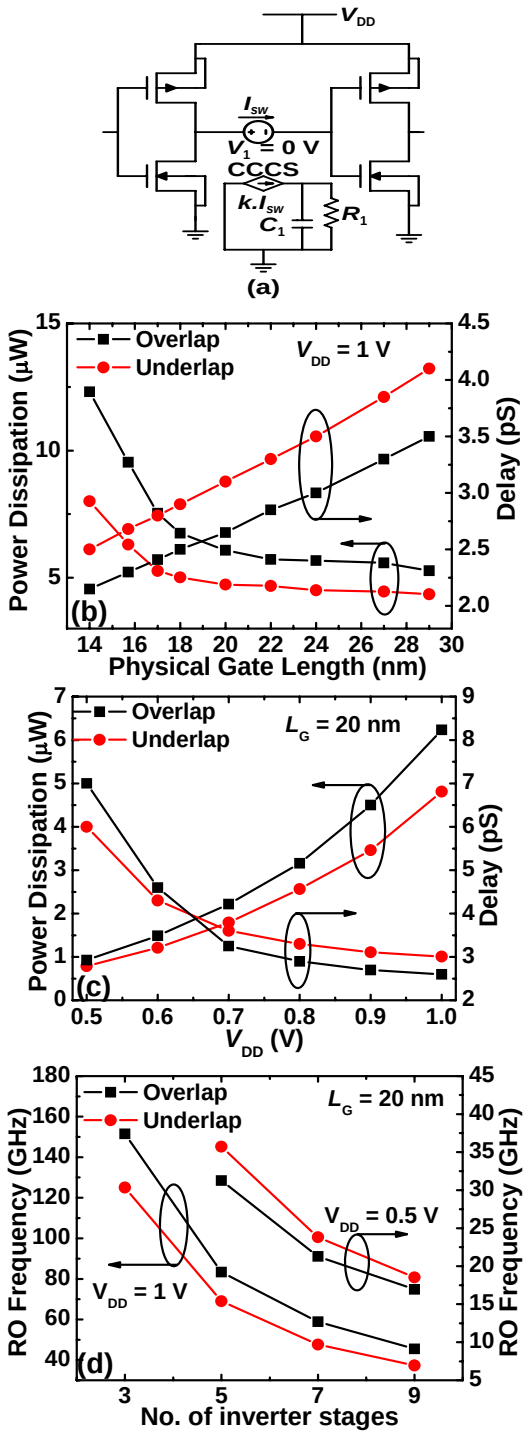


Figure 4: (a) Power measurment circuit used in MEDICI simulations. (b) Variation of PD and delay with $L_G$ , (b) variation of PD and delay with $V_{DD}$ and (c) variation of RO frequency with number of inverter stages for overlap and underlap channel DSSB SOI MOSFETs.

Further, from Fig. 4(c) it can be seen that, at lower supply voltage (i.e. $V_{DD}$ = 0.5 V), the delay in the case of proposed underlap device is also lower as compared to overlap device. This is attributed to the reduction in the parasitic capacitances of an underlap DSSB SOI MOSFET. In addition to this, from Fig. 4(d) it can be seen that, inspite of lower ring-oscillator (RO) frequency in the case of proposed underlap device at $V_{DD}$ = 1 V, the RO frequency at $V_{DD}$ = 0.5 V is higher as compared to overlap channel DSSB SOI MOSFET. This clearly shows that the proposed underlap channel DSSB SOI MOSFET has also scope for low-power CMOS logic circuits.

## 4 CONCLUSION

An underlap channel dopant-segregated Schottky barrier SOI MOSFET has been proposed in this work. The simulation results show that, with an underlap channel at both source and drain the increased effective channel length reduces the short-channel effects, off-state leakage, GIDL and the parasitic capacitances of this device as compared to overlap channel DSSB SOI MOSFET. However, in strong inversion region the voltage drop across the underlap lengths reduces the effective gate voltage and hence reduces the on-state drive current in the proposed device. Although the increased series resistance in the proposed device reduces on-state drive current in strong inversion region, the improved analog figures of merit in weak inversion region and reduced inverter power dissipation and the delay at lower supply voltage makes the proposed underlap device suitable for low-power mixed signal circuits.

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