Variability Study of Silicon Nanowire FETs

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1 ABSTRACT

In this work, impact of device variability for silicon nanowire FETs is assessed and SRAM design implication is presented based on 3-D numerical simulation. Both the conventional and junctionless nanowire FETs are shown to be sensitive to structural variation whereas the former is more tolerable. Both the circular wire and non-circular wire cases for feasible SRAM design with a focus on read noise margin are included in our study.

Keywords: Nanowire FETs, SRAM, SNM

2 INTRODUCTION

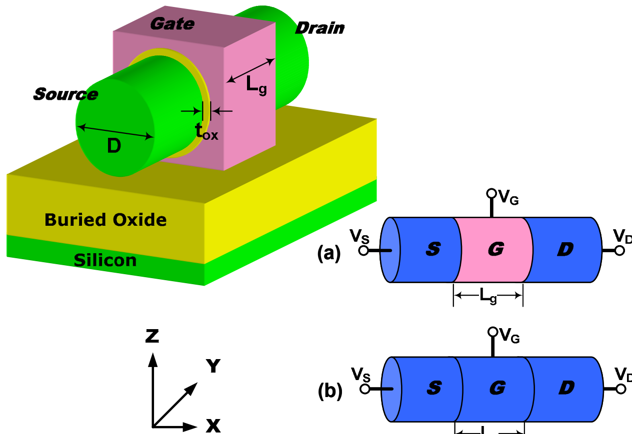

Figure 1: 3-D view of (a) conventional and (b) junctionless nanowire FETs.

Among emerging multiple-gate CMOS devices, Si-based gate-all-around (GAA) nanowire FETs have drawn much of attention due to excellent gate controllability in suppressing short-channel effects (SCEs) for ultimate device scaling. Based on the circular and gate-around structure, the performance could be enhanced significantly, as compared with conventional MOS devices [1]-[3]. Recently, a junctionless (JL) FET device structure that has a homogeneous channel with excellent subthreshold swing was demonstrated experimentally [4]. Though the nanowire FETs are shown to be promising, the issues associated with actual fabrication such as gate coverage and non-circular structure should be taken into account. In this paper, we analyze the process-variability effect of silicon nanowire FETs on SRAM cells at/beyond the 14 nm node using 3-D TCAD simulation [5].

3 DEVICE STRUCTURE VARIATON

3.1. Nominal device structure

Figure 1 shows the 3-D structure view of the nanowire FET. Following the off-state leakage current (I_{off}) target below 14 nm technology node [6], the dimension of the nominal device is defined as follows: L_g = 10 nm, D (diameter) = L_g/2 = 5 nm, and t_{ox} (EOT) = 0.6 nm, with an undoped channel in GAA FETs and a highly doped channel (8×10^{19} cm^{-3}) in junctionless nanowire FETs.

Figure 2 shows I_{DS}-V_{GS} characteristics of nominal GAA n/p-FETs and junctionless nanowire nFET. I_{off} is conformed to ITRS by gate work function adjustment. As can be seen, nFET and pFET show symmetrical property and nearly ideal S.S. whereas the junctionless nanowire nFET shows lower on-state current due to more distributed carriers from the surface.

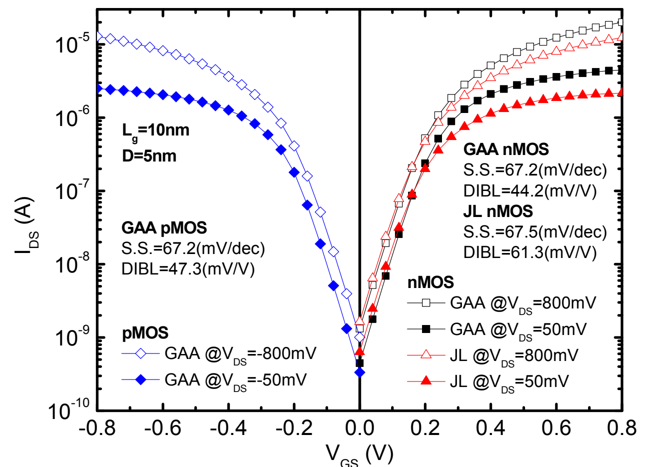

Figure 2: I_{DS}-V_{GS} characteristics of nominal GAA n/p-FETs and junctionless nanowire nFET.

3.2. Nonideal structure

Accounting for nonideal structure variation, the diameter and non-circular (or ellipse) variability are modeled with two factors (D and W_{Si}), as shown in Figure 3. For the non-circular case, the height of Si-film (H_{Si}) is fixed and the width of Si-film (W_{Si}) could be varied by lithography inaccuracy.

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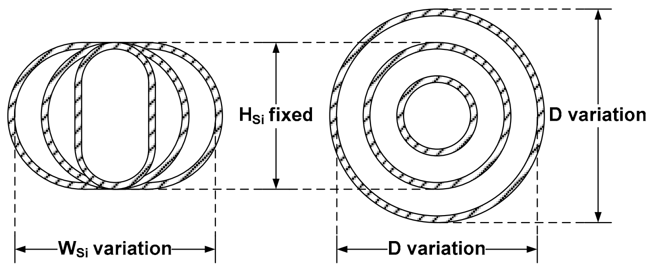
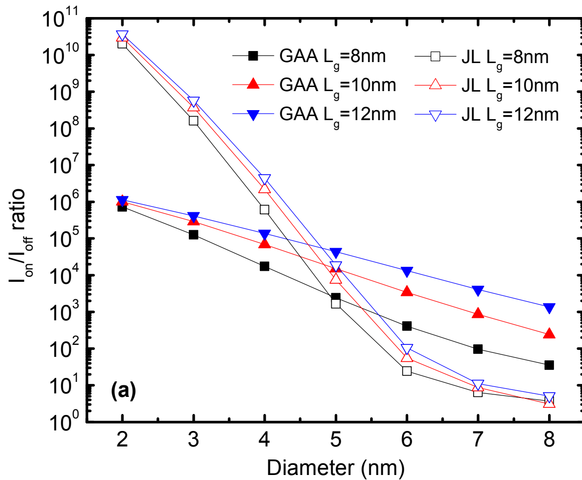


Figure 3: Structure variation with diameter (D) and channel width (W_{Si}).

Figures 4(a) and (b) show TCAD-predicted I_{on}/I_{off} ratio against D and W_{Si}, respectively, for GAA and JL devices. JL devices show higher sensitivity to D because the dependency of V_t on D is more severe in JL. The sensitivity to W_{Si} is relatively milder than to D for all cases due to the higher charge area of Si-body film. The GAA case is more tolerable to structure variation than the JL one. Note that extremely-higher I_{on}/I_{off} for JL implies that JL can be applied to very low voltage/power circuits. Proper design of wire dimension for JL FETs is essential but JL can provide broad range of multiple V_t devices in various high-performance and low-power applications.



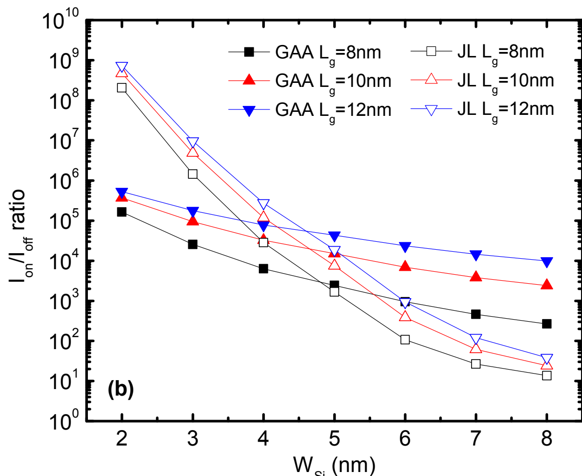


Figure 4: Simulated I_{on}/I_{off} ratio in wire structural variation.

4 CIRCUIT VARIABILITY ASSESSMENT

Based on the methodology for devices, we further assess the variability from circuit perspective using Read SNM for 6T-SRAM as an example. Figure 5 shows a typical 6T-SRAM cell schematic, composed of single-wire nanowire FETs. For our investigation, two types of SRAM design were included, i.e. conventional GAA 6T-SRAM, and novel 6T-SRAM with M_5 and M_6 replaced with JL devices [7]. In next two sections, we discuss the impact of diameter and non-circular variation in conventional and novel SRAM.

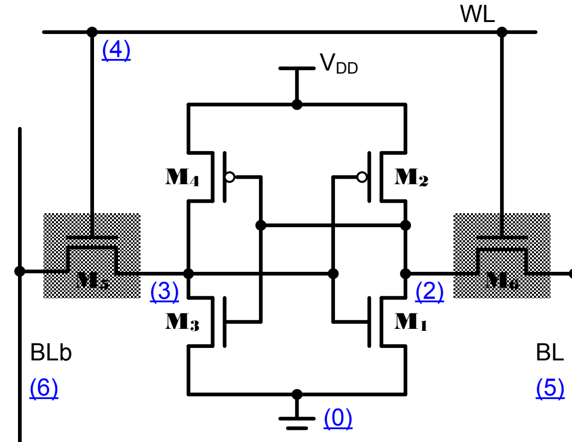


Figure 5: A typical 6T-SRAM cell schematic with all single-wire nanowire FETs.

4.1. Conventional SRAM

Figure 6 and Figure 7 show TCAD-predicted butterfly curves of conventional GAA SRAM in diameter and body film variations, respectively. Due to insensitivity of GAA transistors to variability, RSNM is not much influenced. Comparison with D and W_{Si} variaton, the non-circular cases are not much influenced. Because of H_{Si} is fixed as nominal case, that can provide gate to gate coupling in vertical direction. Hence, the non-circular cases can keep good gate control in vertical that can able to keep RSNM in SRAM, too. In diameter variation cases, there is less gate coupling in large diameter case. Nevertheless, the gate control capability would be improved in tiny diameter as 2 nm. The RSNM would be improved significantly.

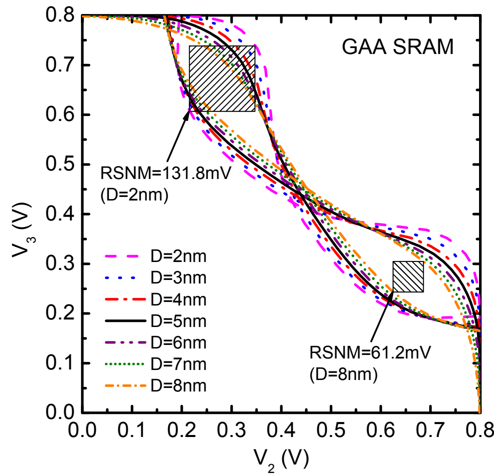


Figure 6: Predicted RSNM with different diameters in single GAA SRAM.

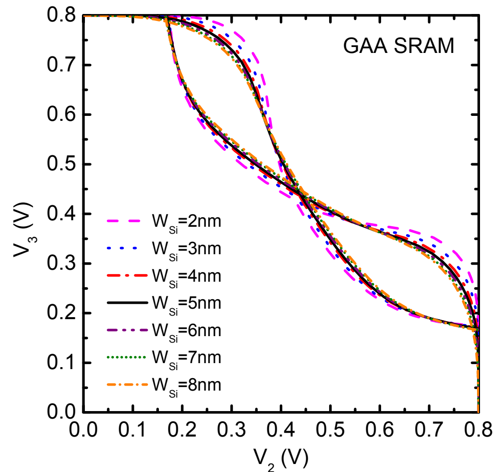


Figure 7: Predicted RSNM with different body widths in single GAA SRAM.

4.2. Novel SRAM

In nominal cases, by using JL FETs for M_5 and M_6 in the novel SRAM cell, RSNM is dramatically improved from 89.4 mV of conventional design to 141.2 mV because of higher resistivity of JL FET as compared with that of nominal GAA FET. However, as shown in Figure 8 and Figure 9, due to higher I_{on}/I_{off}, RSNM with JL FETs is significantly improved when D and W_{Si} are reduced. In addition, impact of W_{Si} variation is not as severe as that of D variation. Note that the design with JL FET is very sensitive to siliocn variation. Hence, the novel SRAM may need special care when dealing with variation issue even though it is advantageous in RSNM.

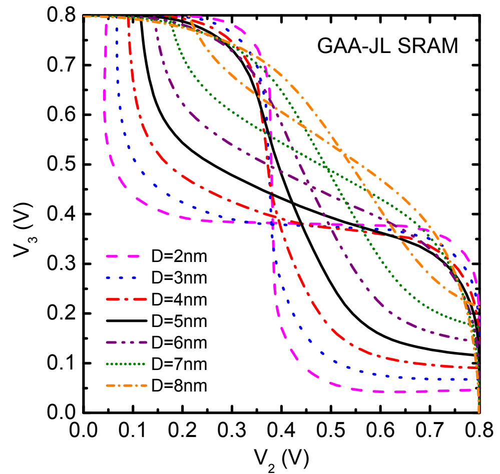


Figure 8: Predicted RSNM with different diameters in single GAA-JL SRAM.

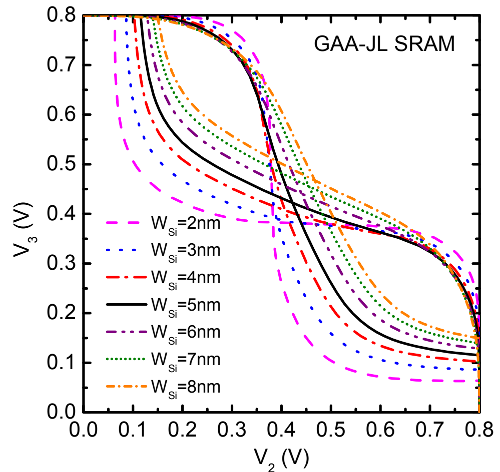


Figure 9: Predicted RSNM with different body widths in single GAA-JL SRAM.

4.3. Analysis and discussion

Figure 10 compares RSNM extracted from Figures 6-9. Again, though the variability tolerance is low for the novel scheme, it has a great advantage in RSNM for both ideal circular and non-ideal (practical) wire geometry. Note that the devices are optimized in D = 5 nm and W_{Si} = 5 nm. As D is larger than 7 nm, RSNM of the novel design could be lower due to more SCEs. Interestingly, even though non-circular structure is inevitable from process variation [8], the sensitivity of RSNM for the case (i.e. different H_{Si} and W_{Si}) is less than the ideal-case counterpart (i.e. different D).

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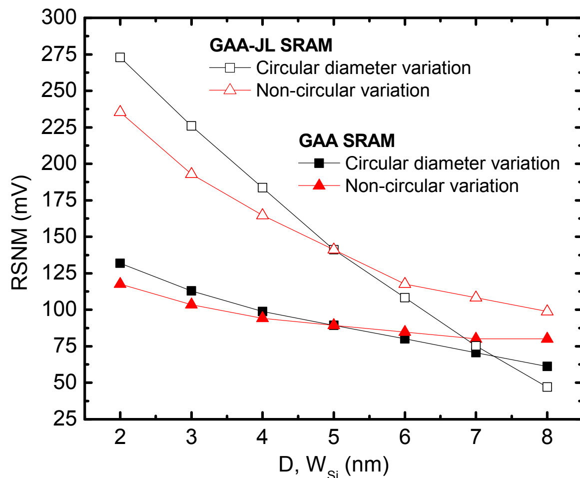

Figure 10: Predicted RSNM vs. wire diameter/body width.

5 CONCLUSION

Device variability study for silicon nanowire FETs and implications on noise margin of SRAM was presented based on 3-D numerical simulation. Both the conventional and junctionless nanowire FETs were shown to be sensitive to structural variation whereas the former is more tolerable. Circuit implications from wire diameter and non-circular wire variations for viable SRAM design were included as well.

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