# Reliability Analysis of Low Temperature Low Pressure Ag-Sinter Die Attach

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## ABSTRACT

The amount of heat to be dissipated from power electronics and microprocessors increases more and more. Therefore new interface materials with high electrical and thermal conductivity have to be considered. Silver is one of a few materials which can fulfil these demands. New low temperature, low pressure Ag-Sinter technologies allow it to use Silver as die attach material instead of solder or glue. Even though silver has excellent thermal and electrical properties, thermo-mechanical reliability aspects have to be considered. In this paper the thermo-mechanical reliability of chip-on-board (COB) assemblies for power applications are studied by experiment and simulation. Thereby the main focus is set on the characterization methods and low cycle fatigue failure behaviour of the die-attach material under thermal cycling conditions. Part of the work has been accomplished within the running EU Project "Nanopack".

***Keywords***: sinter silver, die attach, reliability, nano-indentation, thermal interface

## 1 INTRODUCTION

The thermal interface resistance is one of the major bottlenecks in advanced thermal packaging solutions. Over the last couple of years this trend has become more and more apparent as well as the need for new developments in advanced thermal technology [1-3].

Previous investigations have shown the excellent thermal conductivity (close to bulk silver) and high mechanical strength of sinter silver [4]. These results are very promising for using this material as die attach in high power electronic devices.

On integrating microelectronic systems with this technology it is of great importance to assure the function of these systems and its individual constituents. Thus it is indispensible to analyze their reliability systematically in order to generate lifetime models and design guidelines for lifetime prediction. These models need to reflect the physics-of-failure which have to be reproduced consistently by experiment and simulation. Therefore this paper analyses the stresses and strains of the die attach after processing and under external thermal loads relevant for the envisaged field of application (automotive). As this work considers a new technology in development in a running project, this publication addresses a systematic approach drawing upon both simulation and experimental methods.
First modified COB test vehicles were fabricated and the sinter silver was characterized. Hence materials may behave differently in their mechanical properties if fabricated in smaller dimensions, this characterization is a challenge. Mostly no standard methods can be applied due to the impossibility to fabricate standard test specimens. Therefore, methods like nanoindentation conjunction with FE simulations are applied to determine elasto-plastic material behavior in. This is necessary as the desired material parameters (like Young's modulus and yield stress) cannot be obtained directly but have to be extracted from the simulation.

Then, an FE-model of the COB is generated and material data is implemented. Simulation runs allow to locate and monitor accumulating plastic strain over the process steps and through several thermal cycles. These response parameters can be used to generate a lifetime model for these kind of die attach (e.g. by a Coffin-Manson or Paris-Erdogan approach) when compared to experimental lifetime data.

## 2 SPECIMEN FABRICATION

We used 1.5 mm thick plates of oxygen-free copper and plated a 3 µm thick silver layer onto the upper side. The Ag paste layer was applied by stencil printing of an Ag suspension by using a standard printing machine. Two different stencil thicknesses of 75 and 150 µm were used to achieve different bond thicknesses. After bonding the layer thickness of the die attaches amounts to approximately 22µm and 38µm.

IGBT chips of 130 µm thickness with Ti/Ni/Ag metallization were placed into the printed silver paste after a short drying period. The backside was covered with a polymer sheet then force and temperature was applied to perform the sintering. A sintering temperature of 230°C and a bond pressure of 40 MPa were selected. The assemblies are depicted in figure 1.

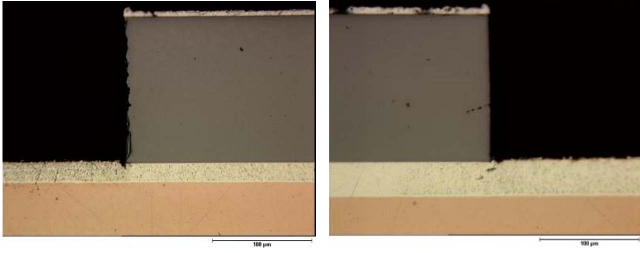

Fig. 1: Cross section of the sintered IGBTs on copper substrate. Stencil thickness of 75µm (left) and 150µm (right) represents 22µm and 38µm in bonded state.

For reliability investigations different geometries are needed. Specimens with die attach thicknesses of 22µm and 38µm as well as chip sizes of 6×6mm² and 9×9mm² were fabricated.

## 3 MATERIAL CHARACTERIZATION

First, the material properties of the sinter silver layers need to be characterised. Therefore, the fabricated chip assemblies with a die attach thickness of 22µm and 38µm were cross-sectioned and polished.

As discussed in the introduction the fabrication of specimens of that thickness for tensile testing is very complicated. Therefore we have opted for material characterisation by nano-indentation. The measurements were carried out normal to the cross-sections of the die attach.

For the determination of correct values, the nano-indenter undergoes first a calibration process [5]. For that purpose indents in a material of known elastic modulus are made (fused silica). In the first step this calibration is applied to level out the load frame compliance using large area indents. After correction for the load frame compliance, the relation of contact stiffness and indent area vs. indentation depth $h_c$ can be represented by equation 1.

$$A(h_c) = \frac{\pi}{4E_r^2}\left(S(h_c)\right)^2 \qquad (1)$$

Here, $E_r$ denotes the known Young´s modulus of the calibration sample and $S$ the contact stiffness recorded as tangent on the force displacement curve upon unloading, therefore containing information about the elastic response of the layer. An underlying assumption for this formula is, that a Berkovich or Vickers indenter can be approximated by an indenter shape of rotational symmetry, leaving an indent-area equivalent to $A = \pi r^2$. The area versus indentation depth curve can be fitted by a polynomial expression (equation 2).

$$A(h_c) = C_0 h_c^2 + C_1 h_c + C_2 h_c^{1/2} + C_3 h_c^{1/4} + C_4 h_c^{1/8} + C_5 h_c^{1/16} \qquad (2)$$

Using this equation 2, we can plot $h_c(r)$ and thus retrieve the actual indenter tip shape function, which is then, mapped onto the FE-model depicted in figure 6.

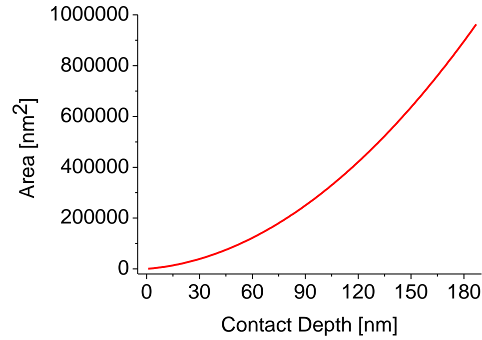


Fig. 2: Calibration curve for Berkovich diamond-tip nanoindenter on fused silica

After the calibration process, the nanoindentation measurements were carried out on the die attach with a layer thickness of 22µm and 38µm. The results produced by indentation with constant maximum force of 2mN are depicted below in figure 3, using equation 1 for the elastic modulus $E_r$ and in figure 4 using equation 3 for the hardness H.

$$H = \frac{P}{A(h_c)} \qquad (3)$$

Here, $P$ is the indentation force.

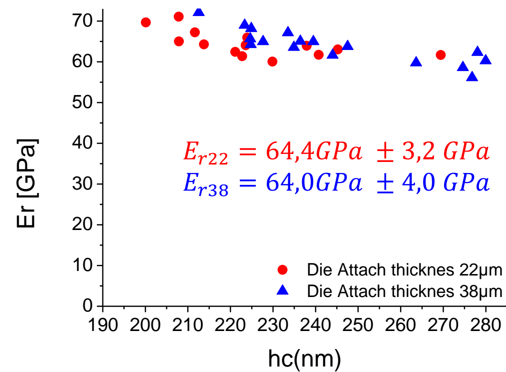


Fig. 3: Reduced E-Modulus calculated from equation 1

Owing to the fact that we want to get pure bulk behaviour from the indentation measurements the indents have to be as small as possible but big enough to avoid surface and interface effects. Experience has shown that indentation depths in the range of 250nm done with a Berkovich indenter are sufficient for this kind of situation.


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Due to scatter of the measurements a pattern of 20 indents is used to get a trustable mean value of the Young´s modulus. Figure 5 shows the positions of the indentations and the corresponding modulus map of the 38µm die attach. The modulus map was manually overlaid on the topology scan made by the indenter after the indentation procedure. On the bottom left corner of the pattern two indents with small values in the range of 15 GPa can be pinpointed. This effect is probably caused by a cavity under the surface of indentation. These points are neglected for the following characterization procedure.

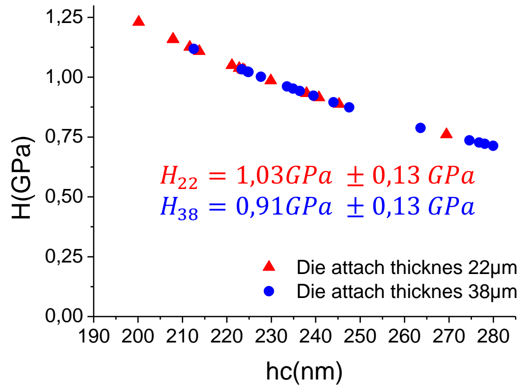


Fig. 4: Hardness calculated from standard equation 3

However, the main target of the indentation tests is a statement about onset and evolution of plasticity, which cannot be obtained from modulus or hardness values. So a combined experimental-numerical approach is needed to extract the desired material properties.

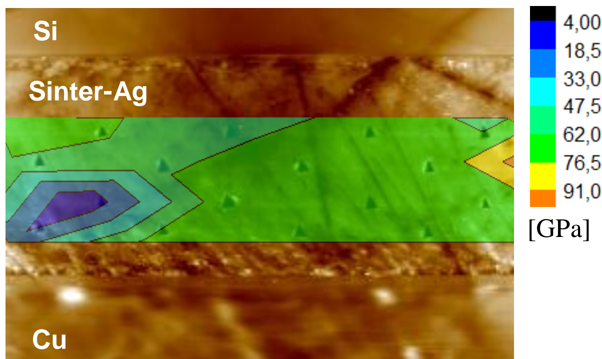


Fig. 5: Surface topography and modulus map of the 38µm die attach indentation region

We have generated a FE model of rotational symmetry (figure 6) to mimic the nanoindentation process. Rotational symmetry seems appropriate, as the whole calibration process hinges upon that assumption. From equation 2 the indenter tip shape function $h_c(r)$ was plotted and transferred on to the model geometry.

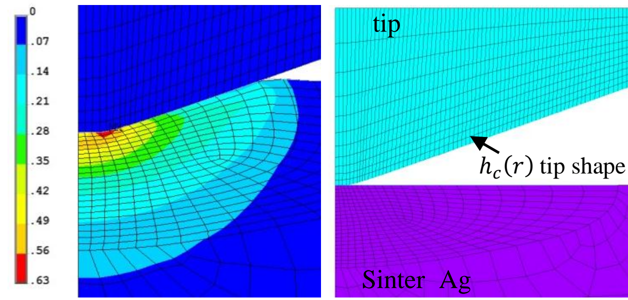


Fig. 6: FE-Model for nanoindentation, rotational symmetry, and resulting plastic strain (Sinter Ag at 2mN). One notices the complex strain distribution below the tip.

As constitutive equation for metal plasticity representation a four-parameter Ramberg-Osgood model [6,7] was implemented in terms of a multilinear elastoplastic material law with kinematic hardening (see figure 7).

$$\varepsilon = \frac{\sigma}{E} + \alpha \frac{\sigma_{0.2}}{E} \left( \frac{\sigma}{\sigma_{0.2}} \right)^n \tag{4}$$

Here, $E$ is the Young´s modulus, $\sigma_{0.2}$ is the stress at 0.2% plastic strain and $\alpha$ as well as $n$ are constants.

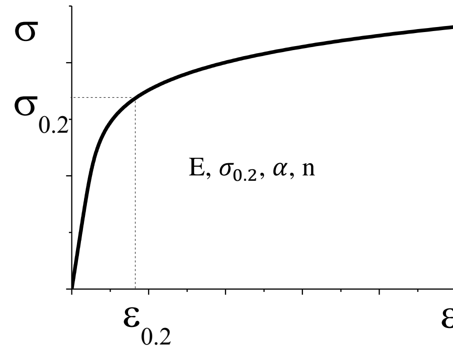


**Fig. 7 Schematic of the Ramberg-Osgood approximation to describe elasto-plastic behaviour**

Now simulations were run parametrically with respect to these four parameters until an optimum fit to the indentation depth versus force curve was found. The optimization procedure started with fitting the E-modulus first, a quantity which governs the unloading behaviour. Then yield stress and the coefficients $\alpha$ and $n$ were fit. As reference data for fitting all valid measured force-depth curves were averaged. The results of this fitting procedure are displayed in figure 8 and table 1.

| **Material** | **E-Modulus [GPa]** | $\sigma_0$ **[MPa]** | $\alpha$ | $n$ |
|---|---|---|---|---|
| SinterAg | 64.0 | 181.0 | 0.752 | 4.16 |

Table 1: Ramberg-Osgood coefficients received from Fit

A very good fit is obtained for the unloading curve, whereas the loading part has still room for improvement. This is believed to be due to the porosity of the Ag-sinter material which is not considered in the FE-Model. But this needs to be checked for.

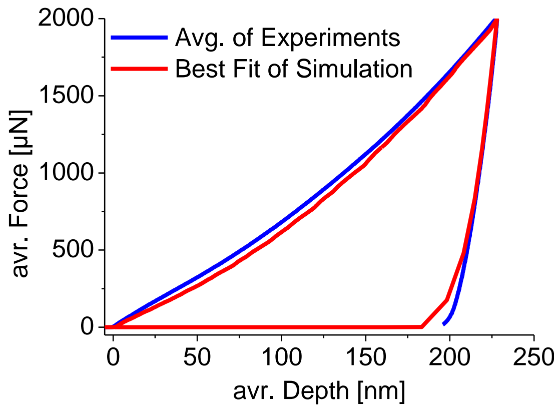


Fig. 8: Correlation of experiment and simulation for nano-indentation in sinter Ag.

## 4 THERMAL CYCLING TEST IN SIMULATION AND EXPERIMENT

In parallel to the simulation, test specimens as described in section 2 underwent thermal cycling according to figure 9. Unfortunately only one set (9×9mm² die with die attach thickness of 22µm) of experiments seems to produce trustworthy results. The reason for this behaviour might be some unsolved problem in the fabrication process, which have to be tackled in the near future.

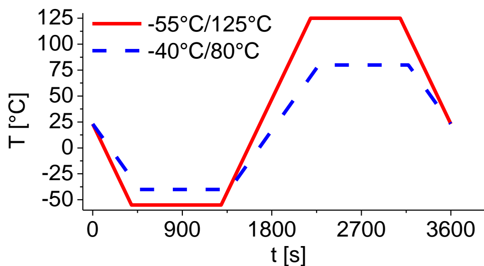


Fig. 9: Simplified thermal cycle during TC testing.

To check the samples for delamination, scanning acoustic microscopy (SAM, figure 10) and metallographic sectioning (figure 11) was carried out. Altogether 20 specimens of the good set went under thermal cycling. Exemplarily figure 10 shows the propagation of the delamination at initial state, after 1000 and 2000 temperature cycles (TC) in the range of -55°C and 125°C. SAM is only a good method to determine delamination and crack length if the crack is far enough from the chip edge. In this case there is very slow crack propagation so that metallographic sections of the specimens need to be carried out. The disadvantage while doing this is destroying one specimen per crack length determination. The planed testing will on-going for at least another 2000 TC.

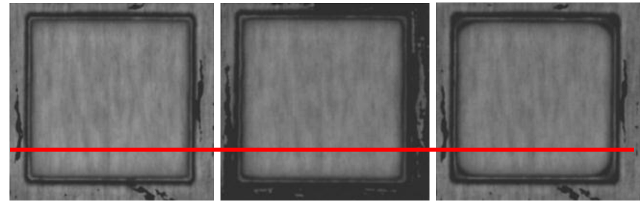

Fig. 10: SAM scans of sinter Ag die attach at initial state (left), after 1000 TC (center) and after 2000 TC (right). The red line represents roughly the position of cross sectioning.

The propagation of die attach damage is depicted in figure 11. On the REM record of the cross section on top we can see the state of the die attach after 1000 TC. The crack length in this region is about 90µm from the edge of the chip. The microscopic picture below shows the crack length after 2000 TC. The crack length here is about 168µm. Specimens coming from the same set cycled in the range of -40°C to 80°C don't show any damage after 2000 TC.

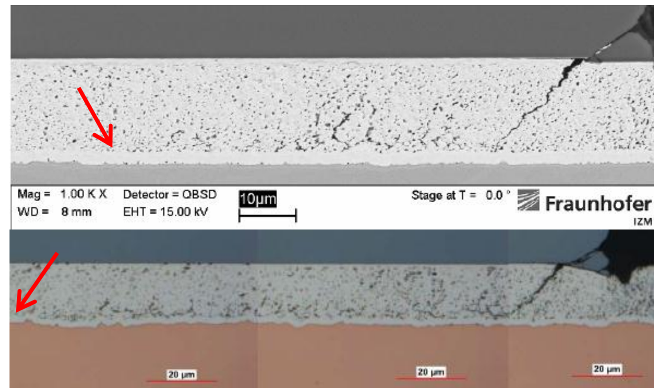


Fig. 11: Crack propagation in die attach after 1000 TC (top) and after 2000 TC (bottom) @ -55°C/125°C. The red arrow pinpoints the tip of the crack.

Now we have a first idea how damage progress under the investigated conditions develops. In the next step the damage process will be physically modeled by transferring the experiments to an FE-Model. Therefore a full parametric model of the COB was build (figure 12).

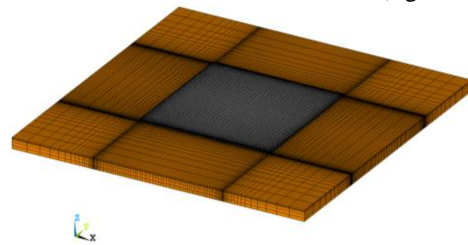

Fig. 12: Expanded 1/4 FE-Model of the 9×9mm² IGBT on a 20×20mm² copper substrate

Material data shown in table 2 were implemented and the original test matrix described in chapter 2 was performed.

| Material | E [GPa] | $\sigma_0$ / T [MPa] | ν | CTE [ppm] | $\alpha$ / $n$ |
|---|---|---|---|---|---|
| SinterAg (Fit) | 64.0 | 181.0 | 0.3 | 19.0 | 0.75 / 4.16 |
| Silicon | 168 | - | 0.28 | 2.6 | - |
| Copper | 110 | 180 / 6500 | 0.34 | 16.5 | - |

Table 2: Material data used in simulations

The question is where in the model and how to evaluate the plastic strain. One possible approach could be to do the damage evaluation in the same way as is usually done for solder balls from, e.g. flip-chip assemblies [8]. This procedure averages the creep strain rate over the region where damage occurs to avoid singularities and numerical effects on interfaces [9, 10]. The idea now is to do the same averaging of the plastic strain rate for the sintered silver as it was performed before for different solder die attach [11].

As for solder material the accumulating creep strain can describe the failure behaviour for sintered silver it is the accumulated plastic strain. As can be seen from the FE-simulation in figure 13, there is an area of high plastic strain rate running along the perimeter of the silver layer, indicating the region of beginning damage.

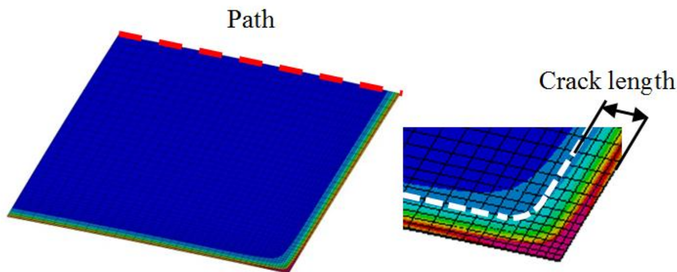


Fig. 13: Failure criterion is the accumulated equivalent plastic strain rate per temperature cycle. The data path for analysis is the red line.

For the evaluation the plastic strain rate is mapped on to the path reaching from the edge to the center of the die attach. It is located in the die attach 4µm above the copper substrate. Equation 5 is used to do the averaging of the path data [11].

$$\varepsilon_{pl}^{avg} = \frac{1}{a}\int_0^a \varepsilon_{pl}(s)ds \qquad (5)$$

Because of the mechanical effect of massive delamination on the chip assembly this approach can only be valid for cracks much shorter than the chip size. Assuming a value of 10% area delamination as failure criterion should be provide cracks short enough to fulfill these demand [11]. The assumed critical crack length corresponding to 10% area delamination is app. 230µm for the 9×9mm² chip sizes and app. 150µm for the 6×6mm² chip sizes. This lies within the result we get from the experiments. Here for the 9×9mm² chip size and a die attach thickness of 22µm the crack length is about 168µm after 2000 temperature cycles.

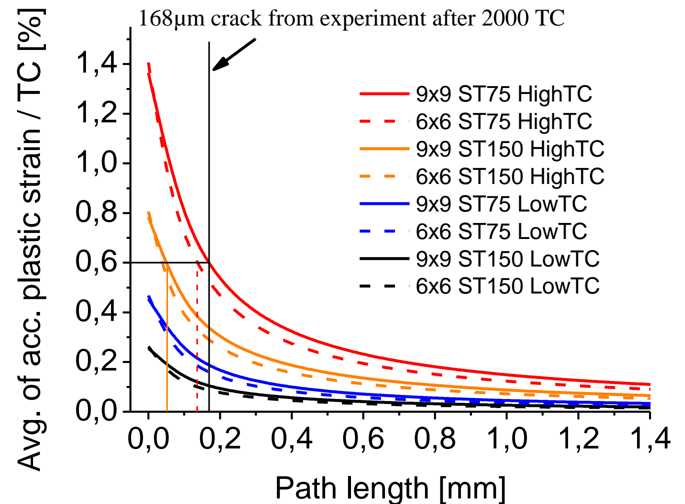


Fig. 14: Averaged accumulated plastic strains per TC plotted over the path length. The failure criterion is the crack length of 168µm from experiment.

Comparing the results from simulation depicted in figure 14 as expected the amount of the plastic strain rate strongly depends on the temperature profile. Specimens loaded with the high TC (-55°C to 125°C) show much more damage potential than the ones loaded with the low TC (-40°C to 80°C). Furthermore plastic strain rate drops with rising stencil thickness. The influence of the chip size seems to be relatively small.

Referring to the experimental result where the crack length reaches 168µm after 2000 TC the average of the plastic strain rate for these length amounts according to the simulation is approx. 0.6%. On the assumption that specimen with similar geometric properties show similar mechanical stress behavior we can compare these results to other simulations. Doing so the crack length after 2000 high TC, e.g. in the die attach of the specimen with 6×6mm² chip size and 75µm stencil thickness (doted red graph) lies about 136µm and for the one with a 9×9mm² chip size and 150µm stencil thickness (orange graph) only at 50µm.

In the experiment we nor observed any damage in the die attach of the specimen with 9x9mm² chip size and a stencil thickness of 75µm at low TC loading. In the simulation (blue graph) the value of 0.6% plastic strain per TC never is reached for any crack length so crack growing can assumed to be much slower than in the high TC loading.

# 5 CONCLUSIONS & OUTLOOK

In this paper a general approach to performing reliability analyses of sinter silver die attach was presented. The whole process from fabrication, material characterisation up to the numerical assisted evaluation of reliability aspects were described. It was found that in general the damage behavior correlates with the numerical approch done by FE-modeling which allows it to compare the effects of geometric and material design parameter on the die attach reliabilty.

Due to the problems with the current test vehicles a new set of test specimens were fabricated and prepared to undergo the cycling procedure again. From these future experimental results we should be able to extract a more sophisticated liftime model.

## ACKNOWLEDGMENTS

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