# HiSIM-DG for Extracting Statistical Variations of Measured I-V Characteristics

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## ABSTRACT

We have developed the double gate (DG)-MOSFET model HiSIM-DG based on the complete surface-potential-based description valid both for the symmetrical and the asymmetrical independent gate structures. HiSIM-DG is verified to reproduce measurement results for any geometries as well as for statistical variabilities. It is found that the reason for the observed channel-length dependence of the different device-performance variations can be explaned by considering the silicon-layer-thickness variations.

***Keywords***: dg-mosfet, symmetry, asymmetry, variations

## 1 INTRODUCTION

Advanced bulk-MOSFETs are facing serious problems such as increased off-current and no saturation behavor of on-current due to enhanced short-channel effects. The Double-Gate MOSFETs are considered to be a promising candidate as the next generation MOSFET structure [1]. A big advantage of such structure with a very thin substrate silicon layer thickness is a suppression of the short-channel effects even down to 10nm channel length [2, 3]. To exploit the advantage for circuit applications, accurate compact models applicable for any device structures is inevitable.

Many different models based on different concepts have been developed [4, 5]. We have developed the complete surface-potential-baced model HiSIM-DG solving the full Poisson equation iteratively.

It is expected that variation of device characteristics might cause serious problems on circuit operations for the generation era of DG-MOSFETs with ultra down scaled device dimensions. Our purpose here is to evaluate the device variations with use of HiSIM-DG. We demonstrate that HiSIM-DG enables measured device characteristics based on device variations originated by process variations. This enables to provide a guideline for the circuit design with the advanced DG-MOSFET technology.

## 2 MEASURED VARIATIONS

Figs. 1 shows the studied DG-MOSFET structure and its device parameters. The values are $T_{ox}$= 2.3 nm, $T_{si}$= 40 nm, $N_{sub}$= $10^{15}$ cm$^{-3}$ and $W_g$= 60 nm for various gate lengths $L_g$. Measured $I_{ds}$-$V_{gs}$ characteristics for various $L_g$ lengths are shown in Fig. 2. Each figure includes measurements of 15 different chips. It can be seen that variations of the *I-V* characteristics are non-negligble even for the long channel device. Fig. 3 summarizes the on-current $I_{on}$ and the threshould-voltage $V_{th}$ variations of the measured characteristics.

Here we observe interesting features of the DG-MOSFET variations. The amount of the variation of $\Delta V_{th}$ is nearly independent of $L_g$ (see Fig. 3a). Whereas that of $I_{on}$ is as expected (see Fig. 3b), namely the variation increases as $L_g$ reduces. Fig. 3c shows the correlation between $\Delta I_{on}$ and $\Delta V_{th}$.

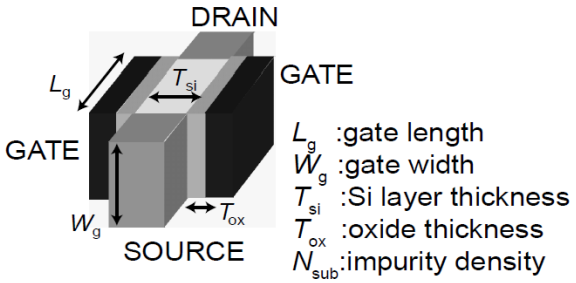


Fig. 1. Schematic illustration of a DG-MOSFET and device parameter.

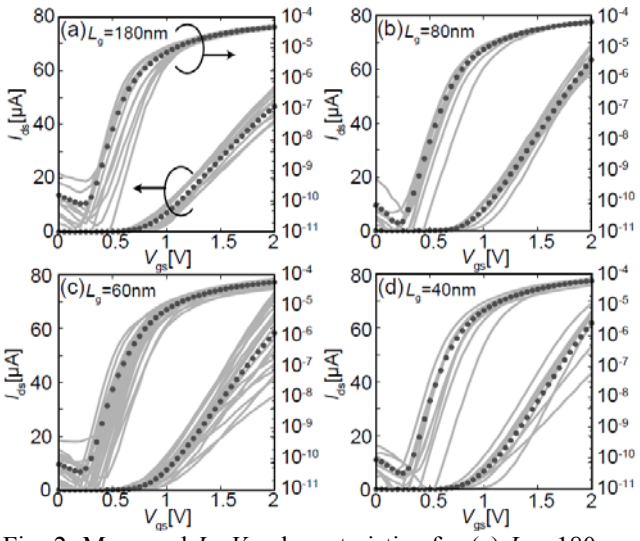


Fig. 2. Measured $I_{ds}$-$V_{gs}$ characteristics for (a) $L_g$= 180 nm, (b) $L_g$= 80 nm, (c) $L_g$= 60 nm and (d) $L_g$= 40 nm. Averaged characteristics are shown with thick dotted lines.

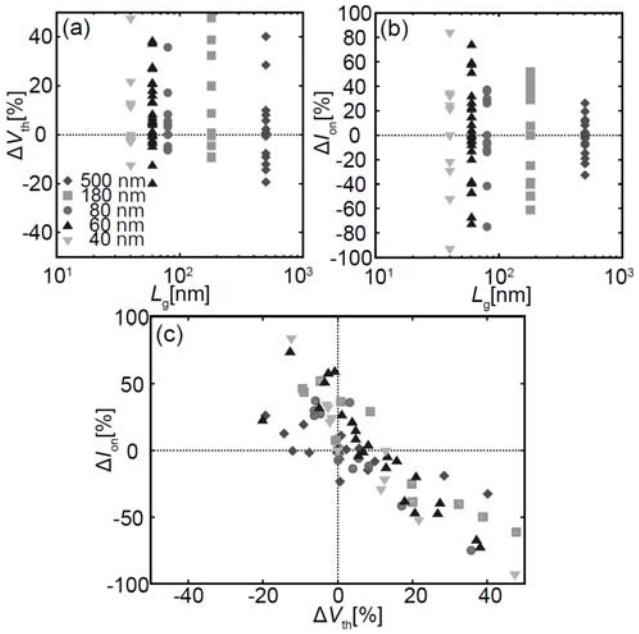


Fig. 3. Measured (a) threshold-voltage deviation $\Delta V_{th}$. vs. gate length $L_g$, (b) on-current deviation $\Delta I_{on}$ vs. $L_g$ and (c) $\Delta I_{on}$ vs. $\Delta V_{th}$.

## 3 CONCEPT OF HiSIM-DG

Fig. 4 shows induced charges and a potential distribution along the depth direction under an applied bias condition. HiSIM-DG solves the Poisson equation includeing all induced charges iteratively [6-8]. HiSIM-DG is applicable for any type of device structures, because it considers the charges $Q_{g1}$ and $Q_{g2}$ independently in the Poisson equation. These charges are combined with the Gauss Law, considering the both electric fields induced by the independent gate voltage explicitly, one from $V_{gs1}$ and one from $V_{gs2}$. The final Poisson equation to be solved together with the Gauss low is written [9]

$$\begin{cases} (V_{gs1}-V_{fb})-\phi_{s1}=-\dfrac{Q_I+Q_{dep}+Q_{g2}}{C_{ox1}},\ Q_I=f(\phi_{s1},Q_{g2}) \\ \phi_{s1}-\phi_{s2}=-\dfrac{\frac{1}{2}Q_{dep}+Q_{g2}}{\varepsilon_{si}}T_{si} \\ \phi_{s2}-(V_{gs2}-V_{fb})=-\dfrac{Q_{g2}}{C_{ox2}} \end{cases} \quad (1)$$

where $\phi_{s1}$ and $\phi_{s2}$ are surface potentials at $V_{gs1}$ and $V_{gs2}$, respectively. The oxide capacitances are denoted by $C_{ox1}$ and $C_{ox2}$ for the 1st gate and the 2nd gate, respectively. Since the Poisson equation is an implicit function, an iterative approach is applied to solve Eq. (1) under any bias conditions.

Since the device parameters such as the gate oxide thickness are considered independently for two independent gates, switching between the symmetrical structure and the asymmetrical structure is done automatically in a smooth way. After solving Eq. (1), HiSIM-DG knows the potential distribution along the silicon-layer-thickness direction. Under the gradual channel approximation, the potential distributions at the source side and the drain side are solved independently. All device characteristics can be calculated with the potential values. The accuracy of the calculated potential values are verified by comparing calculated capacitances and *I-V* characteristics with 2D-device simulation results. The comparisons are given in Figs. 5-8 for various structures. Good agreements have been proven for wide ranges of operation conditions.

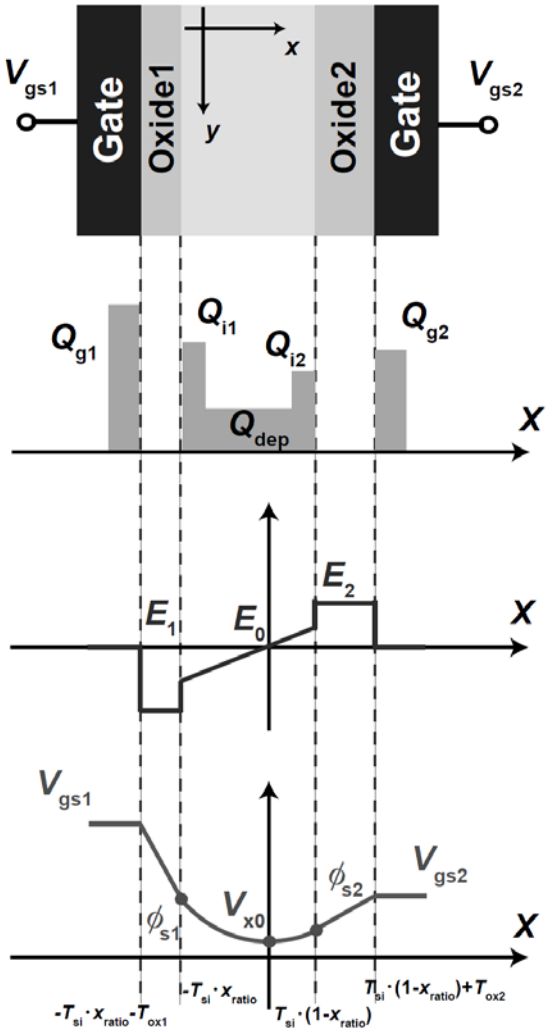


Fig. 4. Cross-section of the studied double-gate MOSFET structure and modeling concept is summarized where three potential values considered ($\phi_{s1}$, $\phi_{s2}$, $V_{x0}$) are depicted together. All charges ($Q$) induced in the device, the field ($E$) distribution, as well as the potential ($\phi$) distribution along the $x$ direction are depicted together. The position $V_{x0}$ denotes the point where the field becomes zero. $x$ ratio, determing the $V_{x0}$ point is caluculated by the ratio of the oxide field between the 1st gate and the 2nd gate.

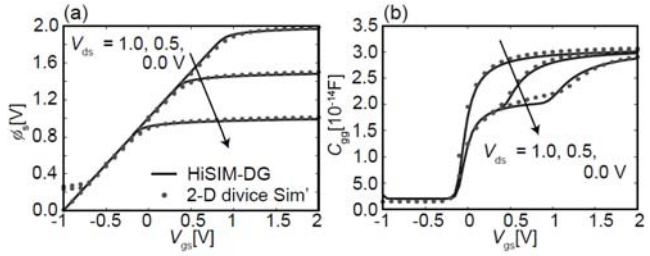


Fig. 5. Comparison of calculated (a) surface potential $\phi_s$ and (b) gate capacitance $C_{gg}$ with HiSIM-DG to those 2D-device simulation results for a symmetrical structure with the common gate.

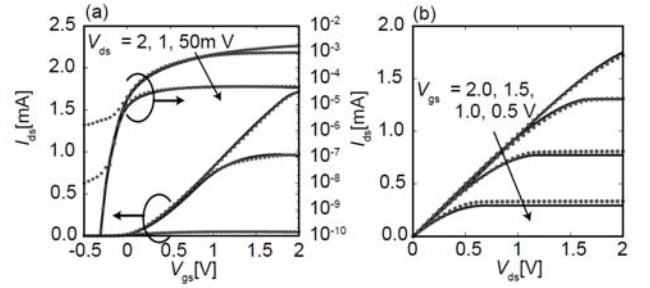


Fig. 6. Comparison of calculated (a) $I_{ds}$-$V_{gs}$ characteristics and (b) $I_{ds}$-$V_{ds}$ characteristics with HiSIM-DG (lines) to 2D-device simulation results (symbols) for the symmetrical device shown Fig. 5.

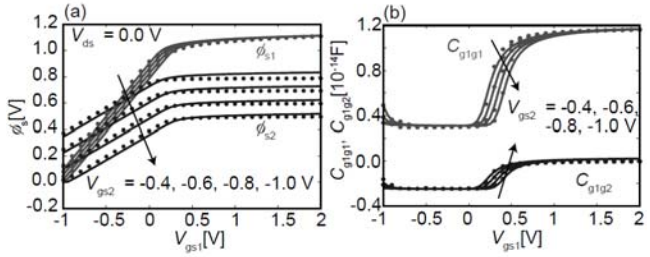


Fig. 7. Comparison calculated (a) surface potential and (b) capacitance values with HiSIM-DG to those of 2D-device simulation results for an asymmetrical structure with the independent gate.

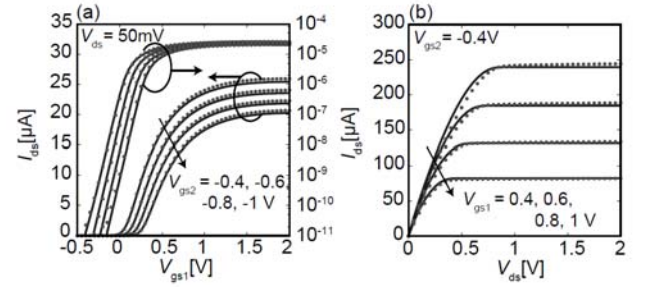


Fig. 8. Comparison of caluculated (a) $I_{ds}$-$V_{gs}$ characteristics and (b) $I_{ds}$-$V_{ds}$ characteristics with HiSIM-DG (lines) to 2D-device simulation results (symbols) for the asymmetrical device in Fig. 7.

# 4 EVALUATION OF VARIATIONS

The parameter extraction is performed with HiSIM-DG for standard *I-V* measurements[10]. As the measurements the averaged characteristics of 15 chips shown by thick dotted lines in Figs. 2a and d are utilized. Figs. 9a and b show fitting results for $L_g$ = 180 nm and 40 nm, respectively. It has to be noticed that a single model parameter set is valid for any transitor sizes.

Fig. 10 shows calculated sensitivity analyses of several important device parameters determing the threshold-voltage $V_{th}$ and the on-current $I_{on}$. These parameters are usually used to characterize transitor features [11]. It can be seen that the model parameters (*TOX*: gate-oxide thickness, *TSI*: silicon-layer thickness, *XLD*: channel-length modification), which are directly related to the corresponding DG-MOSFET structural parameters, show the highest sensitivity on $I_{on}$, as is expected. It is noticable, however, that these parameters gives negligible influence on $V_{th}$, which is different from bulk-MOSFETs.

To reproduce the $\Delta V_{th}$ variation observed in Fig. 3, the impurity concentration (*NSUBC*) of the silicon layer is varied. Fig. 11 shows caluculated $\Delta V_{th}$ and $\Delta I_{on}$ as a function of *NSUBC*. It can be seen that *NSUBC* variation results in observed $V_{th}$ and $I_{on}$ correlation. Caluculated variations with these extracted parameter variations are dipicted in Fig. 12 for two $L_g$ lengths. Measured correlations between $\Delta V_{th}$ and $\Delta I_{on}$ for different gate lengths are well reproduced.

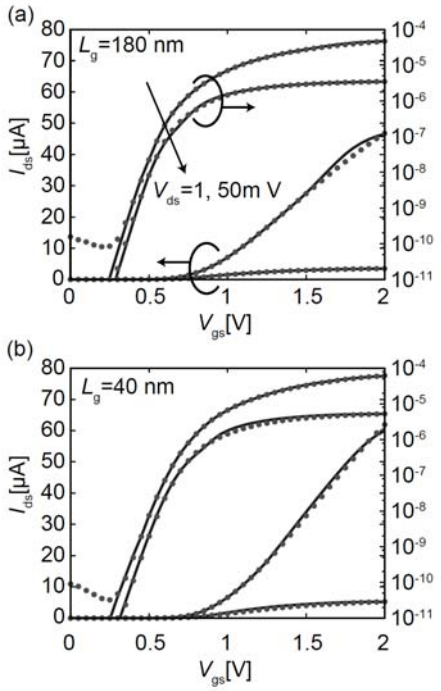


Fig. 9. Comparison of calculated $I_{ds}$-$V_{gs}$ characteristics with HiSIM-DG (lines) to measurements (symbols) for (a) $L_g$= 180nm and (b) $L_g$= 40nm. As the measurments the averaged characteristics depicted by thick dotted lines in Fig. 2 are applied.

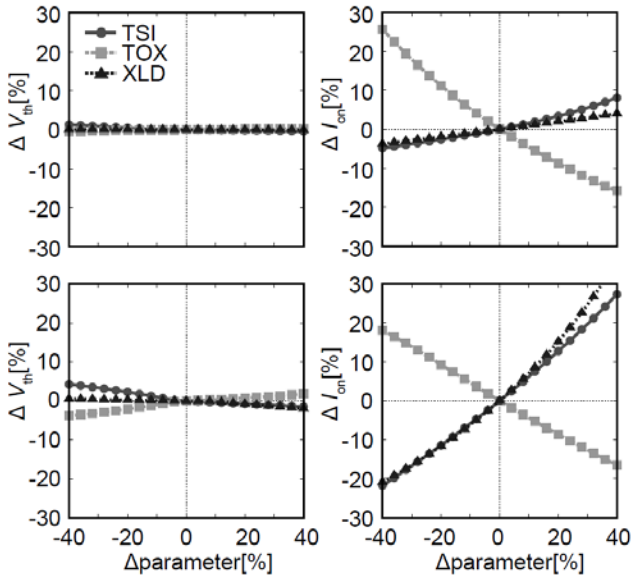


Fig. 10. Sensitivity analysis of the model parameters for $\Delta V_{th}$ (left) and $\Delta I_{on}$ (right) for $L_g$=180nm (upper) and 40nm (lower) case.

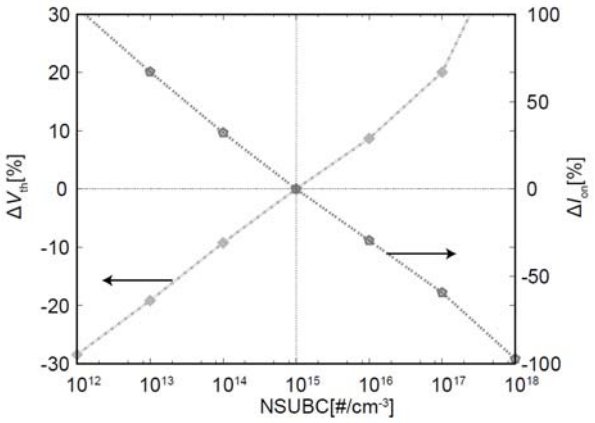


Fig. 11. Sensitivity analysis of the various *NSUBC* for $\Delta V_{th}$ and $\Delta I_{on}$ with HiSIM-DG.

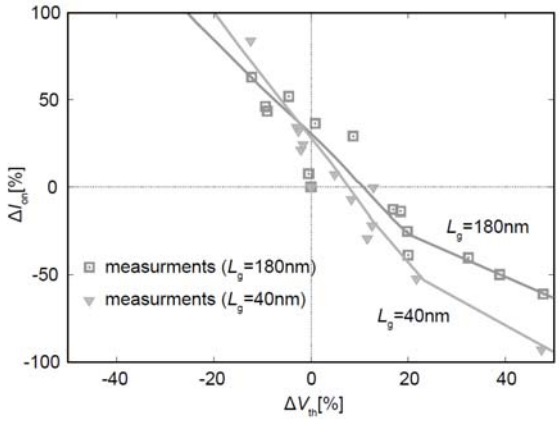


Fig. 12. Measurd $I_{on}$-$V_{th}$ variations of DG-MOSFET in Fig 3 (c). Comparison of $I_{on}$-$V_{th}$ characteristics with HiSIM-DG results to measured results.

# 5 CONCLUSION

We have developed the independent DG-MOSFET model HiSIM-DG based on the complete surface-potential-based description applicable both for symmetrical and asymmetrical structures. It has been demonstrated that the model is applicable for any geometries and any bias conditions.

Variations of $I_{on}$ and $V_{th}$ for DG-MOSFET are analyzed with HiSIM-DG. It was found that the Silicon layer thickness variation and the channel length variation dominate the device-performance variation. Moreover, the transistor characteristics for the smaller gate length are predominate as *XLD* and *TSI*.

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