Modeling Bias Stress Effect on Threshold Voltage for Amorphous Silicon Thin-Film Transistors and Circuits

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ABSTRACT

In this paper, we study amorphous silicon thin-film-transistor (TFT) degradation under bias stress effect. To model threshold voltage shift with bias stress effect, fabricated samples are measured for I-V data with bias stress in variations of temperature. Rensselaer Polytechnic Institute (RPI) model is thus adopted to extract model parameters, such as the flat band voltage (V_{FB}), the characteristic voltage for deep states (V_O), the conduction band mobility (MUBAND), the channel length modulation parameter (LAMBDA), the power law mobility parameter (GAMMA) and the saturation modulation parameter (ALPHASAT) from the measurement. The model card with those extracted parameters is validated via a TFT circuit simulation. The results of the circuit simulation indicate the relationship of effects depending on the stress and operational temperature.

KEYWORDS: Amorphous silicon TFT, threshold voltage, bias stress effect, temperature effect, Rensselaer Polytechnic Institute (RPI) model, circuit simulation.

1 INTRODUCTION

Amorphous silicon thin-film transistors (a-Si:H TFTs) have been widely used in active-matrix backplanes for LCD displays on glass [1-2]. Unfortunately, DC and dynamic characteristics of a-Si:H TFTs are sensitive [3]; in particular, they suffer form electric-field-induced threshold voltage shift [4-6]. Figure 1(a) shows the DC characteristics of fabricated samples with and without (w/o) stress, where gate length/width = 4 μm/26.5 μm, gate bias of stress (V_{gs}) = 28 V, drain bias (V_{ds}) = 0 V and temperature (T) = 65°C. We find that the drain current significantly decreases after a prolonged gate bias stress. From transfer characteristics in log scale viewpoint, the subthreshold swing becomes larger after stressing, as shown in Fig. 1(b). The DC characteristic was widely studied and modeled recently [7-8]; however, the dependence of DC characteristic on bias stress time has not been clear yet.

In this study, we use the proposed parameter extraction technique sequentially to optimize the significant model parameters in the regions of linear, subthreshold and saturation [9]. It consists of the following several steps to complete the model parameter extraction. Before extracting parameters, we replace the default value of threshold voltage calculated from the measured data as the basic foundation. MUBAND and GAMMA are firstly optimized for the linear region of I-V curves. We then extract the threshold regions by choosing the parameters of zero bias threshold voltage (V_{TO}), V_{FB} and V_O. ALPHASAT and LAMBDA are thirdly optimized for the saturation region. After the complicated steps, we put RPI the model card into A 14 a-Si:H TFTs integrated gate (ASG) driver circuit for circuit simulation. The results of power loss of the tested ASG circuit show the degradation with the bias stress effect.

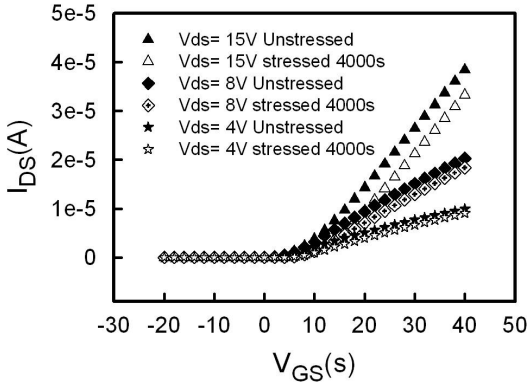

Fig. 1. The I_{DS}-V_{GS} characteristics without stress as V_{GS} varying from -20 - 40 V, where V_{ds} = 4, 8 and 15 V, respectively.

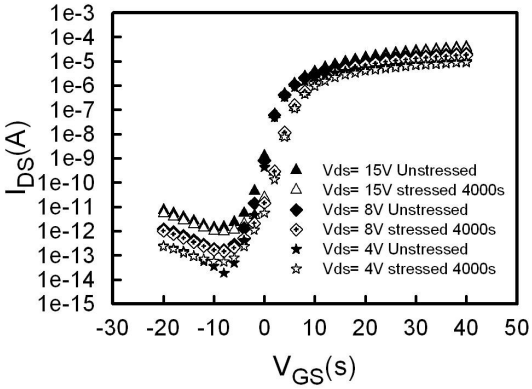

Fig. 2. The I_{DS}-V_{GS} characteristics in log scale without stress as V_{GS} varying from -20 - 40 V, where V_{ds}= 4, 8 and 15 V, respectively.

2 THE BIAS STRESS OF THRESHOLD VOLTAGE

First, we use constant current process to define the threshold voltage. The definition of threshold voltage is the drain current is equal to 1 nA as the drain voltage is 0.5 V. As shown in Fig. 3, the threshold voltage increases rapidly

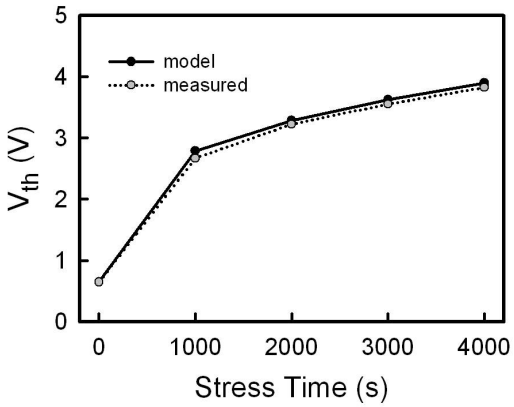

Fig. 3. Measured data and model result of threshold voltage (V_{th}), where the model result is estimated from Eq. (1).

at the beginning of stressing and saturates after 4000 sec as T = 65°C which is one of 4 sets of measurement data (25, 45, 65, and 85°C). The threshold voltage varied with stress time can be modeled by using a power law:

$$V_{th}(t) = V_{th}(0) + A_t \cdot t^{\beta_t} \quad (1)$$

$$\Delta V_{th}(t) = A_{ts} \cdot t^{\beta_{ts}} \cdot \exp\left(-\frac{E_{ta}}{kT}\right) \quad (2)$$

where t is the bias stress time duration, A and β are stress-dependent parameters. After calibration with the threshold voltage variations from the measurement data, the estimated A_t and β_t are 0.27 and 0.3, respectively. According to [10] a semi-empirical description of threshold voltage shift is approximated as shown in Eq. (2).

Figure 4 shows the V_{th} shift with increasing stress time. In this sample, k is the Boltzmann constant, E_{ta} is the mean activation energy, A and β_{ts} are constant to be determined. We use nonlinear regressing analysis with iteration process to get A_{ts} = 23016, β_{ts} = 0.4592, and E_{ta} = 0.3771eV, respectively. Based on the Eq. (1) and a-Si:H RPI TFT model, we further develop a modeling technique for the stressed TFT samples. First of all, model parameters for I-V characteristics without stress are extracted by RPI a-Si:H TFTs model parameter extraction procedure, where the threshold voltage (V_{TO}) is set as the default value form RPI a-Si:H TFTs model before extraction. After calibrating with measurement data with stress, we obtain a new value of threshold voltage V_{th} from Eq. (1) and replace the default value of VTO in RPI a-Si:H TFTs model. Then the I-V characteristics of TFTs with the stress time can be predicted by the extracted model parameters.

3 THE BIAS STRESSED PARAMETERS

Before circuit simulation, the relationship between the model parameters and bias stress effect is tested. According to the extracted method, we can obtain the revised model

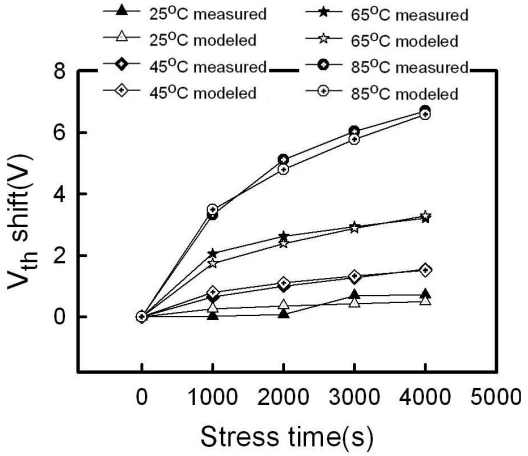

Fig. 4. The measured data and modeled result of V_{th} shift under T = 25, 45, 65 and 85°C, where the model result follows Eq. (2).

card of RPI model. In the linear region, we optimized mobility related parameters MUBAND and GAMMA by using RPI a-Si:H TFTs model parameter extraction procedure. Figures 5 and 6 show the extracted values of MUBAND and GAMMA. The results point out the degradation of MUBAND and GAMMA under the increasing stress time. In the threshold region, first, we use the calculated values of V_{th} to replace V_{TO}, and then consider the Id-Vd curves having translation, we can extract V_{FB} (V_{FB} is default parameter of flat-band voltage) by using RPI extraction procedure under increasing stress time. The extracted results of flat-band voltage and flat-band voltage shift are revealed in Fig. 7. Moreover, we compare slopes of I_d-V_d curves in the threshold region at RPI extraction procedure with measured data and extract those results to obtain V_O. The value of V_O is shown in Fig. 8. In the saturation region, ALPHASAT controls the saturation voltage and LAMBDA represents the channel length modulation. We adjust ALPHASAT and LAMBDA to optimize I_d-V_{ds} curves. The variation under the increasing stress time is shown in Figs. 9 and 10. In summary, we integrate the parameter values and use the RPI extraction procedure to obtain a set of complete model card. Table 1 shows the errors of measured data compared with extracted data in the linear, threshold and saturation regions, respectively, as bias stress time is varying from 0 to 4000 sec. and temperature equals 25°C and 85°C, rsepctively.

4 APPLICATION TO CIRCUIT SIMULATION

We apply the proposed equation with the RPI model cards for ASG driver circuit simulation under bias stress and different temperatures. In this work, the ASG driver circuit of 14 a-Si:H TFTs, as shown in Fig. 11, is the most critical component in GOP (gate-on-panel) design in display industry [11-12]. Which sends the pulse to drive the pixels on panel, but the quality of it may be seriously affected by the biase stress time and the temperature of environment.

The reason is mainly from the threshold voltage shift. The power comsumption of the ASG driver circuit is given by

$$P = f \cdot c \cdot v^2 \qquad (3)$$

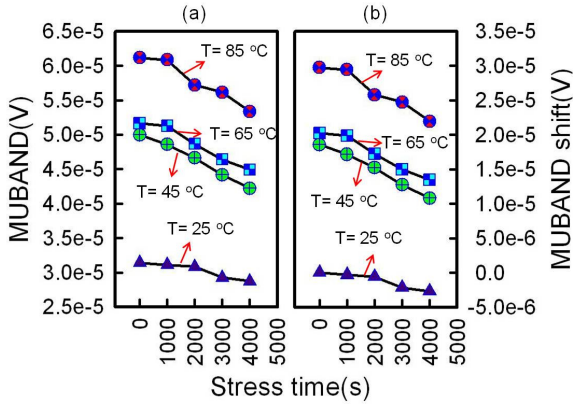

Fig. 5. (a) and (b) Extracted value of MUBAND and MUBAND shift decrease with increasing stress time under temperature (T) = 25°C,45 °C, 65°C, and 85°C.

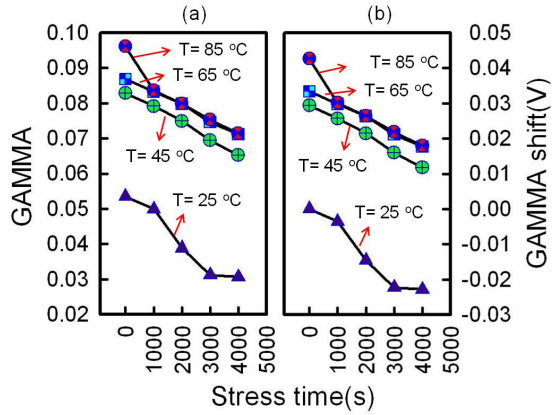

Fig. 6. (a) and (b) Extracted value of GAMMA and GAMMA shift decrease with increasing stress time under temperature (T) = 25°C,45°C, 65°C, and 85°C.

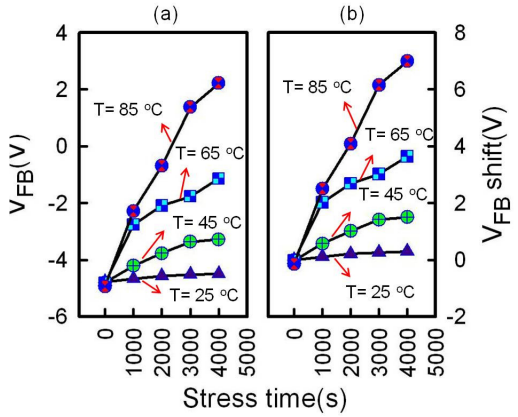

Fig. 7. (a) and (b) Extracted value of V_{FB} and VFB shift decrease with increasing stress time under temperature (T) = 25°C, 45°C, 65°C, and 85°C.

In Eq. (3), *f* is the frequency of the driving clock signal, *c* is the capacitance from clock input node, and *v* is the deviation of high and low voltage level applied on the circuit. Table 2 lists the comparison of power comsumption of various bias

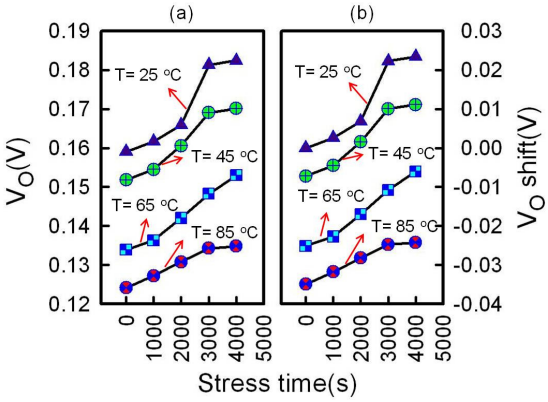

Fig. 8. (a) and (b) Extracted value of V_O and V_O shift decrease with increasing stress time under temperature (T) = 25°C, 45°C, 65°C, and 85°C.

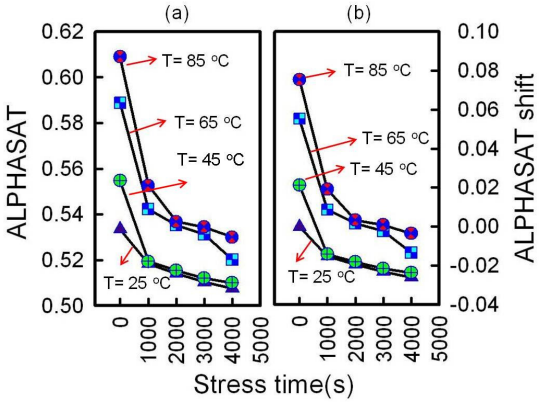

Fig. 9. (a) and (b) Extracted value of ALPHASAT and ALPHASAT shift decrease with increasing stress time under temperature (T) = 25°C, 45 °C, 65°C, and 85°C.

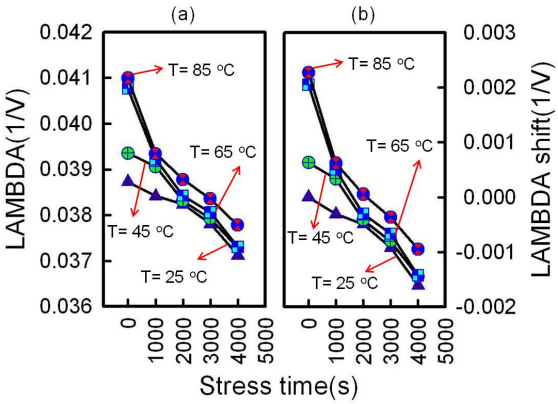

Fig. 10. (a) and (b) Extracted value of LAMBDA and LAMBDA shift decrease with increasing stress time under temperature (T) = 25°C, 45 °C, 65°C, and 85°C.

stress times and temperatures. The negative correlations between stress time and power at each temperature are vious, but if the stress time is fixed, there are no general trend of power among different tempeartures. The reason is that the effects of stress are stronger under high temperature environment.

Tab. 1. The error for measured result compara to extract data with bias stress time under T = 25 and 85°C.

Error table for measured result compare to extracted data			
Region / Stress Time(s)	Leaner (%)	threshold (%)	saturation (%)
0 T = 25°C	0.38	2.13	0.98
1000 T = 25°C	0.74	2.56	0.79
2000 T = 26°C	0.62	2.43	0.92
3000 T = 25°C	0.63	2.66	0.56
4000 T = 25°C	0.71	2.78	0.86
0 T = 85°C	0.68	2.77	0.88
1000 T = 85°C	0.69	2.86	0.86
2000 T = 85°C	0.86	2.23	0.79
3000 T = 85°C	0.52	2.49	0.96
4000 T = 85°C	0.77	2.68	0.91

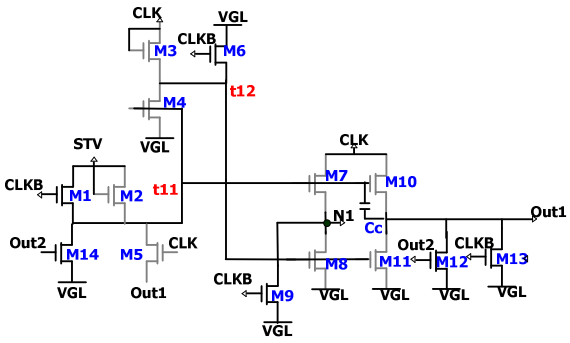

Fig. 11. The tested TFT-LCD driver circuit (denoted as ASG driver circuit) in this work. The a-Si:H TFTs' circuit has fourteen transistors and four capacitance. The bias stress effect of a-Si:H TFTs on ASG circuit is modeled and simulated based upon the calibrated model.

Tab. 2. The simulated circuit dynamic characteristics for power consumption in 14 different temperatures and under the bias stress time 1000, 2000, 3000, and 4000 sec. of the ASG driver circuit.

Compared characteristic of power consumption for circuit simulation				
T (°C)	Stress time 1000 (s)	Stress time 2000 (s)	Stress time 3000 (s)	Stress time 4000 (s)
25	197.65 μW	196.49 μW	194.31 μW	194.09 μW
45	199.81 μW	199.21 μW	197.12 μW	195.69 μW
65	200.15 μW	192.82 μW	189.92 μW	188.61 μW
85	202.14 μW	195.67 μW	183.99 μW	178.78 μW

5 CONCLUSIONS

In this work, we have presented the parameter extraction procedure for modeling bias stress effect on threshold voltage variation of a-Si:H TFTs, based up on RPI model, in TFT-LCD circuit simulation. By considering stress bias, stress time, and operation temperature, the bias stress effect on the threshold voltage has been modeled and calibrated with measured samples. This model can be incorporated into TFT-LCD circuit simulation for reliability issues.

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REFERENCES

[1] M. S. Shur, H. C. Slade, M. D. Jacunski, A. A. Owusu, and T. Ytterdal, "SPICE Models for Amorphous Silicon and Polysilicon Thin Film Transistors," *Journal of The Electrochemical Society,* vol. 144, no. 8, pp. 2833-2839, 1997.

[2] S.-C. Kao, H.-W. Zan, J.-J. Huang, and B.-C. Kung, "Self-Heating Effect on Bias-Stressed Reliability for Low-Temperature a-Si:H TFT on Flexible Substrate," *IEEE Trans. Electron Devices*, vol. 57, no. 3, pp. 588-593, Mar. 2010.

[3] Y. Li, C.-H. Hwang, C.-L. Chen, S. Yan, J.-C. Lou, " UV Illumination Technique for Leakage Current Reduction in a-Si:H Thin-Film Transistors," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3314, November.2008.

[4] Y. Kaneko, A. Sasano, and T. Tsukada, "Characterization of instability in amorphous silicion thin-film transistors," *Journal of Applied Physics*, vol.69, no. 10, pp, 7301-7305, May 1991.

[5] F. R. Libsch and J. Kanicki, "Bias-stress-induced stretched-exponential time depen-dence of charge injection and trapping in amorphous thin-film transistors," *Applied Physics Letters*, vol. 62, no. 11, pp. 1286-1288, Mar. 1993.

[6] H. C. Slade and M. S. Shur, "Analysis of bias stress on unpassivated hydrogenated amorphous silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 45, no. 7, pp. 1548-1553, Jul. 1998.

[7] M. Powell, "The physics of amorphous-silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 36, no. 12, pp. 2753-2763, Dec. 1989.

[8] S.-E. Liu, C.-P. Kung and J. Hou,"Estimate Threshold Voltage Shift in a-Si:H TFTs Under Increasing Bias Stress," *IEEE Trans. Electron Devices*, vol. 56, no. 1, pp. 56-59, Dec, 2009.

[9] A. Cerderia, M. Estrada, R. Garcia, A. Ortiz-Conde and F. J. Garcia, "New procedurefor the extraction of basic a-Si:H TFT model parameters in the linear and saturation regions," *Solid-State Electronics*, vol. 45, pp. 1077-1080, 2001.

[10] D. R. Allee, L. T. Clark, B. D. Vogt, R. Shringarpure, S. M. Venugopal, S. G. Uppili, K. Kaftanoglu, H. Shivalingaiah, Z. P. Li, J. J. Ravindra Fernando, E. J. Ba-wolek, and S. M. O'Rourke, "Circuit-Level Impact of a-Si:H Thin-Film-Transistors Degradation Effects," *IEEE Trans. Electron Devices*, vol. 56, no. 6, pp. 1166-1176, Jun. 2009.

[11] K. F. Lee, Y. Li, I. H. Lo, Tony. Chiang, K. Y. Huang, and T. H. Hsieh, "Gate Driver Circuit Design Optimization for TFT-LCD Panel Manufacturing," in: *2nd Asia Symposium on Quality Electronic Design*, pp. 13-16, 2010.

[12] I. H. Lo, Y. Li, and K. F. Li, "Highly Optimized Electrical Characteristics of a-Si TFT Gate Driver for Display Panel Manufacturing," in: *Proc. Inter. Meeting Infor. Disp.*, pp. 114-117, 2010.