Inverter Circuits Based on Low-Temperature Solution-Processed ZnO Nanoparticle Thin-Film Transistors

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ABSTRACT

An enhancement-load inverter circuit is presented, which is based on ZnO nanoparticles as active material. Poly(4-vinylphenol) is used as a polymeric gate dielectric layer, so it was possible to perform the integration process with a maximum temperature of 200℃. Aluminum and gold gate electrodes were investigated for individual transistors. In both cases the transistors exhibited a field-effect mobility of $2 \cdot 10^{-3}\,\mathrm{cm^2/(Vs)}$ and the transfer characteristics were dominated by hysteresis, which is presumably related to charge trapping in the gate dielectric layer. The thin-film transistors with aluminum gate electrodes showed a significantly better performance in the transistor off-state. Therefore, the Al-gated transistors were utilized for the inverter devices. The maximum peak gain and static power dissipation were 6 V/V and 600 nW, respectively. These values are reasonable for nanoparticle based devices.

Keywords: inverter circuits; zinc oxide; nanoparticle; field-effect transistor

1 INTRODUCTION

During the last years, inorganic semiconductors have received much attention for low-cost electronic applications [1, 2]. In particular, zinc oxide (ZnO) is a promising candidate for flexible, transparent and printable thin-film transistors (TFT). Future printability is a main issue and for printable electronics, ZnO is usually deposited as a nanostructured material like nanorods, nanowires and nanoparticles [2, 3] or by sol-gel method [4]. TFTs which were integrated by inkjet-printing technique have already been demonstrated [5]. However, solution-processing via the sol-gel route is in need of relatively high temperatures for the precursor decomposition [6,7]. Reports of ZnO inverter circuits are limited to devices integrated by plasma-enhanced atomic layer deposition or plasma-enhanced chemical vapor deposition [8,9]. Using nanoparticles as semiconductor material, the integration of individual TFTs often demands a post-treatment of the active layer (high-temperature annealing or laser sintering) in order to improve the conductivity of the semiconductor film [10–12]. Inverter circuits based on enhancement-type bottom-gated TFT,

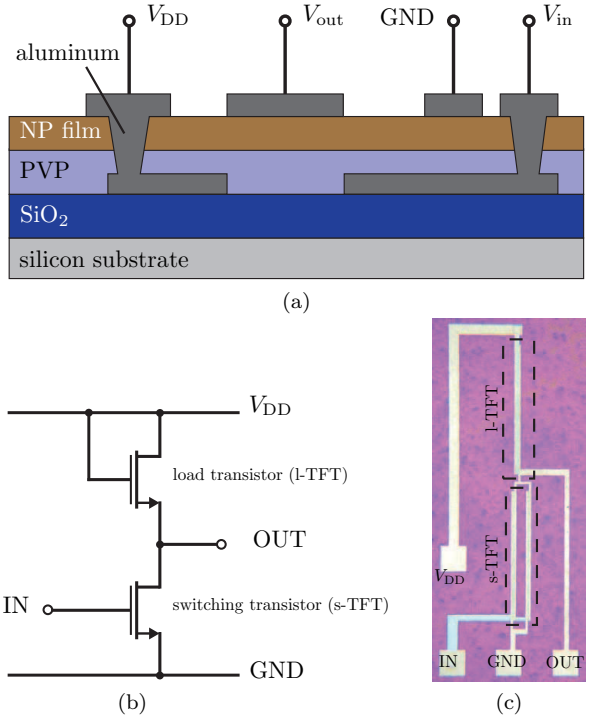
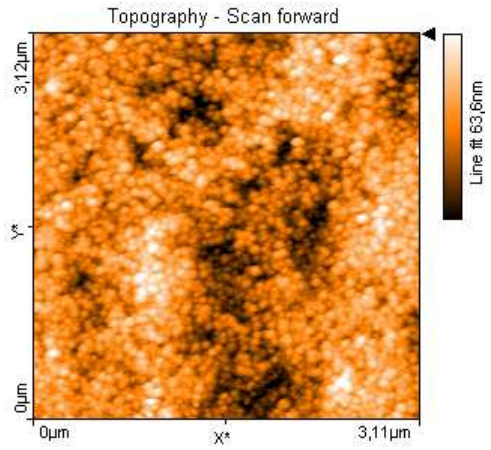


Figure 1: Schematic cross-section (a), circuit diagram (b) and optical micrograph (c) of the presented enhancement-load inverter device. V_{DD} denotes the supply voltage.

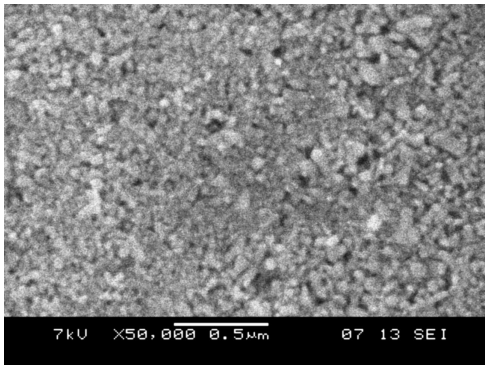
which uses ZnO nanoparticles as active layer material and a polymer as gate dielectric layer, are presented in this paper. The maximum temperature during the integration flow is 200℃ to demonstrate a process, which is compatible to plastic substrates.

2 DEVICE INTEGRATION

The inverter circuit is schematically depicted in Fig. 1. For the integration of the devices, a cleaned silicon substrate was thermally oxidized (300 nm). Then, a thin layer of 50 nm aluminum was deposited by e-beam evaporation and structured to gate electrodes. A cross-linkable poly(4-vinylphenol) (PVP) solution was prepared and spin-coated over the gate electrodes to form a closed gate dielectric film. After thermal cross-linking at 200℃ for 1 h, contact vias were etched into the PVP



(a)



(b)

Figure 2: AFM-topography (non-contact mode) (a) and SEM micrograph (b) of an ZnO nanoparticle layer.

layer using a RIE oxygen plasma. The composition of the solution, the spin-coating process parameters, film properties and the RIE process are described in [13].

In order to deposit a ZnO layer, an aqueous colloidal dispersion with a solid fraction of 34%wt ZnO, received from Evonik Degussa GmbH (Germany), was first treated in an ultrasonic bath to crack up loose agglomerates. The dispersion was then spin-coated over the dielectric layer and pre-baked at 120℃ for 5 minutes to evaporate the water. Afterwards, the samples were annealed at 200℃ for 1 h. Thereby, improvement in adherence to the PVP layer as well as in the electrical properties was achieved. SEM analysis of a sample's cross-section revealed a layer thickness of approximately $250-400$ nm. The mean root square roughness, which was determined by AFM measurement, was 12 nm. Fig. 2 shows the AFM topography of the ZnO nanoparticle layer and the SEM micrograph.

The deposition and structuring of the drain- and source-electrodes finished the device integration. The drain-/source-electrodes were defined by negative optical lithography and a layer of 200 nm aluminum was e-beam evaporated before performing a lift-off process.

3 RESULTS AND DISCUSSION

On-wafer electrical measurements at room temperature in darkness were performed using a HP 4156A Precision Parameter Analyzer. The relative humidity was approximately 40% throughout all measurements.

3.1 Individual Transistors

The transfer and output characteristics of typical TFT devices with Al- and Au-gate-electrodes are shown in Fig. 3. The transistor parameters are listed in Table 1, whereas the indices 'f' and 'b' denote the forward and backward sweep, respectively. The charactersistics

Table 1: Transistor parameters of the TFTs in Fig. 3.

	Al-gated TFT	**Au-gated TFT**
$V_{\mathrm{th,f}}$	3.6 V	2 V
$V_{\mathrm{th,b}}$	-0.9 V	-2.2 V
V_{hys}	4.4 V	4.2 V
μ_{FE}	$2 \cdot 10^{-3}\,\mathrm{cm}^2/(\mathrm{Vs})$	$2 \cdot 10^{-3}\,\mathrm{cm}^2/(\mathrm{Vs})$
$I_{\mathrm{ON}}/I_{\mathrm{OFF}}$	$2 \cdot 10^4$	$1 \cdot 10^3$

of both devices are dominated by hysteresis. With V_{hys} as the difference of the threshold voltages between the forward and the backward sweep, the amount of hysteresis is virtually the same for Al- and Au-gated devices. The hysteresis is mainly caused by charge trapping in the PVP layer, whereas it indicates an insufficient degree of cross-linking [14,15]. It has to be mentioned that Al-gated devices with solely positive threshold voltages were available. Obviously, the field-effect mobility is affected rather by the semiconductor than by the contact interface, because mobilities of $2 \cdot 10^{-3}\,\mathrm{cm}^2/(\mathrm{Vs})$ were found for both types of TFT. Nevertheless, the contact metal influences the off-state of the transistor, which can be seen from the lower on/off ratio of the Au-gated transistors as well as from the lower threshold voltages. With regard to the output characterisics, the Al-gated device shows a well-defined saturation regime, whereas the Au-gated TFT exhibits a break-down for high V_{DS}, in particular for low V_{GS}.

With the higher on/off ratio, the higher threshold voltages and the stable saturation regime, the TFT with Al-gate-electrodes are suitable for the integration of inverter devices.

3.2 Inverter Devices

A voltage transfer characteristic (VTC) of an inverter device using Al-gated TFTs is depicted in Fig. 4 for a supply voltage $V_{\mathrm{DD}} = 15\,\mathrm{V}$. As already observed in the individual TFT, the VTC is dominated by hysteresis, too. Nonetheless, the inverting function is clearly visible and the minimum and maximum output levels

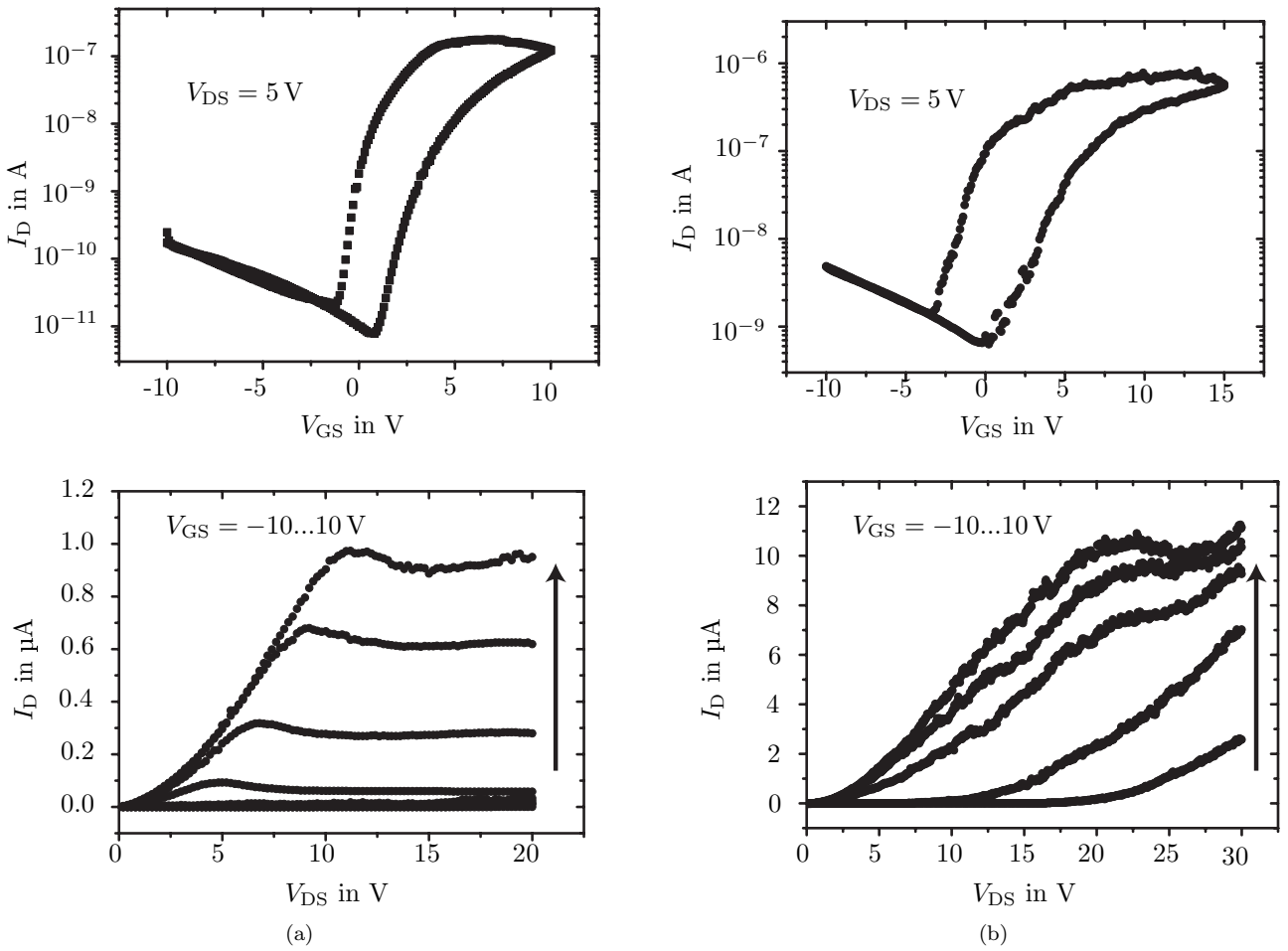


Figure 3: Transfer characteristics and output characteristics of individual ZnO nanoparticle TFTs with aluminum (a) and gold (b) gate electrodes. The channel width and length are 1000 µm and 3 µm, respectively.

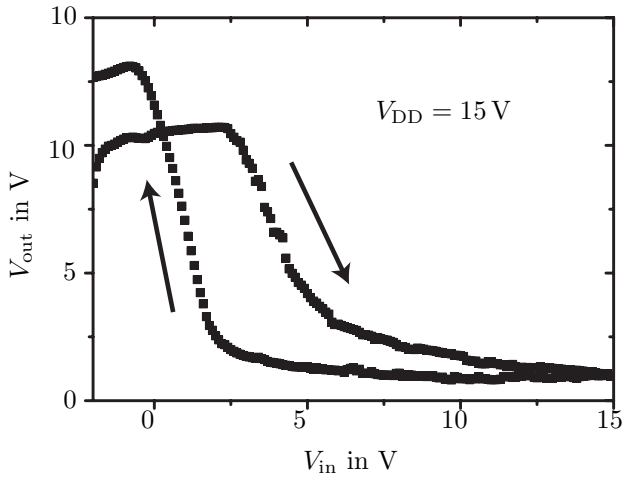


Figure 4: Voltage transfer characteristics of an integrated inverter at $V_{DD} = 15\,V$.

are $0.06 \cdot V_{DD}$ and $0.88 \cdot V_{DD}$, respectively. The latter one is only achieved for the backward sweep.

A figure of merit for inverter devices is the maximum peak gain v_p, which is defined as $v_p = \max|\partial V_{out}/\partial V_{in}|$. For the presented inverter in Fig. 4, the maximum peak gains are $v_{p,f} = 3.6\,V/V$ and $v_{p,b} = 6.0\,V/V$. These values are superior to inverter devices, which were integrated by plasma-enhanced chemical vapor deposition [9] and plasma-enhanced atomic layer deposition [8].

It has to be noted that the transition points, where $\partial V_{out}/\partial V_{in} = -1$, occur at relatively low V_{in}. This behavior is due to either the low threshold voltages or a mismatched geometry ratio. The geometry ratio is the ratio of the W/L of the load and the switching transistor. The geometry ratio of the presented device was 25. Generally, there is a relation between the geometry ratio and the maximum peak gain: the higher the geometry ratio, the higher the expected maximum peak gain. However, a shift of the transition points to low V_{in} is induced, if the geometry ratio is too high. In the presented case, it is neccessary to apply a negative input

voltage to obtain a high output level. Therefore, the geometry ratio and the threshold voltage have to be adjusted or a level-shifter diode has to be introduced for further investigations [16]. In particular, the threshold voltage shift can be obtained by using an alternative material for the drain/source electrodes or by thinning the ZnO nanoparticle layer.

The static power dissipation P_s was calculated from V_{DD} and the measured I_{DD}. Since the likelihood is equal for both logic levels, the static power dissipation denotes as $P_s = 0.5 \cdot V_{DD} \cdot I_{DD}$. With $I_{DD} = 80\,\text{nA}$ at $V_{in} = 15\,\text{V}$, P_s was 600 nW, which is reasonable for a nanoparticle device.

4 CONCLUSION

An enhancement-load inverter device was demonstrated. The inverter circuit consisted of two TFTs, which used a semiconducting ZnO nanoparticle layer as active material. The integration process is simple and cost-effective, because the semiconductor film is deposited by spin-coating of a colloidal dispersion. As a gate dielectric layer, a polymeric PVP film was used.

The inverter devices show reasonable characteristics with a maximum peak gain of 6 V/V and a low static power dissipation. For further investigations, an adjustment of the treshold voltage has to be done in order to shift the transition region for symmetric characteristics.

ACKNOWLEDGEMENT

The authors would like to thank Tim Konopka for his participation in sample preparation, the German DFG for funding (Hi551/24-1) and Evonik Degussa GmbH, Creavis Technologies & Innovation for the nanoparticle supply.

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