

Effective Carbon Nanotube Materials and Design Strategies for CNT-Based Electronics

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ABSTRACT

Lockheed Martin together with Rice University and Sandia National Laboratories are actively involved in the development of devices using carbon nanotube materials (CNTs) for various sensor and electronics applications. Micro-devices fabricated with different types of nanotube networks (different CNT sources, randomly oriented tubes vs. aligned tubes, dense tube coverage vs. sparser coverage, material with as-synthesized metallic tube content vs. highly enriched semiconducting content) are characterized for electrical behavior as part of our ongoing research activities aimed at addressing the widely recognized challenges facing the effective development of this technology. Associated material characterization results are also presented.

Keywords: carbon nanotube, synthesis, metallic, semiconducting, device

1 INTRODUCTION

Many groups are hoping to exploit the beneficial properties of carbon nanotubes (e.g. direct semiconductor bandgaps, high carrier mobility, and high surface area) for next-generation electronic devices and advanced sensors, and many different device fabrication processes and types of nanotube devices have been demonstrated. Despite the significant progress in these areas, it is recognized by most that in many target applications the complex nature of available CNT materials (with their mixture of CNT types and contaminants) and other material-related issues are major impediments to achieving the full potential of CNT devices.

Lockheed Martin (LM), Sandia National Laboratories (SNL), and the Rice University (RU) Smalley Institute are collaborating on understanding and mitigating these issues from a number of angles. Our efforts range from modifying CNT synthesis to achieve a greater degree of control of CNT properties, to developing and demonstrating new material and device processing routes. Developing our understanding of CNT device behavior via advanced physical models is another area in this collaboration, but is not discussed in this paper.

2 CARBON NANOTUBE DEVICE FABRICATION

There are a variety of methods available for incorporating CNTs in electronic devices. Some of these methods, such as spin or spray coating substrates with CNT suspensions, are attractive because they are familiar to CMOS process engineers and are straightforward to implement. These methods offer a lot of options for different suspending solvents, stabilizing methods (e.g. surfactants), and process variables such as suspension concentration and number of coatings applied to the substrate. Figure 1 shows an atomic force microscope (AFM) image of a field-effect device made from a suspension of single-walled carbon nanotubes (SWCNTs). A number of nanotubes can be seen bridging the source-drain gap.

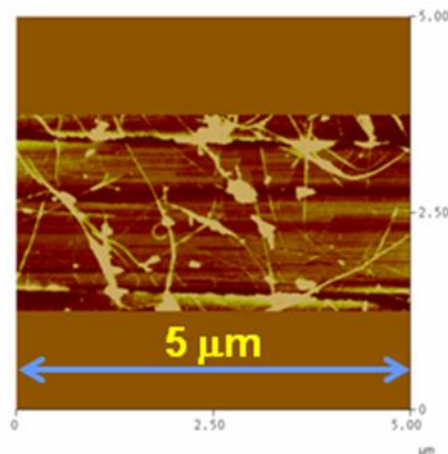


Figure 1 AFM image of a multi-SWCNT device. Top and bottom areas are source and drain. The silicon substrate is used as a back gate.

Some applications, particularly sensing applications where the maximum detection sensitivity is desired, require higher nanotube densities or larger nanotube surface areas than shown above. Multiple spin coats can be used to build up a denser film of nanotubes, and the nanotube film can be patterned by standard lithographic and etchant methods, and

metal contacts applied. An example device made in this manner is shown in Figure 2. We refer to the nanotube network of this type as a “random” mat since there is no preferred orientation of nanotubes.

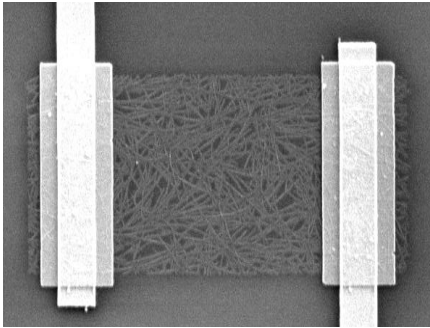


Figure 2. SEM image of a patterned SWCNT random mat in a two-terminal device made at LM.

When the source-drain channel length exceeds the average nanotube length the probability for conduction paths spanning from contact to contact along single nanotubes becomes low, and inter-tube “junctions” become important factors in device performance. Wet deposition methods such as spin coating are usually limited to nanotube lengths on the order of 1 micron because it is difficult to suspend longer tubes without breaking them up in the suspension process. Devices made by this approach with S-D channels much larger than 1 micron, have many tube-tube interactions affecting their conduction.

An alternate approach developed by the Smalley Institute at RU [1] is depicted in Figure 3. Vertical forests of SWCNTs are grown in patterns of lines which are laid over to form a film of aligned nanotubes. This film can easily be transferred to another substrate for subsequent device processing. The length of nanotubes in a laid-over film is limited only by the growth length (which can be 100s of microns) and the ability to successfully lay the forest rows over. Figure 4 shows SEM images of the aligned film and a simple device made from such a film where the device channel is smaller than the original forest height, so nanotubes span from one contact to the other. This approach results in a device with a high density of aligned tubes. Of course, the film in this case contains the as-grown material with its full range of nanotube types (metallic and semiconducting).

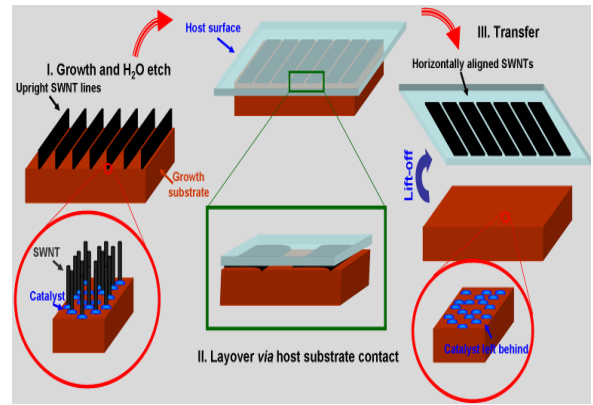


Figure 3. RU method of creating an aligned SWCNT film via patterned vertical forest growth and dry film transfer.

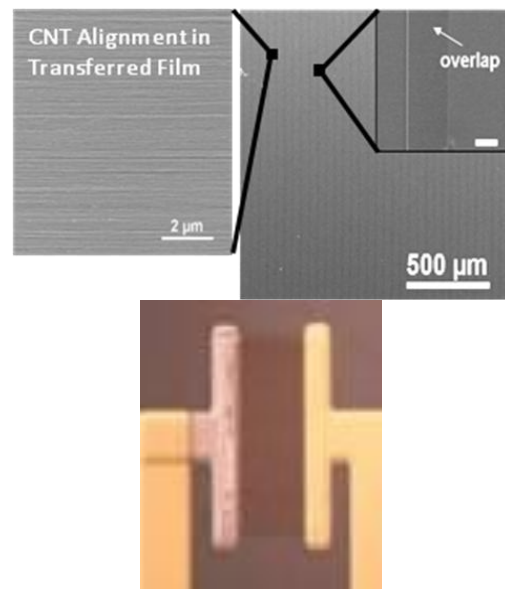


Figure 4. Top: SEM images of an aligned SWCNT film. Bottom: Two terminal device made from aligned SWCNT film (processed at LM).

3 DEVICE BEHAVIOR VERSUS NANOTUBE CONDUCTION TYPE

One of the biggest challenges in the application of carbon nanotubes in electronics is dealing with the complex nature of the mixture of tube types and contaminants produced by all CNT synthesis methods. As-synthesized SWCNTs are a mixture of “metallic” conducting and semiconducting tubes. The presence of metallic conducting SWCNTs in a device can short out the device if they form a conductive path connecting source and drain contacts. Metallic tubes might also screen field gradients that some devices rely on to drive carrier current. For this reason, numerous groups are working on methods to remove metallic nanotubes from the starting material or mitigate

their effects in fabricated devices by other means. One approach that can be applied at the device level is breaking high-conduction pathways by driving current through the device until tubes on those paths fail. This is demonstrated for the device of Figure 1. After metallic tube burnout, on-to-off current ratio improves, as shown in Figure 5. This approach works well when the number of nanotubes in the channel is small, or the conduction network is close to metallic tube percolation, but may not work well with denser mats with high metallic tube content.

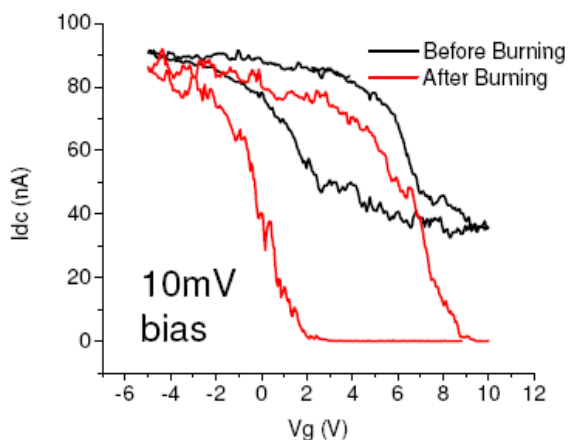


Figure 5. I-V curves for SWCNT device of Figure 1 before and after breaking metallic tube conduction via Joule heating.

Other strategies for mitigating metallic tubes include chemical destruction of metallic tubes, functionalization of metallic tubes to convert them to semiconductors, and avoidance of metallic tube percolation by device design. The nanotube material can also be processed to separate out metallic tubes before device fabrication. Avouris and co-workers demonstrated this approach by making CNT field-effect transistors with high-semiconducting content SWCNT suspensions prepared by density gradient ultracentrifugation (DGU) [2]. We adopted this approach for our random-mat devices and saw improvements in device behavior with reduction of metallic tube content. Table 1 shows that, as the metallic tube content of the nanotube network decreases, our SWCNT field-effect devices showed more gate-voltage dependence in their I-V characteristic. More work is needed to improve device performance further and to purify the materials to meet CMOS standards.

SWCNT Material Source	Metallic CNT Fraction	Resistance change (Gate: -10 to +10V)
SWeNT CG	33%	3%
NanoIntegris Puretubes	20%	18-25%
SWeNT SG	10%	13-18%
NanoIntegris IsoNanotubes-S, 95%	5%	22-85%

Table 1. Change in random-mat SWCNT device resistance (measured by slope of I-V curve near zero bias in gated two terminal devices with 6 x 5 micron CNT mats) with % metallic tube content.

4 VARIATION OF NANOTUBE TYPE VIA SYNTHESIS

Carbon nanotube synthesis is an active research area, with many groups exploring methods to make nanotube materials with improved characteristics or specific types. We use chemical vapor deposition (CVD) by the so-called supergrowth (H₂O vapor assisted) method to grow our vertical nanotube forests. The supergrowth method we use with substrate-bound nanoparticle catalysts formed from thin metal films makes larger-diameter single-walled CNTs than HiPCo or laser-based methods. It has been shown by others that nanotube diameters can be controlled by varying temperature or carbon source feed rate [3]. However, the results of this earlier work produced SWCNT diameters smaller than we require. We are investigating how pre-selected nano-sized catalyst particles might be used to control nanotube diameter. Nishino, et al., [4] reported growth of SWCNT with average diameters of 3 nm from colloidal Fe-Mo nanoparticles. We used pre-formed catalyst nanoparticles (NPs) from a synthesis similar to theirs and from two commercial sources. Data on diameters for these NPs are given in Table 2. SEM images of nanotube forests grown from the commercially sourced NPs are shown in Figure 6, and a Raman spectrum for tubes grown from 5 nm NPs are shown in Figure 7. The forest heights and Raman data (high G/D peak ratio) indicate that efficient nanotube growth was achieved. We are currently analyzing these materials to determine nanotube types and diameters grown and other factors.

Source	Diameter (nm)	Composition
Vendor #1	5 ± 1	Iron Oxide
Vendor #2	6.5 ± 3	Iron Oxide
Our Synthesis	~3	Fe-Mo oxide (90+% Fe)

Table 2. Nanoparticle diameters and compositions.

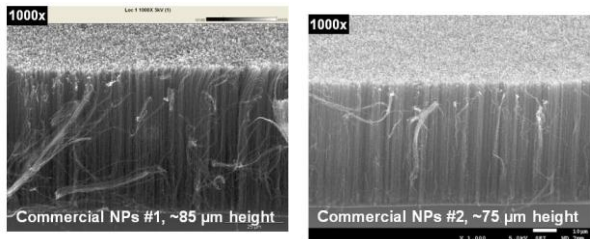


Figure 6. SEM images of vertical SWCNT forests grown from pre-sized nanoparticle catalysts.

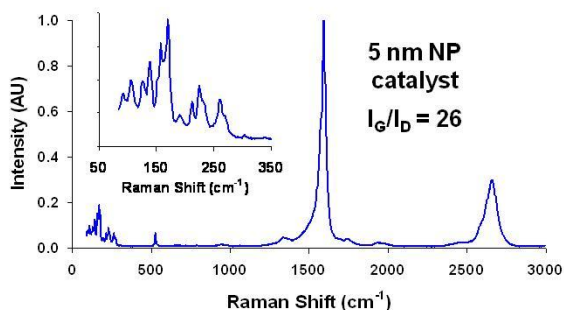


Figure 7. Raman spectrum of SWCNTs grown with 5 nm nanoparticle catalysts.

5 SUMMARY

Many of the challenges associated with carbon nanotube-based electronic and sensor devices are materials-based. Working on CNT synthesis, device design, device fabrication, models, and materials characterization, Lockheed Martin, Sandia National Laboratories, and Rice University are addressing some of these challenges.

We gratefully acknowledge funding from the Lockheed Martin Corporate Engineering & Technology and Space Systems Company Internal Research and Development programs. The work at Rice University was supported by the Lockheed Martin Advanced Center for Nanotechnology at Rice University (LANCER) program. Sandia National Laboratories acknowledges support from the LM Shared Vision R&D program.

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