Crystalline Silicon Solar Cell Efficiency Improvement by Advanced Cleaning Technology

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ABSTRACT

Sunsonix has identified technology gap/need in the area of crystalline silicon photovoltaic efficiency and field degradation. The cause of both poor efficiency and rapid degradation may share common roots. Trace contamination at the photovoltaic junctions lead to both mid-level traps and photonic defects. In other words, very small amounts of contamination can result in poor photovoltaic efficiency as well as susceptibility to further efficiency decay when exposed to sunlight after field installation. In recent trials we have conducted best of class cleans that increase the implied open circuit voltage by 3%. In manufacturing split lot trials for both batch and in-line wet cleaning tools a post texturing etch resulted in a cell efficiency increase of 0.3% absolute on multi-crystalline Si wafers.

Keywords: silicon, solar cell, cleaning, efficiency

1 INTRODUCTION

Over the past 30 plus years, considerable effort, has been expended to eliminate deleterious contaminants that degrade transistor performance in the manufacture of integrated circuits. Surface engineering through advanced cleaning and handling processes have resulted in the ability to continue scaling according to the well known Moore's law. These same contaminants so aggressively addressed in the SEMI industry have not been addressed in the Silicon PV manufacturing processes. With the volume throughput of silicon for PV at 10 to 100 times that of semiconductor PV the same methodologies developed for SEMI are not economically or manufacturing scalable. For instance in the SEMI industry, wafers are transported in individual slots of pristine fluorocarbon wafer carriers from silicon foundry to semiconductor fab. In the PV industry wafers are transported in Styrofoam containers or worse yet cardboard boxes and delivered to the PV fab. More often than not, PV wafers only receive a quick deionized water rinse, HF dip to remove native oxide and a final deionized water rinse. Other PV manufacturers add rudimentary SC1 or SC2 cleans, while a few follow sound cleaning practices, at least from a 1990's IC semiconductor perspective; due to cost pressures, cleaning baths are often used far longer than IC manufacturers would ever consider feasible. One must also consider that, whereas an IC is a thin thin film device with stringently controlled interfaces and *local* criticality, Si PV is *bulk* device with relatively uncontrolled critical interfaces.

Compounding these differences in the devices, neither the deionized water rinse or acid (e.g., HF or HCl) dip are effective at removing transition metal contaminants such as Fe, Ni, Cr, Cu, Zn and others that are mid-level traps responsible for severe degradation of minority carrier lifetime. Photovoltaic efficiency is directly correlated to minority carrier lifetime through increased open circuit Voltage.

Sunsonix has developed a cleaning chemistry that efficiently removes interfacial transition metals and most metal cations in both HF based surface cleans and SC 2 HCl based cleans. The chemistry can also be applied directly in a deionized water bath or added directly to a KOH texturing bath. This versatility of the chemistry makes the Sunsonix clean (SX-E™) a "drop-in" replacement for existing silicon based photovoltaic manufacturing lines.

2 EXPERIMENTAL

The goal for a cleaning chemistry for PV crystalline applications is to eliminate surface contaminants that arise from the processing of crystalline substrate material or unintentionally added to the manufacturing environment. The contamination for which the Sunsonix SX-E™ clean has been developed is those of metallic cations liberated into the wet processing baths. In the normal course of processing a wafer, two process steps are the most critical with respect to damaging the solar cell surface. These two steps are discussed below.

2.1 Post-Texturing Clean

The first is the removal of contaminants after the texturing etch. The texturing etch (KOH and alcohol) modifies the silicon surface by providing an optically rough surface that traps light incident to this surface [3]. The texturing etch removes bulk material from the wafer. Any contaminant present in the silicon substrate that is removed is liberated into the texturing bath. Iron and other transition

metals are present in most substrate at levels below $1x10^{11}/cm^3$, and therefore a substantial concentration of these metals can build up in the texturing bath. Equilibrium exists between the textured silicon surface and the bath eventually resulting in a substantial surface concentration of the contaminating metal. After the texturing etch the wafer is removed and neutralized by addition to an acid bath. This bath is usually a dilute solution of HF and sometimes HCl. Any metallic contamination present on the wafer surface is transferred to this bath.

In this bath the metallic contaminant is not selectively removed from the substrate, again due to the equilibrium set up between the silicon surface and the chemical bath. This equilibrium between the surface and the chemical bath can be adjusted by small additions of a chemical that effectively sequesters the metallic contaminant. The preferential sequestration of the metallic contaminant, with selectivity ratios in excess of 10^6 for metallic cations, is responsible for the effectiveness of the Sunsonix approach to removing metallic contaminants from the silicon surface.

Two separate experiments were conducted utilizing Sunsonix chemistry (SX-E™) for post texturing clean chemistry. In our first experiment $\leq$ 300 ppm of the SX-E™ is added to the first of two D.I. water rinses immediately following a 5% HF post texturing neutralizing / cleaning bath. The addition of this chemical is provided directly to D.I. water bath. The substrates are monocrystalline silicon substrates with the experiments conducted in a small wet bench in a university laboratory.

Wafers are removed from the texturing bath clean and the minority carrier lifetime measured by a Sinton Consulting WCT120 minority carrier lifetime tool [1]. The implied open circuit voltage is measured and compared to a two step, standard D.I. water rinse.

In our second experiment trials are conducted on a 80MW production fab. Here 300 ppm of the SX-E™ is added to the post texturing neutralizing acid bath. Split lots of wafers are run to compare the fab process of record and the SX-E™ clean. Wafers are then processed in the normal process sequence, emitter diffusion, PSG removal, anti-reflection coating and contact formation. Cell efficiency of the two lots of wafers is measured, recorded and statistical efficiency differences recorded.

2.2 PSG Removal Clean

The formation of the emitter for p-type silicon solar cells involves the diffusion of phosphorous into the top layer of one side of the silicon. This is accomplished by a high temperature anneal in a phosphorous rich ambient usually with phosphorous oxychloride (“$POCl_3$”). One key benefit of the phosphorous anneal is the formation of phosphosilicate glass (PSG) layer on top of the diffused emitter. The PSG layer acts like a getter for transition metal impurities especially iron. The iron preferentially diffuses to the PSG surface in a process termed gettering. This phenomenon is very well understood and is often used in semiconductor manufacture of bipolar devices that require high carrier lifetimes, similar to the needs of the PV application. However to remove the iron from the PSG requires a cleaning sequence that involves stripping the PSG by HF and then cleaning the metals from the surface by subsequent cleans in standard clean 1 (SC1) ($NH_4OH:H_2O_2:6H_2O$) and standard clean 2 (SC2) ($HCl:H_2O_2:6H_2O$) followed by another HF clean. HF cleans do not effectively remove transition metals from the surfaces of silicon. Many in the PV industry, in an effort to minimize costs, have eliminated the SC1 and SC2 steps. This choice leaves the possibility that transition metal impurities are left on the surfaces by the PSG removal strip or re-reacts with the Si surface through the previously discussed solution equilibrium. This is particularly the case with PSG strip baths used for subsequent substrate lots throughout a day. Realizing this aspect of the HF clean, SX-E™ added to the D.I water rinse immediately after the PSG strip can sequester the transition metals, effectively removing them from the surface.

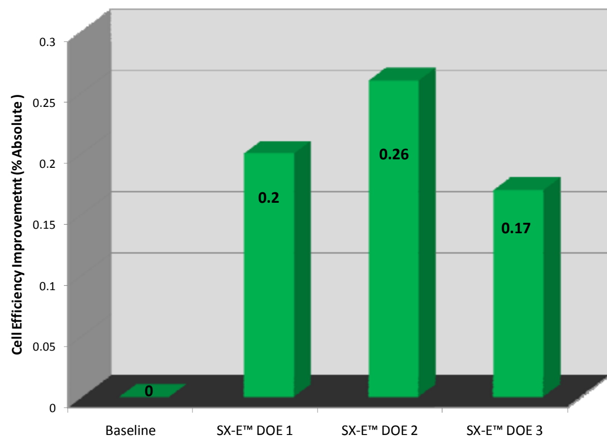
To evaluate this clean 300 ppm of SX-E™ is added to the first of two D.I. water rinses immediately following a 5% HF PSG stripping bath. The chemical is added directly to D.I. water bath. The processed substrates are monocrystalline silicon substrates. Wafers are removed from the PSG bath clean and the minority carrier lifetime is measured by Sinton WCT120 minority carrier lifetime tool. The implied open circuit voltage is reported and compared to a two step, standard D.I. water rinse.

2.3 Iron Challenged Surfaces

In order to demonstrate the effectiveness of the Sunsonix clean we intentionally contaminated pristine FZ silicon surface with iron. In this experiment the surfaces of the wafers were contaminated with iron by immersion solution of iron nitrate in dilute nitric acid solutions. Five different solution concentrations over five decades were used to contaminate the wafers. After immersion, wafers were subjected to two alternate cleans one consisting of a 5% HF bath and the second a 5% HF bath with 300 ppm of the Sunsonix SX-E™ chemistry. Wafers were then annealed for 20 seconds at 750 °C to electrically activate any contaminants. Wafers were then cleaned in 5% HF and immediately immersed into an Iodine/Methanol bath to passivate the wafers. Minority carrier lifetimes of these samples were measured by photoconductivity decay according the RCPCD method [2]. The measured minority carrier lifetime is reported.

3 RESULTS

3.1 Post Texturing and Post PSG Clean of Monocrystalline Silicon



The reported implied V_{oc} comparison for the Sunsonix clean for both the post –texturing clean and post PSG clean is reported in Figure 1. The implied open circuit voltage is calculated from the measured carrier lifetime and carrier injection. In figure 1 the post texturing clean result is shown as the post diffusion and the post PSG. . Post-PSG anneal substrates showed less impact, but still positive at 1.6%, as measured by V_{OC}. We can not assume that all other variables of the PV efficiency equation (FF, I_{SC}, etc.) were equivalent, because they were not measured. However, this very large increase in V_{OC} would imply at least some dramatic improvement, at least in those materials aspects that impact V_{OC}.

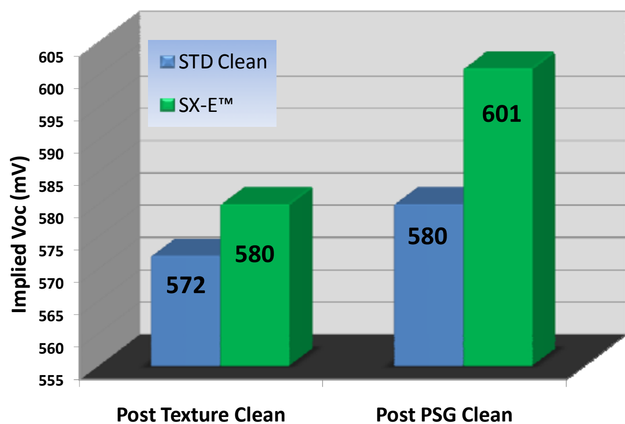


Figure 1: Improved open circuit voltage (V_{oc}) of Sunsonix Clean compared to a standard clean. The final V_{oc} improvement results in a > 3% improvement in open circuit voltage.

3.2 Post Texturing Clean of Multi-Crystalline Silicon

An 80MW multicrystalline silicon production line was used to conduct these experiments. Split lot trials on both a batch clean line and an in-line clean line. A design of experiments was conducted for each trial. Approximately 5000 wafers are processed for each set of experiments. The reported data represents the average measurements for each experiment.

Figure 2 shows the absolute efficiency change for each of the experiments for the batch clean line. The experiments adjusted both the concentration of the SX-E™ chemistry and the residence time of the wafers in the post texturing bath. The optimized cell improvement performance for this batch process is 0.26%.

Figure 2: Cell efficiency improvement for batch post texturing clean line for the Sunsonix SX-E™ chemistry.

In a second trial the Sunsonix SX-E™ chemistry was applied to an in-line cleaning station. The experiments adjusted both the concentration of the SX-E™ chemistry and the residence time of the wafers in the post texturing bath. Figure 3 shows the absolute efficiency improvement for each experiment.

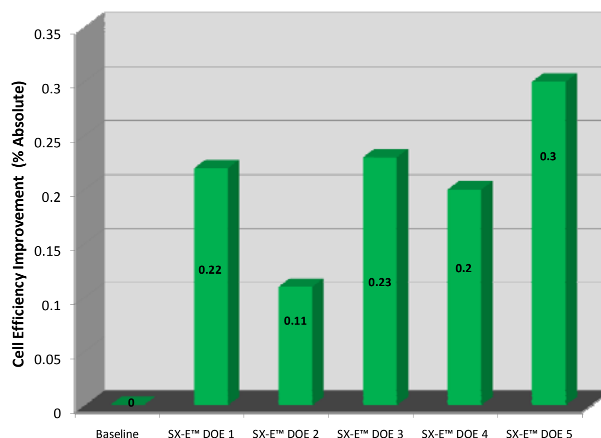


Figure 3. Cell efficiency improvement for in-line post texturing clean line for the Sunsonix SX-E™ chemistry.

Each experiment represents approximately 5000 wafers and the reported cell efficiency improvement is the average of these wafers. The optimized cell efficiency improvement is 0.3%, which is consistent with the improvement of 0.26% found in the batch tool.

3.3 Iron Challenged Surfaces

Crystalline silicon cell efficiency is directly related to the recombination rate of minority carriers in the silicon cell [4]. It is well understood that transition metal impurities in silicon material can dramatically reduce the minority carrier lifetime due to its occupation energy being about the middle between the valence and conduction bands; a (mid-gap contaminant [5].

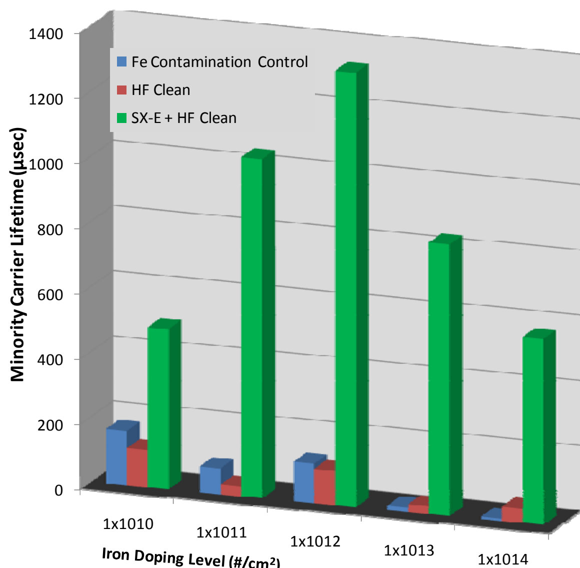


Figure 4. Performance of HF clean and SX-E™ + HF clean for intentionally contaminated FZ silicon wafers. Minority carrier lifetime is directly related to increased cell efficiency.

The contamination profile shows a non-linear response with respect to the iron doping level. This may be due to handling issues or that the SX-E™ chemistry was not fully optimized for these surface contaminant levels. Alternatively, the mechanisms associated with these differences in surface coverage, cleaning efficiency, and carrier lifetime may be different and are still being investigated. Regardless, the improvement even at the lowest contamination levels is dramatic.

4 DISCUSSION

It is clear that the presence of iron contaminant can have a strong influence on minority carrier lifetime and ultimately solar cell efficiency. The presence of iron and other transition metal contaminants is detrimental to solar cell efficiency. The SX-E clean can significantly reduce the presence of these contaminants ultimately improving solar cell efficiency. The demonstrated 0.2% to 0.3% absolute efficiency improvement by the SX-E™ clean chemistry provides a compelling advantage to crystalline solar cell manufacturers. The projected value for a typical 100 MW production line by the addition of the Sunsonix SX-E™ chemistry is approximately $3M to $4M per year. The advantage of the SX-E™ is that it is a drop-in addition to existing chemical processes in use by the crystalline silicon solar lines.

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