Jet-printed Si Nanowires for Flexible Backplane Applications

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ABSTRACT

The integration of Si nanowire (Si NW) materials with low-temperature plastic substrates can enhance the performance of low-cost flexible electronics. We report the properties of Si NW thin film transistors (TFTs) fabricated with various contact metals. We demonstrate the use of dielectrophoresis and inkjet printing to pattern and assemble Si NW TFTs from a liquid suspension in a manner that is suitable for display backplane applications.

Keywords: nanowire, printing, transistor, large-area, flex

1 INTRODUCTION

Semiconductor nanowires exhibit unique properties which can be tailored and exploited for a variety of device applications including electronic devices [1,2], optoelectronic devices [3,4] and sensing applications [5,6]. The ability to independently fabricate crystalline nanowires, along with their small mechanical size make them a good candidate for large-area and flexible electronics. However, the ability to position and place nanowires in a reliable and economic manner continues to be a considerable obstacle to realizing nanowire based systems.

Jet-printing solution processable semiconductors has been identified as a scalable, cost-effective process technology that is well suited for making large area electronics [7]. Furthermore, because jet-printing can be carried out at low temperatures it can also be applied to fabricate electronic devices on flexible, low-temperature substrates leading to many interesting applications such as flexible displays or sensor arrays [8]. Organic semiconductors are well suited for jet printing [9], but because of their low mobilities [10,11], may not be the best option for high performance large-area electronic systems. Si nanowires exhibit very high mobilities [12,13], much higher than that of amorphous Si or organic semiconductors. Because of their enhanced performance over amorphous materials, the ability to solution process and jet-print Si nanowires could provide an economic and scalable method to distribute nanowires as a means to fabricate high performance large-area and flexible systems.

Jet-printing nanowire suspensions is not straight forward. The suspended nanowires tend to be on the same length scale as the print head ejection nozzle. Because of this the print head is prone to clogging after short periods of time. Furthermore, the nanowire volume tends to be much smaller than that of the jet-printed drop in which it is deposited making it difficult to control the final position of the nanowire by controlling only the position of the printed drop. Fabricating a device at a specified location becomes very difficult because printing provides no assurances that a nanowire in suspension will be correctly oriented to connect the source and drain source and drain electrodes in a device.

In this paper we overcome these challenges and demonstrate the ability to fabricate a field effect transistor (FET) devices using jet-printed Si nanowires. We are able to prepare very dilute nanowire suspensions which allow the printer to function reliably for over a week without experiencing any clogging issues. These dilute solutions greatly reduce the number of nanowires that are deposited in a single printed drop. In order to control the final location of the nanowire, electric fields are generated on the printing substrate to induce a dielectrophoretic (DEP) force on the suspended nanowires. Dielectrophoresis refers to the force induced on a neutral, suspended particle, by a non-uniform, external electric field [14] and has already been shown to be an effective way to manipulate nanowires [15-19]. The induced DEP force can be used to orient and place nanowires across the channel of a FET device. Our approach is straight forward and well suited to print nanowires for display backplane applications.

2 PRINTING NANOWIRES

Silicon nanowires are grown in a CVD reactor using the vapor-liquid-solid approach at 450 °C with a chamber pressure of 100 Torr (and Si partial pressure of 2 Torr) for 15 minutes. 40 nm Au colloid is first dispersed across the surface of a <100> Si substrate to seed the growth. The as-grown nanowires have a diameter of approximately 90 nm and a length of about 50 µm (shown in Fig 1).

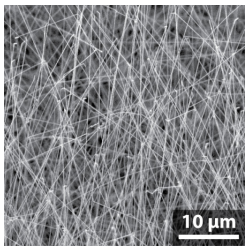

Figure 1: SEM image of as-grown nanowire.

The growth substrate is then placed in 5 ml of deionized water and sonicated for 30 seconds to create a nanowire suspension. After sonication the suspension is centrifuged to remove larger particles leaving nanowires that are well dispersed in the suspension. The resulting suspension is almost clear with a low density of nanowires that vary in length from about 5 to 20 µm.

The printing substrate is first prepared with alignment sites on which nanowires are printed and aligned for device fabrication. Standard processing techniques are used to fabricate Ti/Au source-drain electrodes on a Si <100> wafer with 1000 Å of thermal oxide. The source electrodes of all the devices are connected together, and to an external contact. The drain electrodes are all discrete. A layer of CF_4 plasma-treated photoresist is patterned such that there are openings in the channel region (or alignment sites) of each device where nanowires are to be printed. These opening serve to confine the drop as well as well as isolate individual devices from one and other.

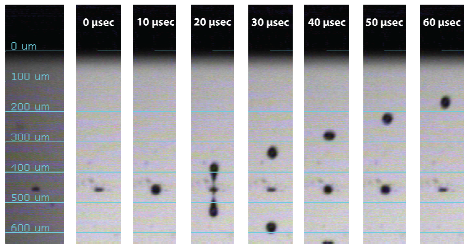

Figure 2: Strobe images of drop ejection sequence.

The nanowire solution is loaded into a commercially available ink-jet printer and then printed at each alignment site. The drop ejection sequence is shown in Fig. 2. With a properly centrifuged suspension the nozzle will jet reliably for more than one week. The common source electrode is connected to an AC voltage potential (10 V_{pp}, 10 kHz) during printing in order to induce a dielectrophoretic force on the suspended nanowires. The global Si wafer back gate is connected to ground. Once printing is complete a second Ti/Au layer is deposited (immediately following a BOE etch) in order to make electrical contact to the source and drain electrodes.

In order to utilize DEP it is necessary to generate an electric field at each alignment site. This field is typically generated by either connecting all devices in parallel or by using a separate set of connections that provide a signal at each alignment site while the suspension is present. These approaches are not suitable for systems having multiple interconnected devices such as large-area backplanes. In our approach the DEP signal is provided to all devices in parallel via the common source. The discrete drain at each device is capacitively coupled to the grounded substrate through the gate oxide which allows the source electrode potential to induce an electric field at each alignment site. This approach can easily be translated into a large-area TFT display back plane by shorting all the data lines and connecting them to an AC potential and shorting all the gate lines and connecting them to ground as shown in Fig. 3. In this way it is possible to deliver the needed DEP signal at each alignment site without significantly altering the design of the display backplane.

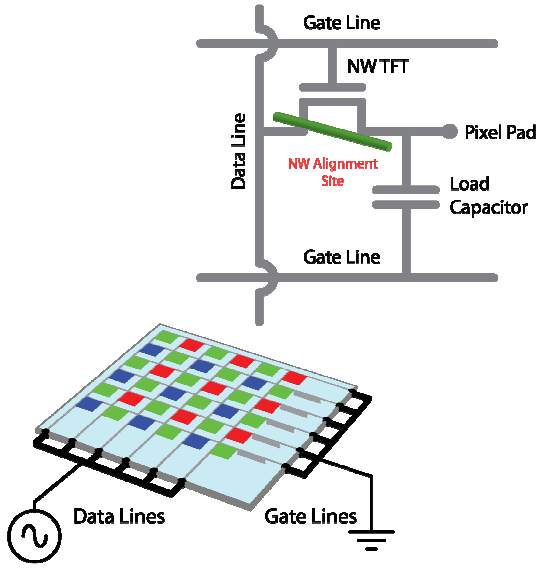

Figure 3: Circuit diagram of an individual pixel (upper right) for an array back plane highlighting the location of the NW alignment site. Cartoon of a full display backplane (lower left) illustrating the necessary connections to induce a DEP force at each alignment site in the array.

3 DEVICE PERFORMANCE

Figure 4 shows an SEM micrograph and measured electrical characteristics of a single jet-printed Si nanowire TFT device that was fabricated within a larger array. Devices in the array were found to be p-channel and exhibited on-off ratios of greater than 10^5. Threshold voltage values of -2.5 V and a mobilities as high as 50 cm^2/Vs were observed. Device parameter values are extracted by fitting the data using the gradual channel approximation based on the number of nanowires in the device, the gate capacitance of the nanowire and the applied voltages. The gate capacitance for each nanowire is computed using the wire-on-a-plate methodology [20].

Fig. 4 shows one printed device from a larger array. The alignment yield in the array was very good. More than half of the devices had nanowires that were placed such that device fabrication was feasible with approximately one - third of these devices having switching operation. While most of those devices showed very good on-off ratios, the contact resistance in these devices was too great to extract meaningful device parameters. All measured devices showed p-type operation, likely due to the work-function of the contact since the nanowires are nominally undoped. In order to improve device performance, device yield, and

control over device polarity it is necessary to examine the nanowire contacts more carefully.

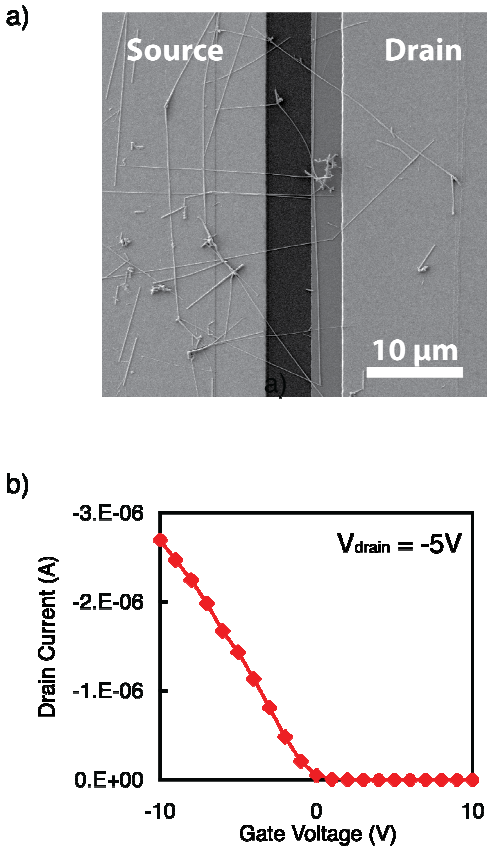

Figure 4: SEM micrograph (a) of a jet-printed and DEP aligned nanowire TFT device. (b) shows the corresponding transfer curve for the device.

4 DEVICE OPTIMIZATION

In order to better understand the nature of the nanowire contact material and its influence on device polarity TFT device were fabricated by mechanical transfer of the nanowires from its growth substrate onto a device substrate. In this process, the nanowires on the original growth substrate are put into direct contact to the process wafer. The growth wafer is then slid across the process wafer and the shearing force from the sliding transfers the wires and creates a nanowire matte onto the process wafer [21]. Bottom and top-gate nanowire FETs with SiO^2 gate dielectric and various metal contacts were fabricated using this process on nominally undoped Si nanowires. Direct metal contacts using Al metal at the source/drain regions resulted in p-channel devices having a threshold voltage of ~ -2V, similar to the jet-printed devices with Ti/Au contacts discussed above. N-channel devices were fabricated by using a doped a-Si n^+/metal contact. These FETs had threshold voltage of < 5V and field-effect mobility of ~ 60 cm^2/Vs. These experiments further highlight the influence of contact materials on device behavior.

5 CONCLUSIONS

High performance large-area and flexible electronics can benefit from the performance advantages afforded by Si nanowires over amorphous semiconducting materials typically employed in these applications. We have demonstrated the ability to fabricate TFT devices with mobilities as high as 50 cm^2/Vs by jet-printing Si nanowire suspensions on a device substrate. Such an approach allows Si nanowires to be utilized in a cost-effective and scalable way that should be well suited for flexible displays and other large-area applications.

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