Architecture for Designing Noise-Tolerant QCA Nanocircuits

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ABSTRACT

Due to many random factors from thermal fluctuations to wave interference, computation perfection in nanoICs is hard to achieve. Defects and faults arise from noise susceptibility of nanoICs which leads to unreliable results. A probabilistic computational model is needed to cope with such errors and to achieve more reliable computations. The main purpose of this paper is to present a new architecture for designing noise-tolerant Quantum-dot Cellular Automata (QCA) nanocircuits.

Keywords: Nano-scale Architecture, Molecular Electronics, Quantum Devices, Fault Tolerance

1 INTRODUCTION

In the past sixty years, these are many groups of researchers working on the problem of how to design reliable circuits. A good review of various approaches to this problem is documented in a recently published book by Mary Eshaghian-Wilner [1], in which the most commonly-used approach is the redundancy technique, such as, using majority gates and/or multiplexers. Furthermore, most of the researchers in the past provided solutions to transient and permanent faults in computational circuits, but so far no group has focused on faults due primarily to environmental noise (thermal noise, electromagnetic noise and random physical defects.) The method presented in this paper is focused on the design of reliable QCA nanocircuit which is immune to noise. The architecture proposed to achieve such a design in shown in figure 1 followed by an example of how this would be used for a QCA full adder in figure 2. Note that in this design, each output of the circuit is connected to a specially designed Reliability Enhancement Nano Wire (RENW) which will enhance the reliability of the output to any desirable level, that is, to approach infinitely close to a Boolean logic value 0 or 1. The construction of RENW using QCAs and the explanation of why RENW can enhance circuit reliability in such a profound way will be presented. The design of a noise-tolerant 1-bit binary QCA full adder is given to illustrate the method. The result is verified though a simulator.

The architecture presented in this paper for enhancing reliability is completely general and thus applicable to the design of noise-tolerant reliable nanocircuits using other nanotechnologies.

REFERENCES

[1] M. Macucci, Ed. Quantum Cellular Automata, London, UK: Imperial College Press, 2006

[2] M. Mehrnoosh and E. Wilner, Eds., Bio-Inspired and Nanoscale Integrated Computing. Hoboken,NJ: Wiley, 2009.

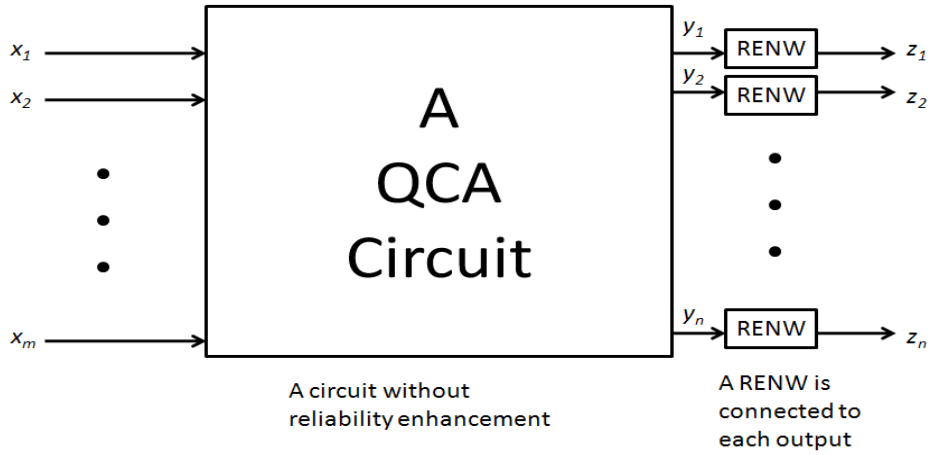

Figure 1. Design of noise-tolerant QCA circuit. Note: RENW stands for Reliability Enhancement Nano Wire y1, y2,...,yn, are circuit outputs z1, z2,...,zn, are reliability enhanced circuit outputs

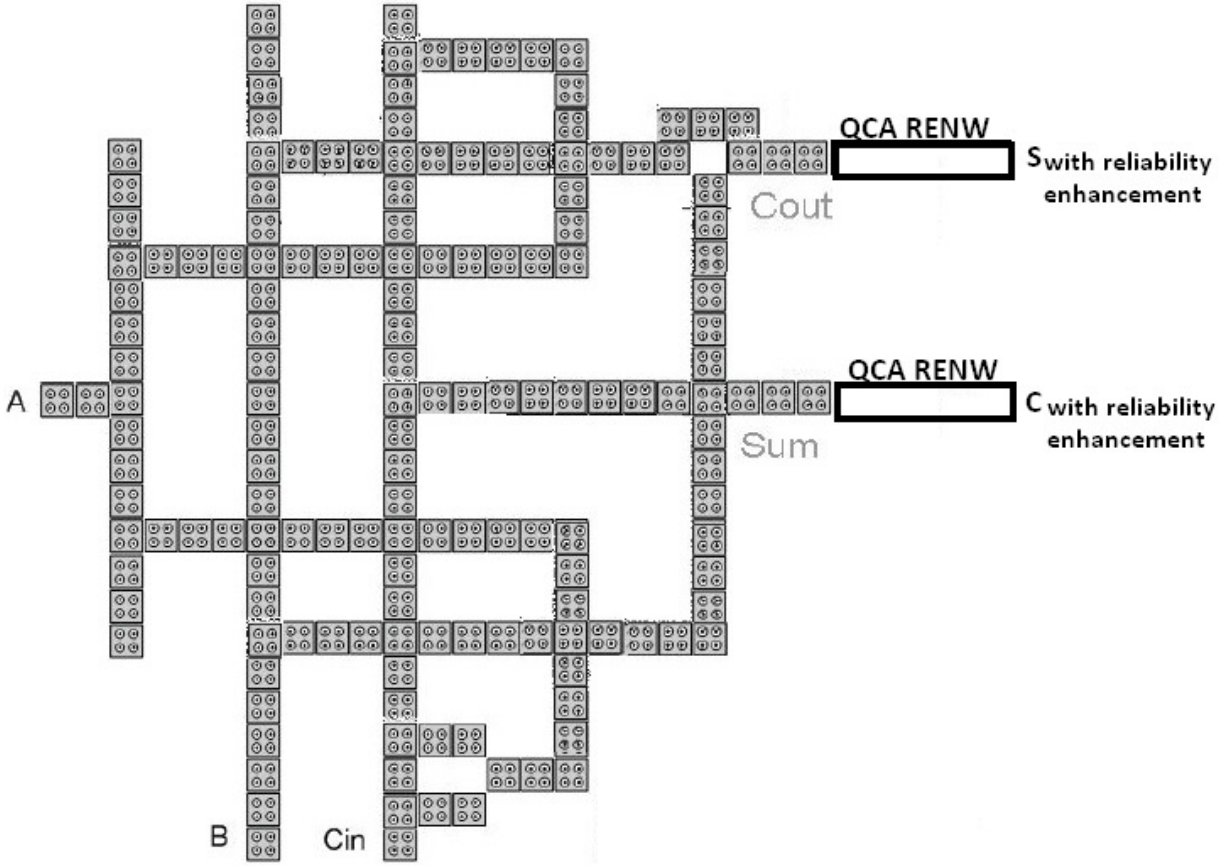

Figure 2. Design of noise-tolerant QCA 1-bit full adder