

Non-Charge-Sheet Analytic Model for Ideal Retrograde Doping MOSFETs

Zhize Zhou^{*,**}, Jian Zhang^{*,**}, Xingye Zhou^{**}, Xinnan Lin^{*,**} and Jin He^{*,**,*}

^{*}The Key Laboratory of Integrated Microsystems, Shenzhen Graduate School of Peking University, Shenzhen 518055, P. R. China, hejin@szpku.edu.cn

^{**}TSRC, Institute of Microelectronics, School of EECS, Peking University, Beijing 100871, P. R. China

^{***}Peking University Shenzhen SOC Key Laboratory, PKU HKUST Shenzhen Institute, W303, West Tower, IER Bldg., Hi-Tech Industrial Park South, Shenzhen 518057, P. R. China

ABSTRACT

This paper presents a physics-based non-charge-sheet analytic model for an ideal retrograde doping MOSFET structure. The model adopts an approach of solving Poisson's equation for the heavily-doped region and lightly-doped region, respectively, and the analytic expression of potential distribution and the drain current of the retrograde doping MOSFET are ultimately obtained. The analytical model is also compared with numerical simulation results, which demonstrates that the analytic current model is applicable to both the weak and strong inversion operations and to different geometry structures. Therefore, this proposed model provides a foundation to develop a complete non-charge-sheet retrograde doping model involved with advanced physical effects, such as short-channel effect, quantum mechanics effect, et al.

Keywords: Retrograde, Non-Charge-Sheet, Analytic

1 INTRODUCTION

The retrograde doping structure shown in Fig. 1 has been proposed [1] to solve the contradiction between the high doping concentration and the requirement of high mobility in Bulk CMOS. Numerous methods have been proposed for modeling this device, but most of them are based on the empirical and phenomenal description. There are few models totally based on physics except the charge-sheet model [2] which has been developed in 2002.

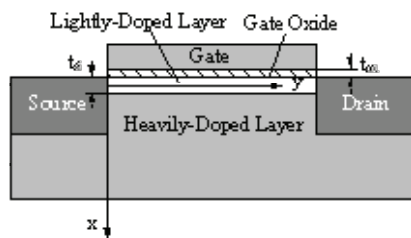


Figure 1: The schematic retrograde-doped device structure.

In this paper, an analytical physics-based model based on non-charge-sheet approach is proposed. The model assumes that the inversion charges are distributed not only

at the interface between channel and oxide layer as usual, but also in the whole substrate. Starting completely from the physical level, the compact expressions of electric potential and current has then been derived. For the practical circuit simulation, the model not only meets the requirements of computational efficiency, but also provides further understanding of non-uniform doping device operation. Furthermore, the model also makes benefits to establish further compact models and research SCE, CV and other physical effects.

2 THEORETICAL DERIVATION

2.1 Derivation of Potential Distribution

A simple doping concentration diagram of retrograde doping device along the vertical direction is shown in Fig. 2. In this figure, x represents the direction of the vertical channel, the starting point is the surface of the lightly-doped semiconductor layer, and t_{si} represents the thickness of lightly-doped region. As shown in Fig. 2, non-uniform substrate has been divided into two uniform regions: lightly-doped and heavily-doped layer. For the sake of simplicity, the lightly-doped layer doping concentration is ignored and similarly an intrinsic layer is considered, while the doping concentration of heavily-doped layer is N_A [1].

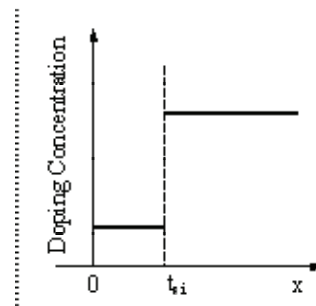


Figure 2: The doping concentration of retrograde doping device along the vertical direction

Holes are ignored because they are only dominant in the accumulation operation. Considering the impact of the junction between the low and high doping substrate regions [3] and the gradual channel approximation, the

one-dimensional Poisson equations in the lightly-doped region and the heavily-doped region of NMOS devices are given by [2-4]:

$$\frac{d^2 \phi}{dx^2} = \frac{qn_i}{\epsilon_{si}} \exp\left(\frac{\phi - \phi_F - V}{v_t}\right) \quad (1)$$

$$\frac{d^2 \phi}{dx^2} = \frac{qN_A}{\epsilon_s} \left[1 + \exp\left(\frac{\phi - 2\phi_F - V}{v_t}\right) \right] \quad (2)$$

where ϵ_s is the silicon dielectric permittivity, n_i is the silicon intrinsic carrier concentration, $v_t = kT/q$ is the thermal potential, $\phi(x)$ is the electrostatic potential, $\phi_F = v_t \ln(N_A/n_i)$ is the Fermi potential in the heavily-doped region, V is the quasi-Fermi potential. Since the current flows predominantly from the source to the drain along the y-direction, the gradient of the electron quasi-Fermi potential is also in the y-direction. This justifies the gradual channel approximation that V is constant in the x-direction.

Eq. (1) can be integrated twice to yield the solutions of potential and electric field in the form of $\sin(h)$ corresponding to the trigonometric function and the hyperbolic function [5]:

$$\phi(x) = V - 2v_t \ln \left[\frac{A}{\beta} \sin(h) \left(\alpha + \frac{\beta x}{t_{si}} \right) \right] \quad (3)$$

$$E(x) = \frac{2v_t \beta}{t_{si}} \cot(h) \left(\alpha + \frac{\beta x}{t_{si}} \right) \quad (4)$$

where $A = t_{si} \sqrt{\frac{qn_i}{2\epsilon_s v_t} \exp\left(-\frac{\phi_F}{v_t}\right)}$, α, β are the

parameters related to the boundary conditions, and ϕ_0 is the potential where the electric field is 0 along with the x-axis.

With Gauss's Law at the gate oxide, the boundary condition of the surface above the lightly-doped region is as follows:

$$\epsilon_{ox} \frac{V_g - \Delta\phi - \phi_s}{t_{ox}} = -\epsilon_s \frac{d\phi}{dx} \Big|_{x=0} = \epsilon_{si} E_s \quad (5)$$

where $\Delta\phi$ is the work-function difference between gate metal and substrate.

Reducing the order of Eq. (2), another boundary condition at the surface under the lightly-doped region is given by:

$$\epsilon_{si} E_b = \sqrt{2q \epsilon_{si} N_A \left(v_t e^{(\phi_0 - 2\phi_F - V)/v_t} + \phi_0 \right)} \quad (6)$$

Then solving the above equations leads to:

$$V_g - \Delta\phi - V + 2v_t \ln \left[\frac{A}{\beta} \sin(h)(\alpha) \right] \quad (7)$$

$$= 2r_f v_t \beta \cot(h)(\alpha)$$

$$\sqrt{V - 2v_t \ln \left[\frac{A}{\beta} \sin(h)(\alpha + \beta) \right]} \quad (8)$$

$$+ v_t e^{-2\phi_F/v_t} \left[\frac{A}{\beta} \sin(h)(\alpha + \beta) \right]^2$$

$$= v_t \beta \sqrt{2r_b} \cot(h)(\alpha + \beta)$$

where the parameter $r_f = \epsilon_{ox}^2 / t_{ox} \epsilon_{ox}$ and $r_b = \epsilon_s / qN_A t_{si}^2$ is adopted for simplification of the equation. Solving Eq. (7) and Eq. (8), the value of α and β is obtained and the potential and electrical field distribution is further attained.

2.2 The Derivation of the Drain Current

Section headings should be 12-point boldface capital letters, centered in the column. Sub-section headings require initial capitals using boldface and left justification. Headings should appear on separate lines, using the Arabic numbering scheme. The abstract and reference section headings are not numbered.

The formulation of the drain current is derived by using potential based method [6-7] which is discussed in this section. Starting from the current continuity equation, the integral expressions of static current in lightly-doped region and the heavily-doped region for the MOS devices are derived as [6-8]:

$$I_{d,L} = \mu \frac{W}{L} \int_{V_s}^{V_d} \int_{\phi_0}^{\phi_s} \frac{qn}{E} d\phi dV \quad (9)$$

$$I_{d,H} = \mu \frac{W}{L} \int_{V_s}^{V_d} \int_0^{\phi_0} \frac{qn}{E} d\phi dV \quad (10)$$

where μ is the mobility of the channel carriers, W/L is the ratio of width to length for the device channel, V_d and V_s are the voltages of the source and drain, respectively.

As the current derivation is started from the potential based method, the Eq. (1) can be integrated out based on the boundary conditions Eq. (5) and Eq. (6) by following the method in [9]. Through a complicated calculation, the current in lightly-doped region is derived:

$$I_{d,L} = -\mu\epsilon_{si} \frac{W}{L} \left\{ \left[\frac{t_{si}}{2} \theta + 2v_t (E_s - E_b) \right] + \frac{C_{ox}}{2\epsilon_{si}} (V_g - \phi_s)^2 + \int_{\phi_0}^{\phi_s} E(\phi_b, V_b) d\phi \right\} \quad (14)$$

Similarly, the current in heavily-doped region is:

$$I_{d,H} = -\mu\epsilon_{si} \frac{W}{L} \left\{ \left[2v_t E_b + 2v_t \frac{qN_A}{\epsilon_{si}} \int_{t_{si}}^{\infty} \left(\frac{\phi}{v_t} - 1 \right) dx \right] - \int_{\phi_0}^{\phi_s} E(\phi_b, V_b) d\phi \right\} \quad (15)$$

The depletion approximation is used to obtain that:

$$\int_{t_{si}}^{\infty} \left(\frac{\phi}{v_t} - 1 \right) dx = \sqrt{\frac{2\epsilon_{si}}{qN_A}} \left(\frac{1}{3v_t} \phi_b^{3/2} - \phi_b^{1/2} \right) \quad (15a)$$

By adding Eq. (14) with Eq. (15), the final expression of the total current is attained:

$$I_d = -\mu\epsilon_{si} \frac{W}{L} \left\{ \left[\frac{t_{si}}{2} \theta + 2v_t E_s + \frac{C_{ox}}{2\epsilon_{si}} (V_g - \phi_s)^2 + 4 \sqrt{\frac{qN_A}{2\epsilon_{si}}} \left(\frac{1}{3} \phi_b^{3/2} - v_t \phi_b^{1/2} \right) \right] \right\} \quad (16)$$

3 RESULTS AND DISCUSSION

In order to verify this analytical model, we have designed a 2-D numerical simulation of long channel with constant mobility by Sentaurus TCAD [10]. Our proposed model, the charge-sheet model [2] and numerical results are compared in this section.

A large transistor with a channel length of $10 \mu m$ has been used. The channel width is $1 \mu m$ and the thickness of oxide layer is $t_{ox} = 3 nm$ while metal gate with mid-gap work-function is adopted. The default doping concentration in heavily-doped area is $N_A = 10^{18} cm^{-3}$ and the thickness of lightly-doped region is $t_{si} = 20 nm$ unless specified in the verification. Then constant mobility has been used and velocity saturation has been neglected in the verification.

Fig. 3 shows the surface potentials versus gate voltage. When the gate voltage is relatively low, the surface

potential under the lightly-doped region increases as the gate voltage increases, which predicts that the depletion approximation of the heavily-doped region used in calculating the current expression is reasonable. The transfer characteristics of the drain current are shown in Fig. 4, Fig. 5 and Fig. 6, and the output characteristics are shown in Fig. 7, Fig. 8 and Fig. 9. We obtain easily from Fig. 8 and 9 that the charge-sheet model stands no longer to match numerical results accurately when N_A declines or t_{si} increases, while our model still matches the numerical results very well. From the analysis of the whole data of these three models in the same test cases discussed in [2], the deviation between charge-sheet model and numerical result reaches 1.5% while the maximum of the one between our model and numerical result is only 0.85%. Furthermore, the simulation process shows that our model is as efficient as the charge-sheet model in calculation. In sum, our model is more accurate than the charge-sheet model and also satisfies the requirement of computing efficiency.

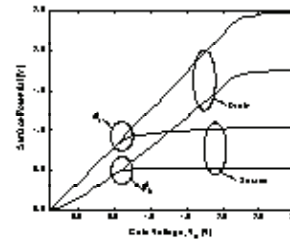


Figure 3: Plot of the surface potentials versus gate voltage

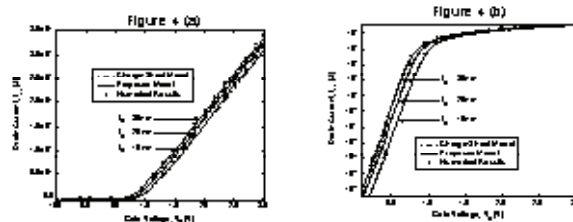


Figure 4: Transfer characteristics of the drain current with different thickness of the lightly-doped region

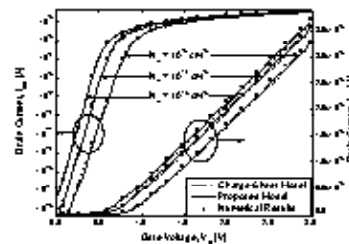


Figure 5: Transfer characteristic of the drain current with different doping levels of the heavily-doped region

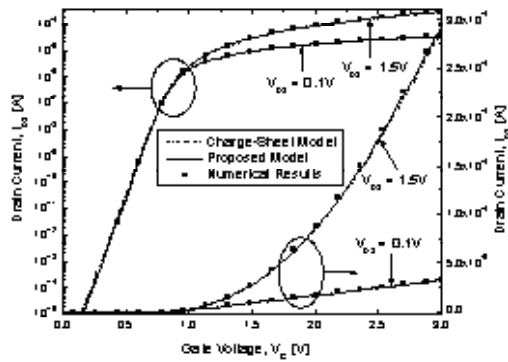


Figure 6: Transfer characteristics of the drain current with different values of Drain-Source Voltage

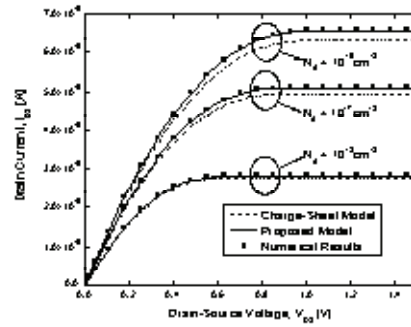


Figure 9: Output characteristics of the drain current with different doping levels of the heavily-doped region

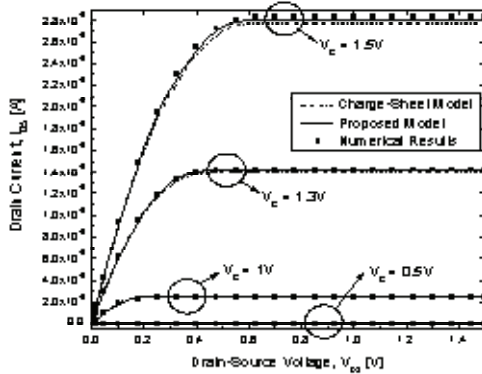


Figure 7: Output characteristics of the drain current with different values of Gate Voltage

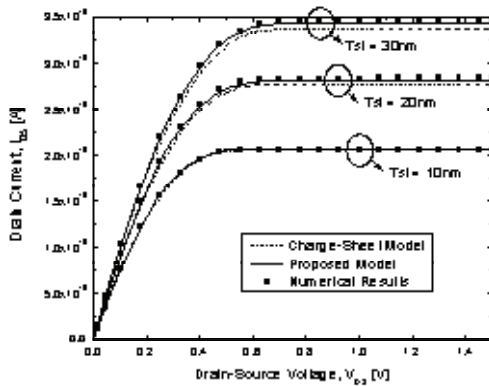


Figure 8: Output characteristics of the drain current with different thickness of the lightly-doped region

4 CONCLUSION

An analytic physics-based model for the ideal retrograde MOSFET is developed and widely verified by the numerical simulation. It is shown that the developed model is more accurate than the charge-sheet model, and thus provides more detail information on the channel potential profile and the drain current prediction.

5 ACKNOWLEDGEMENT

This project is supported by the National Natural Science Foundation of China (Grant No. 60876027 and 60976066) and the National Science Fund for Distinguished Young Scholars of China (Grant No. 60925015).

REFERENCES

- [1] M. Aoki, T. Ishii, T. Yoshimura, Y. Kiyota, S. Iijima, T. Yamanaka, T. Kure, K. Ohyu, T. Nishida, S. Okazaki, K. Seki, and K. Shimohigashi, *IEEE Trans. Electron Devices*, 13, 50, 1992.
- [2] S. Persson, P. E. Hellberg and S. L. Zhang, *Solid-State Electronics*, 46, 2209, 2002.
- [3] Z. T. Kuznicki, *J. Appl. Phys.* 69, 6526, 1991.
- [4] Yuan Taur, *IEEE Electron Device Letters*, 21, 245, 2000.
- [5] Huaxin Lu, and Yuan Taur, *IEEE Trans. Electron Devices*, 53, 1161, 2006.
- [6] R. F. Pierret, and J. A. Shields, *Solid-State Electronics*, 26, 143, 1983.
- [7] A. Ortiz-Conde, R. Herrera, P. E. Schmidt, F. J. Garcia Sanchez, and J. Andrian, *Solid-State Electronics*, 35, 1291, 1992.
- [8] H. C. Pao and C. T. Sah, *Solid-State Electronics*, 9, 927, 1966.
- [9] Jeffrey W. S., and Rafael Rios, *IEEE Trans. Electron Devices*, 45, 821, 1998.
- [10] TCAD Sentaurus Device User's Manual, Synopsys, Mountain View, CA, 2005