Source/Drain Edge Modeling for DG MOSFET Compact Model

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ABSTRACT

A compact model for four terminal double-gate MOSFET, based on double charge-sheet approximation with carrier-velocity saturation is discussed. The model describes the channel consisting of two regions, the drift-diffusion region and constant-velocity drift-only region. In this paper we discuss on the remaining space-charge regions which is present at the source/drain edge of the undoped channel. In particular the modeling of the region for gate underlap devices, which will be introduced to alleviate GIDL, is discussed in detail.

Keywords: Compact model, MOSFET, Double-gate.

1 INTRODUCTION

We have developed a compact model for four terminal double-gate MOSFET [1], based on double charge-sheet approximation with carrier velocity saturation. The model describes the channel consisting of two regions. The source-side region is the drift-diffusion region with carrier-velocity saturation characteristics. The second region, which is introduced at the drain-side when the transistor behavior approaches saturation, is the constant-velocity drift-only region. The boundary point of these two regions remotely corresponds to the pinch-off point. The introduction of the latter region provides, for the first time, crude but consistent profile of the surface potential, the quasi-Fermi level and the carrier-density almost throughout the channel. This thus achieved a monolithic model both for conductance and intrinsic capacitances [2].

This model is not, however, a complete analytical model across the entire channel: space charge regions at the source/drain edge have not been modeled. For conventional bulk transistors, this region is realized as the space charge layer of the p-n junction at the source/channel boundary and at the drain/channel boundary. In the case of DG MOSFET, where the channel region is often lightly doped or undoped, it is realized as a space charge layer at the n-i junction. As far as the gate is exactly aligned or overlapped to the channel, such space-charge regions only slightly increase effective gate-overlap length. On the other hand, gate underlap at the drain, i.e. the drain space-charge region outside the gate, is preferable to alleviate the GIDL (Gate Induced Drain Leakage) effect, since the effect may trigger much larger drain current by the parasitic floating-base bipolar transistor. If the device is constructed such that the source and the drain are geometrically symmetric, the drain-side underlap accompanies the source-side underlap. In this report, we discuss the modeling of these regions, and their effect on the effective gate length, and on the conductance modulation caused by it.

2 SPACE CHARGES AT THE EDGE

We consider the double gate structure as shown in Fig. 1, where full cross-section of (a) the gates which exactly align to the source/drain doing edge, and upper-half cross-sections of (b) overlapped gates, and (c) underlapped gates are illustrated.

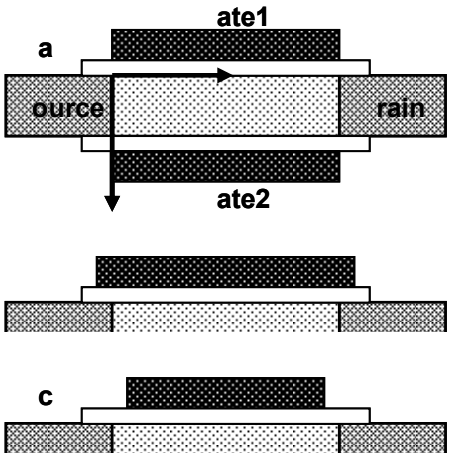


Figure 1.Double-gate transistor with (a) the exactly aligned, (b) overlapped, and (c) underlapped gates.

For a transistor with exactly aligned gates, typical profile of the surface potential and the carrier concentration at the surface is shown in Fig. 2. The transistor has 100nm exactly aligned gates, the silicon channel 10nm thick, and gate oxides 2nm thick. At the boundary between the channel and the source/drain, there are thin (around 4-5nm) transition layers, where carrier concentration is much larger than that expected by gradual channel approximation. At the source/channel boundary, the channel current is given by the diffusion current which overwhelms the drift current of the reverse direction. At the drain/channel boundary, the overwhelming drift current is largely compensated by the diffusion current of the reverse direction.

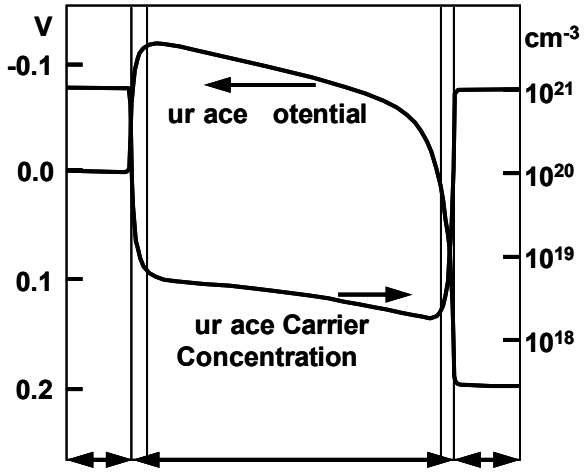


Figure 2. ATLAS simulation result of the surface potential and the surface carrier concentration of a double-gate transistor. The gate voltage is 0V and the drain voltage is 200mV.

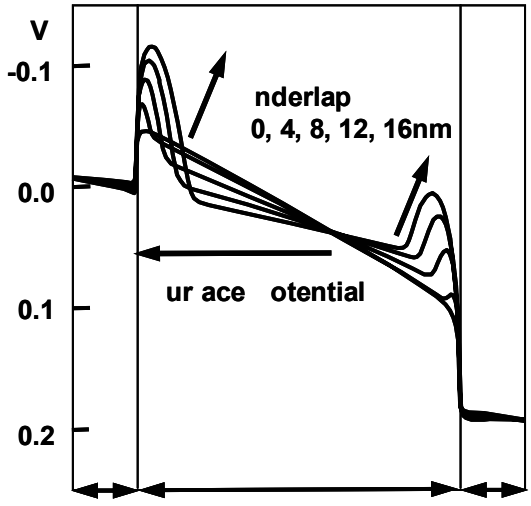


Figure 3. ATLAS simulation result of the surface potential when the underlap (4, ...16nm, both at source and at drain) is introduced to the device in Fig.2. The gate voltage is 600mV and the drain voltage is 200mV.

Such a characteristic is inherent to the space charge region adjacent to the abrupt n-i junction. Since the total layer-thickness of the transition region is small, the channel length modulation by them will be obliterated by doping edge uncertainly.

When the underlap is introduced to the device, situation changes drastically. One example is depicted in Fig. 3, where gate underlap up to 16 nm is introduced to the device shown in Fig. 2. The gate voltage of 600mV is applied while the drain voltage is kept to 200mV; a condition where both the source underlap and the drain underlap affect the drain current. Development of the potential hump at both source/drain edges, as the underlap increases, is clearly seen.

When the drain voltage is changed, the behavior of these two humps differ each other, as in Fig.4, where ATLAS simulation for the device with the 16nm source/drain underlaps are shown by changing the drain voltage from 0.2 to 1V. The height of the source hump slightly decreases for a small drain voltage, while the drain hump diminishes as the drain voltage is increased.

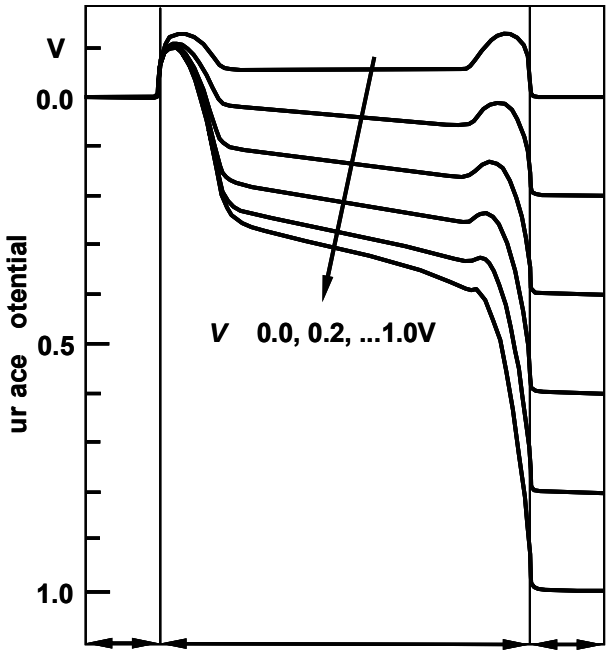
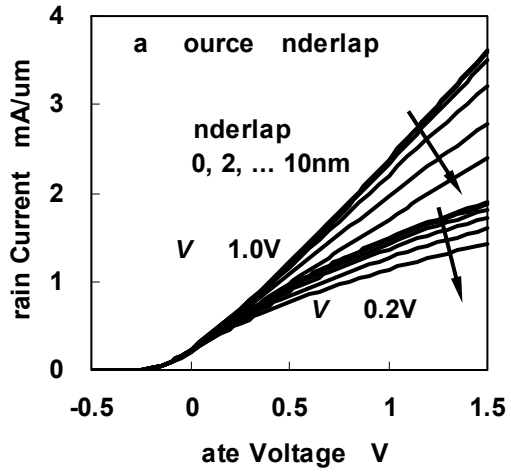


Figure 4. ATLAS simulation result of the surface potential for a device of 16nm source/drain underlap. The gate voltage is fixed to 600mV.

3 DRAIN CURRENT MODULATION

The humps cause the drain current decrease. In Fig. 5, the drain-current change caused by the underlap is shown. To separate the effects of source/drain underlaps, simulation is performed using device structures of only source-underlap or drain-underlap is present. The figure 5(a) shows the case for the source underlapped device, while the figure 5(b) shows the case for the drain

underlapped device. When the drain voltage is small, both the source/drain underlaps results in similar drain current decrease. On the other hand, when the drain voltage is large, the source underlap causes sharp decrease in drain current, while the current decrease by the drain underlap vanishes. This difference in the behavior of source/drain underlap is consistent with the behavior of the humps.



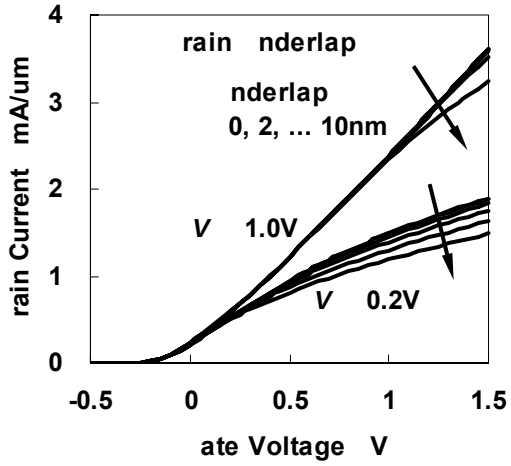


Figure 5. ATLAS simulation result of the drain current when (a) the source underlap and (b) the drain underlap is introduced. The device structure is the same to the previous ones.

It is not easy to extract any empirical relationship from data shown above. One interesting feature concerning to the source underlap is shown in Fig. 6, where correlation between the drain currents of the exactly aligned device and the source underlapped device under various operating condition is shown. There are four bunches of lines in the figure, where each bunch corresponds a device with source underlap of 4, 8, 12 and 16 nm. In each bunch, there are 8 lines corresponding to the gate voltage V_G=0.6, 0.8, ... 2.0V. And each line is obtained by changing the drain voltage from 0.05 to 1V.

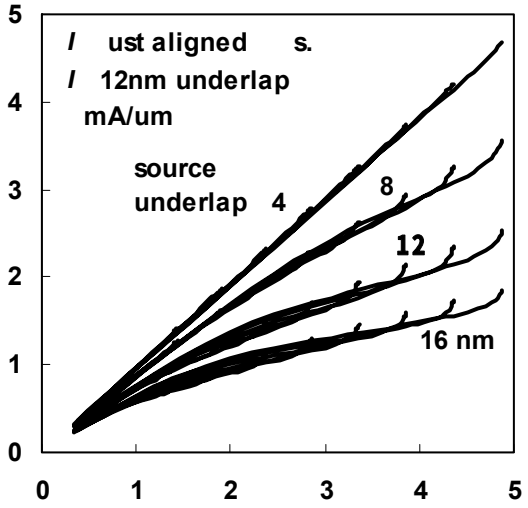


Figure 6. Correlation between drain currents of gate just-aligned devices and source-underlapped devices.

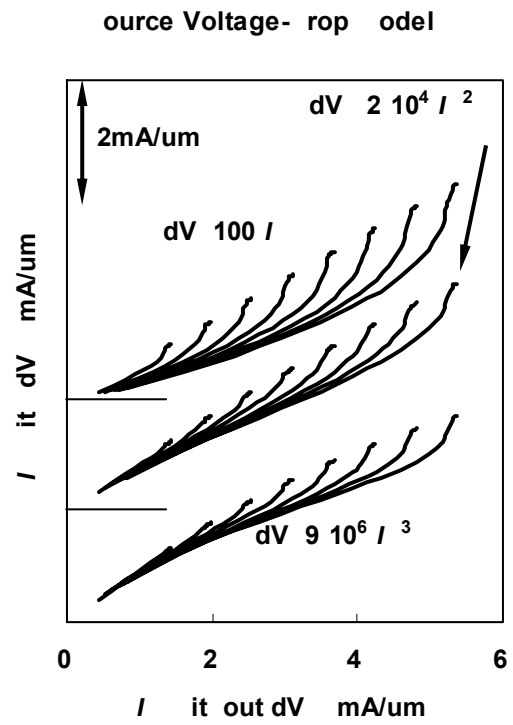


Figure 7. Correlation between drain currents, of gate just-aligned devices and source-underlapped devices, for a model where a linear or a non-linear diode is inserted at the source node.

Most prominent feature is that, regardless to the gate voltage and the drain voltage applied, there is strong relation between the drain currents of the exactly-aligned device and source-underlapped devices. The relation is largely nonlinear.

If we construct the compact model by using this feature, an easy way is to first calculate the drain current of the exactly-aligned device, and, consulting the relation obtained from Fig. 6, multiply it a factor to obtain the drain current of the underlapped device. This approach is, however by no means "physics based." Still more, this approach is not applicable to drain-edge underlap, since the current decrease vanishes when sufficiently large drain voltage is applied, resulting in two independent models.

Another possible approach to model the device is to introduce "effective channel length," which varies as the gate voltage and the drain voltage are changed. As is implied in Fig. 5, the effective channel length is, in all cases, longer than the real gate length. This approach is again, not physics based, because the resultant additional gate length is often much longer the underlap value, and even longer than physically acceptable value.

A general way to construct the model is to insert a diode of any nonlinear characteristics between the source resistor and the channel. Fig. 7 shows the result by inserting a linear or a non-linear resistor. The plotting style is the same to that in Fig. 6. It can clearly be seen that the relationship between two drain currents are quite different observed in Fig. 6, and it also strongly suggests that any type of nonlinear diode cannot fulfill the condition.

We also tried to model the underlapped area as a thermal carrier emitter; an emitter of room temperature and an emitter of elevated temperature. In both cases the result was not satisfactory.

4 SUMMARY

We have discussed the effect on the current transport by the gate underlap configuration for double-gate MOSFETs. By using ATLAS device simulator, profile change in the surface potentials and in the drain current, caused by the introduction of the gate underlap, have been investigated. A large potential hump by the source unterlap, which is persistent even at the higher drain voltage, and a diminishing potential hump by the drain underlap have been shown. The behavior of the drain current has found to be consistent with the change in the hump height.

The drain current for the underlapped devices have been primarily a nonlinear function of the drain current of the corresponding exactly-aligned device, regardless to the gateand drain voltage.

No diode model attached in series at the source node has been found to be satisfactory to model this behavior.

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