A Unified Charge-Based Model for SOI MOSFETs Valid from Intrinsic to Heavily Doped Channel

Jian Zhang[*,**], Jin He[*,**,***], Lining Zhang[**], Xingye Zhou[**], and Zhize Zhou[*]

[*] The Key Laboratory of Integrated Microsystems, School of Computer & Information Engineering, Peking University Shenzhen Graduate School, Shenzhen 518055, P. R. China

[**] TSRC, Institute of Microelectronics, School of Electronic Engineering and Computer Science, Peking University, Beijing 100871, P. R. China, hejin@szpku.edu.cn

[***] Peking University Shenzhen SOC Key Laboratory, PKU HKUST Shenzhen Institute, W303, West Tower, IER Bldg., Hi-Tech Industrial Park South, Shenzhen 518057, P. R. China

ABSTRACT

A unified charge-based model for SOI MOSFETs is presented. The proposed model is valid and accurate from intrinsic to heavily doped channel with various structure parameter variations. The framework starts from one-dimension Poisson-Boltzmann's equation. Based on the full depletion approximation, an accurate inversion charge density equation is obtained. With the inversion charge density solution, the unified drain current expression is derived. And the unified terminal charge and intrinsic capacitance model is also derived under quasi-static case. The validity and accuracy of presented analytic model is proved by extensive verification with numerical simulation.

Keywords: charge-based, SOI MOSFET, compact model, double gate.

1 INTRODUCTION

With the continuous scaling down, SOI MOSFET has become a mainstream technology for high-performance and low-power application due to the advantages of the unique SOI structure, such as great isolation and latch-up free. In addition, the fully depleted device has high drive current, suppression of floating body effect and low junction tunneling current [1-2]. Especially for the nanoscale device and IC design, the ultra-thin-body (UTB) SOI MOSFETs with the fully depleted body show the potential superior scalability relative to the partially depleted and the bulk CMOS counterparts [2].

In order to realize these advantages for integrated circuit design, there has been much research work on compact modeling for fully depleted SOI MOSFETs [3-7]. The charge-based models that formulate the terminal charges and drain current with the inversion charge density have potentials in analog and RF CMOS simulation application [5-7]. A charge-based model for fully depleted SOI MOSFETs has been early presented and describes the different operating regimes respectively [5]. In recent works, a unified charge control model is derived for fully depleted structure for the first time [6,7]. This model deal with highly doped and undoped devices with different expressions and the variation of the buried oxide thickness is also neglected by assuming it equal to the front-gate oxide thickness. Thus a unified model considering various structure parameter variations is still lacking for the circuit design applications with fully depleted devices.

In this paper, a unified charge-based model for fully depleted SOI MOSFETs is presented, which is valid and accurate for both intrinsic and heavily doped devices with various structure parameter variations. An accurate inversion charge density equation is obtained. A unified drain current expression is derived which is physically continuous between subthreshold and strong inversion regions. The unified terminal charge and intrinsic capacitance model is also derived under quasi-static case as an explicit function of the inversion charge solution at terminals. The validity and accuracy of presented analytic model is proved by extensive verification with numerical simulation. The large application scope of various structure parameters not only proves the practicability of the long-channel model as the basis for development of improved models for actual devices, but also gives an instructive reference to the compact modeling of symmetric and independent double gate MOSFET which based on the same oxide-silicon-oxide structure.

2 UNIFIED DRAIN CURRENT MODEL

The analyzed device is a typical four-terminal n-channel SOI MOSFET illustrated in Fig.1. The doping concentration of the substrate is assumed high enough and the voltage drop on the substrate is neglected.

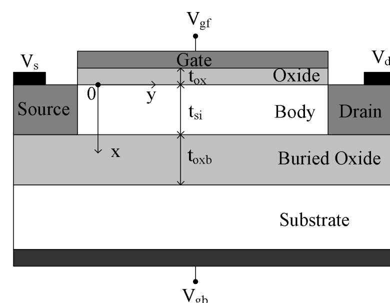

Fig.1. Schematic diagram of the fully depleted MOSFET.

Under the gradual-channel approximation, 1-D Poisson-Boltzmann's equation is written as

$$\frac{d^2\phi}{dx^2}=\frac{qN_A}{\varepsilon_{si}}\left[1+\exp\left(\frac{\phi-2\phi_F-V_{ch}}{V_t}\right)\right] \tag{1}$$

Integral the Poisson-Boltzmann's equation, thus

$$\varepsilon_{si}^{\,2}\left(E_s^{\,2}-E_0^{\,2}\right)=2qN_A\varepsilon_{si}\left[\begin{array}{l}(\phi_s-\phi_0)+\\ V_t\exp\left(\frac{\phi_s-2\phi_F-V_{ch}}{V_t}\right)\left(1-\exp\left(\frac{\phi_0-\phi_s}{V_t}\right)\right)\end{array}\right] \tag{2}$$

To obtain the relationship between the potentials at the interfaces between silicon and oxides, depletion approximation is used [3],

$$\phi_s-\phi_0=\frac{qN_At_{si}^{\,2}}{2\varepsilon_{si}}+E_0t_{si}\triangleq V_B+E_0t_{si} \tag{3}$$

Substituting (3) into (2), and combining it with Gauss's law, yields the logarithm of the normalized expression,

$$q_{inv}+\ln q_{inv}+\ln\left(1+Hq_{inv}\right)=v_1-q_{dep}-2\varphi_f-v_{ch}+\ln\left[\frac{C_{si}q_{dep}}{\left(C_{ox}+C_1\right)q_1}\right] \tag{4}$$

The charge and voltage terms in (4) are normalized by $q_0=\left(C_{ox}+C_1\right)V_t$ and V_t, respectively.

In Eq.(4),

$C_1=\frac{C_{oxb}C_{si}}{C_{oxb}+C_{si}}$, $q_1=\frac{1}{q_0}\frac{C_{ox}}{C_{ox}+C_1}\left[\frac{Q_{dep}}{\beta}+C_1\left(V_{GF}-V_B-V_{GB}\right)\right]$,

$H=\frac{C_{ox}-C_1}{C_{ox}+C_1}\frac{1}{2q_1}$, and $v_1=\frac{1}{V_t}\frac{C_{ox}V_{GF}+C_1\left(V_B+V_{GB}\right)}{C_{ox}+C_1}$ with $\beta=1-\exp\left(-2v_b\right)$ for the accurate modeling from intrinsic to heavy channel doping concentration [6-9].

The normalized drain current is derived as

$$i_{ds}=\int_0^{V_{ds}}q_{inv}dv_{ch}=-\left[\frac{q_{inv}^{\,2}}{2}+2q_{inv}-\frac{1}{H}\ln\left(1+Hq_{inv}\right)\right]_{q_s}^{q_d} \tag{5}$$

where q_d, q_s are the normalized inversion charge density at the source (V_{ch}=V_s) and drain (V_{ch}=V_d) ends, respectively, which is calculated from the inversion charge density equation (4).

To verify the proposed analytical model, a long-channel SOI MOSFET with constant mobility is designed for the two-dimension numerical simulation [10]. The doping concentration of the substrate silicon film is 1e18cm^{-3}, constant electron mobility 350cm^2/Vs and metal gate with mid-gap work-function are used, the width of the channel is 1μm, and to avoid the short channel effects and prove the validity of the long channel theory, the channel length of 5μm is used.

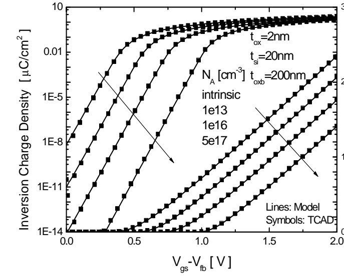

Fig.2. Inversion charge density as a function of gate voltage for different doping concentrations.

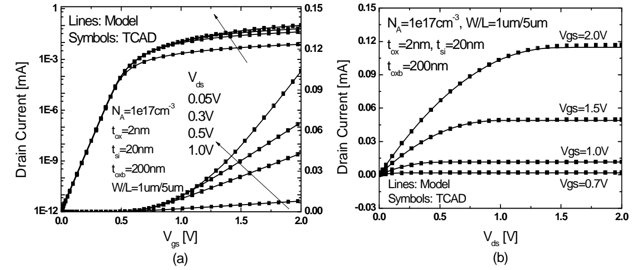

Fig.3. Drain current calculated from the unified current model and numerical simulation.
(a) Transfer characteristic; (b) Output characteristic.

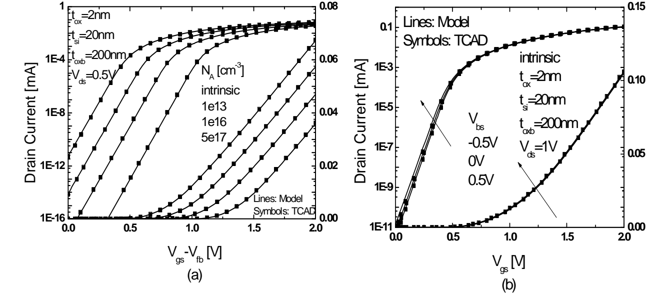

Fig.4. Transfer characteristics of devices with
(a) different doping levels; (b) different back gate bias.

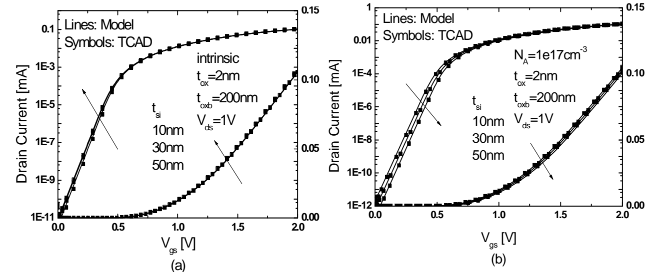

Fig.5. Transfer characteristics of devices with different silicon film thickness. (a) Device with intrinsic channel; (b) Device with heavily doped channel.

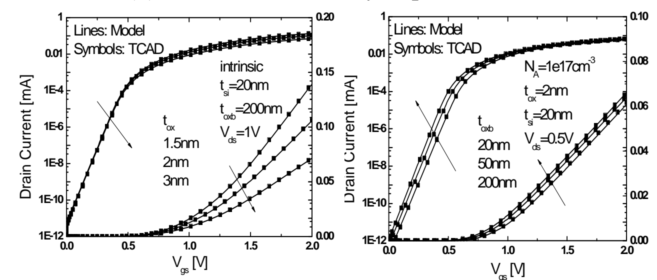

Fig.6. Transfer characteristics of devices with different (a) gate oxide thickness, (b) buried oxide thickness.

Fig.2 compares the inversion charge density in the silicon film as a function of gate voltage under V_{ds}=0 for different channel doping concentrations. Fig.3 plots the drain current predicted by the unified current model and the numerical simulation results. In the absence of QME and PSE, the application scope of various structure parameters for the model is widely verified.

Figs.4-6 illustrate the drain currents with different structure parameters as channel doping levels, back gate bias, silicon film thickness, gate oxide thickness, and buried oxide thickness. Fig.4(a) shows the drain current calculated from the model compared with the numerical results from intrinsic to heavily doped condition. The transfer characteristics of devices with different back gate bias is also obtained in Fig.4(b). Fig.5 shows the impact of different silicon thickness on the drain current for both intrinsic and heavily doped channels. The volume inversion is observed for lightly doped device, where the subthreshold leakage is linearly proportional to t_{si} [11]. This unique characteristic is accurately accounted for with the unified current model. Fig.6 illustrates accurate modeling of the devices with different oxide thickness. These results prove the predicting ability for the electric fields at the interfaces, which is important for the characteristic prediction of the oxide-silicon-oxide structure, such as the suppression of short-channel-effects and mobility degradation. The large application scope of various structure parameters not only proves the validity and practicability of the proposed model, but also gives a reference to the compact modeling of symmetric and independent double gate MOSFET.

3 TERMINAL CHARGE AND CAPACITANCE MODEL

In the fully depleted device, the four principal charges are described as

$$Q_{GF} = W\int_0^L C_{ox}\left(V_{GF}-\phi_s\right)dy \tag{6a}$$

$$Q_{GB} = W\int_0^L C_{oxb}\left(V_{GB}-\phi_0\right)dy \tag{6b}$$

$$Q_N = -Wq_0\int_0^L q_{inv}dy \tag{6c}$$

$$Q_B = -WLq_0 q_{dep} \tag{6d}$$

Combining (6c) with (4) and the current continuity, performing the above integral gives that [12]

$$Q_N = WLq_0\frac{M(q_{inv})\big|_{q_s}^{q_d}}{i_{ds}} \tag{7a}$$

$$M(q_{inv}) = \frac{q_{inv}^3}{3}+q_{inv}^2-\frac{q_{inv}}{H}+\frac{1}{H^2}\ln[1+Hq_{inv}] \tag{7b}$$

From the Poisson-Boltzmann's equation (1) and Gauss's law, the integral in (6b) is performed using the same method in the derivation of (7) as

$$Q_{GB} = -WLq_0\left(q_2-\frac{C_1}{C_{ox}+C_1}q_{dep}-\frac{C_1}{C_{ox}+C_1}\frac{M(q_{inv})\big|_{q_s}^{q_d}}{i_{ds}}\right) \tag{8}$$

Where $q_2 = \dfrac{1}{q_0}\dfrac{C_1C_{ox}\left(V_{GF}-V_B-V_{GB}\right)}{\left(C_{ox}+C_1\right)}$.

Thus, the other charge is also obtained from the neutrality condition yields that

$$Q_{GF} = WLq_0\left(q_2+\frac{C_{ox}}{C_{ox}+C_1}q_{dep}+\frac{C_{ox}}{C_{ox}+C_1}\frac{M(q_{inv})\big|_{q_s}^{q_d}}{i_{ds}}\right) \tag{9}$$

The channel inversion charge Q_N is partitioned between drain and source according to Ward and Dutton's charge partition model [13], and the drain terminal charge is expressed as

$$Q_D = -Wq_0\int_0^L \frac{y}{L}q_{inv}dy \tag{10}$$

Combining the current continuity with the drain current expression (5) under quasi-static case, the relationship between y and q_{inv} is derived as

$$y = \frac{L}{i_{ds}}\left\{2(q_s-q_{inv})+\frac{(q_s^2-q_{inv}^2)}{2}+\frac{1}{H}\ln[\frac{1+H\cdot q_{inv}}{1+H\cdot q_s}]\right\} \tag{11}$$

After complicated calculation, the drain terminal charge is finally obtained as

$$Q_D = -WLq_0\frac{\left[M(q_{inv})F(q_s)+N(q_{inv})\right]\big|_{q_s}^{q_d}}{{i_{ds}}^2} \tag{12a}$$

$$\begin{aligned}N(q_{inv}) &= \left[-\frac{q_{inv}^5}{10}-\frac{3}{4}q_{inv}^4-\frac{2q_{inv}^3}{3}\right]+\frac{1}{H^2}\left[-\frac{q_{inv}^2}{12}-q_{inv}\ln(1+Hq_{inv})\right]\\&+\frac{1}{H}\left[q_{inv}^2\ln(1+Hq_{inv})+\frac{q_{inv}^2}{2}+\frac{q_{inv}^3}{3}\ln(1+Hq_{inv})+\frac{q_{inv}^3}{18}\right]\\&+\frac{1}{H^3}\left[\frac{1}{6}q_{inv}+\ln(1+Hq_{inv})\right]+\frac{1}{H^4}\left[-\frac{1}{6}\ln(1+Hq_{inv})\right]\end{aligned} \tag{12b}$$

And the source terminal charge is obtained similarly as

$$Q_S = -WLq_0\frac{\left[M(q_{inv})F(q_d)+N(q_{inv})\right]\big|_{q_d}^{q_s}}{{i_{ds}}^2} \tag{13}$$

As a four terminal device, SOI MOSFET has 16 capacitances. Among them, only 9 capacitances are independent. These capacitances are defined as

$$C_{ij} = \begin{cases}-\dfrac{\partial Q_i}{\partial V_j} & i\neq j\\[2ex] \dfrac{\partial Q_i}{\partial V_j} & i=j\end{cases}\qquad i,j=GF,GB,S,D \tag{14}$$

With the terminal charge expressions, the above partial derivatives and the capacitance matrix are easily obtained for fully depleted SOI MOSFETs. All the capacitances are explicit functions of the inversion charge density at source and drain ends.

Fig.7 plots the normalized capacitances calculated from the unified capacitance model and compared with numerical simulation results. Fig.7(a) gives the capacitances versus gate voltage. The trans-capacitances (C_{gd}, C_{dg}), (C_{gs}, C_{sg}) and (C_{sd}, C_{ds}) are all different, conforming the nonreciprocal characteristics [12]. Fig.7(b) plots the capacitances versus drain voltage. Good agreements between the proposed model and the TCAD results are observed. The symmetry of the trans-capacitances, e.g. C_{gs}=C_{gd} when V_{ds}=0 is also accurately predicted by the proposed capacitance model.

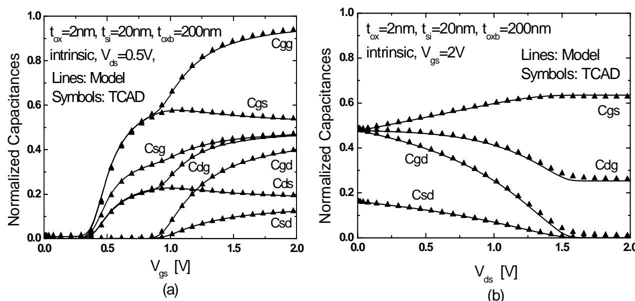

Fig.7 Normalized independent capacitances of fully depleted SOI MOSFET (a) Capacitances versus gate voltage (b) Capacitances versus drain voltage.

4 CONCLUSIONS

In this paper, a unified charge-based model for SOI MOSFETs is presented. An accurate inversion charge density equation is obtained based on the full depletion approximation. With this inversion charge density solution, the unified drain current expression is derived. The quasi-static terminal charge and intrinsic capacitance is also derived. This work gives an accurately compact model for the device with both intrinsic and heavily doped channel. Extensive verification with numerical simulation for various structure parameter variations proves the accuracy and practicability of the proposed model. For the devices which based on the same oxide-silicon-oxide structure, such as symmetric and independent double gate MOSFET, this presented result also gives an instructive reference to those compact modeling.

ACKNOWLEDGEMENT

This project is supported by the National Natural Science Foundation of China (Grant No. 60876027 and 60976066) and the National Science Fund for Distinguished Young Scholars of China (Grant No. 60925015).

REFERENCES

[1] J.-P. Colinge, “Novel gate concepts for MOS devices,” in Proc .ESSDERC 2004, pp. 45–49. Sep. 2004.

[2] V. P. Trivedi, and J. G. Fossum, “Scaling fully depleted SOI CMOS,” IEEE Trans. Electron Devices, vol. 50, no. 10, pp. 2095–2103, Oct. 2003.

[3] J. W. Sleight, and Rafael Rios, “A Continuous Compact MOSFET Model for Fully- and Partially-Depleted SOI Devices,” IEEE Trans. Electron Devices, vol. 45, no. 4, pp. 821-825, 1998.

[4] Xing Zhou, K. Chandrasekaran, S. B. Chiah, W. Shangguan, Z. Zhu, G. H. See, S. M. Pandey, G. H. Lim, S. Rustagi, M. Cheng, S. Chu, and L-C. Hsia, “Unified approach to bulk/SOI/UTB/s-DG MOSFET compact modeling,” NSTI-Nanotech, vol. 3, pp. 652-657, 2006.

[5] P. C. Yeh and J. G. Fossum, "Physical subthreshold MOSFET modeling applied to viable design of deep-submicrometer fully depleted SOI low-voltage CMOS technology," IEEE Trans. Electron Devices, Vol. 42, pp. 1605-1613, Sep. 1995.

[6] O. Moldovan, A. Cerdeira, D. Jiménez, J. P. Raskin, V. Kilchytska, D. Flandre, N. Collaert and B. Iñiguez, “Compact model for highly-doped double-gate SOI MOSFETs targeting baseband analog applications”, Solid-State Electronics, vol. 51, no. 5, pp. 655-661, 2007.

[7] O. Moldovan, F. A. Chaves, D. Jiménez, and B. Iñiguez, “Compact charge and capacitance modeling of undoped ultra-thin body (UTB) SOI MOSFETs”, Solid-State Electronics, vol. 52, pp. 1867-1871, 2008.

[8] F. Liu, J. He, L. Zhang, J. Zhang, J. Hu, C. Ma, and Mansun Chan, “A Charge-Based Model for Long-Channel Cylindrical Surrounding-Gate MOSFETs From Intrinsic Channel to Heavily Doped Body,” IEEE Trans. Electron Devices, vol. 55, no. 8, pp. 2187–2193, Aug. 2008.

[9] A. S. Roy, J.-M. Sallese, and C. C. Enz, “A closed-form charge-based expression for drain–current in symmetric and asymmetric double gate MOSFET,” Solid State Electron., vol. 50, no. 4, pp. 687–693, Apr. 2006.

[10] TCAD Sentaurus Device User’s Manual, Synopsys, Mountain View, CA, 2005.

[11] V. P. Trivedi, J. G. Fossum, W. Zhang, “Threshold voltage and bulk inversion effects in nonclassical CMOS devices with undoped ultra-thin bodies,” Solid-State Electronics, Vol. 51, pp. 170-178, Jan. 2007.

[12] Feilong Liu, Jian Zhang, F. He, Feng Liu, L. Zhang and Mansun Chan, “A charge-based compact model for predicting the current–voltage and capacitance–voltage characteristics of heavily doped cylindrical surrounding-gate MOSFETs,” Solid-State Electronics, vol. 53, no. 1, pp. 49–53, Jan. 2009.

[13] D. Ward and R. Dutton, “A charge-oriented model for MOS transistor capacitances,” IEEE J. Solid State Circuits, vol.13, no. 5, pp. 703-708, Oct. 1978.