Linearity Performance Assessment of Nanoscale Gate Material Engineered Trapezoidal Recessed Channel (GME-TRC) MOSFET for RFIC design and Wireless application

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ABSTRACT

In this work, an extended study of linearity behaviour of proposed Gate Material Engineered-Trapezoidal Recessed Channel(GME-TRC) MOSFET has been performed using ATLAS and DEVEDIT device simulators and the results so obtained are compared with Trapezoidal Recessed Channel(TRC) MOSFET. Simulation results reveal that GME-TRC MOSFET enhances the linearity performance in terms of figure of merit (FOM) metrics:VIP2, VIP3 and higher order transconductance coefficients: gm1, gm2, gm3, proving its efficacy for RFIC design and wireless application.

Keywords: ATLAS-3D, DEVEDIT-3D, GME, RF, SCEs.

1 INTRODUCTION

Linearity has been an important figure of merit (FOM) in all RF and wireless applications to guarantee minimum signal distortion in modern communication systems [1,2]. Recent developments in sub-100nm CMOS technology results in great interest in system on chip (SOC) applications based on all CMOS technologies due to their inherent low cost and high density. However, as the miniaturization of device proceeds, control of short channel effects (SCEs) is one of the biggest challenges in future downscaling technologies. Recessed MOSFETs can be consider as a promising candidate to mitigate many of the SCEs and hot-carrier effects [3-5]. In case of recessed channel MOSFETs, potential barriers are formed at the two corners which results in decreasing of many SCEs but on the other side it also decreases the current driving efficiency of the device. The recessed channel MOSFET, however, in conjunction with gate material engineered (GME) architecture [8–10], enhances drain current characteristics, average carrier velocity and suppresses SCEs, thereby proving superior to the conventional recessed channel MOSFET. With GME architecture, the step potential profile, due to different work functions of two metal gates, ensures reduction of SCEs and screening of the channel region under metal M1 from drain potential variations. Thus, the average electric field in the channel is enhanced, improving the electron velocity near the source and, hence, the carrier transport efficiency, thereby improving the linearity performance of the device. The GME-TRC MOSFET [6,7] considered in this study integrates the potential benefits of recessed MOSFETs with GME architecture for enhancing the linearity performance of scaled devices in comparison to single material gate TRC MOSFET design.

2 RESULT AND DISCUSSION

In this paper, the RF performance for Gate Material Engineered-Trapezoidal Recessed Channel (GME-TRC) MOSFET(Fig.1.) has been investigated and the results so obtained are compared with Trapezoidal Recessed Channel (TRC) MOSFET(Fig.1.), using device simulators; ATLAS and DEVEDIT. The result offers the opportunity for realizing the reliability of GME-TRC MOSFET for high speed logic and RF applications.

Fig. 2, 3 and 4 shows the significant enhancement of higher order transconductance coefficients: gm1, gm2 and gm3, respectively, for GME-TRC MOSFET as compared to its conventional counter part TRC MOSFET. In GME-TRC MOSFET, a perceivable step in the surface potential profile due to different metal gate work functions, i.e. Φ_{M1} and Φ_{M2}, results in enhancement of device performance in terms of improved gate control, driving current capabilities, linear behavior; reduced hot carrier effects and harmonic distortion, thereby enhancing gm1, gm2, gm3 in comparison with TRC MOSFET, as shown in Fig.2, 3 and 4 respectively. Moreover, harmonics in MOS devices is mainly present due to the nonlinearity exhibited by higher-order derivatives of I_{ds}–V_{gs} characteristics, thus the amplitude of gm3 should be minimum since it determines a lower limit on the distortion. The zero-crossover point of gm3 determines the DC bias point for optimum device operation and hence, the non-linear behaviour of gm3 can be minimized by setting DC bias close to gm3 zero-crossover point. For GME-TRC MOSFET bias point moves towards the lower V_{gs}, as shown in Fig.4., thereby showing the lesser harmonic distortion as compared to TRC MOSFET.

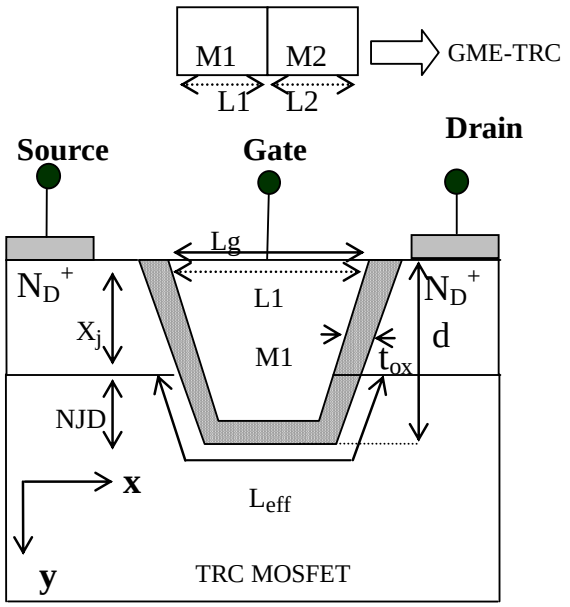

Fig.1. Schematic structure of GME-TRC and TRC MOSFET. The effective channel length L_{eff} corresponds here to the metallurgical channel length, taken along the gate oxide, i.e. L_{eff}= (2 x Ls) + Lp, where, Lp = 38nm, is the planar part and Ls = 32nm, is the angular part of the channel.Groove Depth (d)=76nm, NJD=32nm, N_A =1x10^{17} cm^{-3}, N_D=1x10^{20} cm^{-3}, t_{ox}=4nm, ε_{ox}=3.9. Work function (ϕ_{M1})=4.77V and channel length, Lg= L1 = 30nm for TRC MOSFET and for GME-TRC MOSFET, (ϕ_{M1})=4.77V and (ϕ_{M2}) = 4.10V and and channel length Lg= L1 + L2 = 30nm . All these parameters are same in all figures unless stated otherwise.

The decrease in NJD, i.e. increase in source/drain junction depth (X_j), shifts the bias point towards the left, thereby further reducing the harmonic distortion, as shown in Fig.4., due to the decrease in potential barriers formed at the corners in recessed channel MOSFET which limits the driving capabilities of the device. Moreover, increasing workfunction difference and decreasing substrate doping can further suppress the harmonic distortion and non linear behavior of the device due to the improved gate control and transconductance for GME-TRC MOSFET, as shown in Fig.2, 3 and 4 respectively.

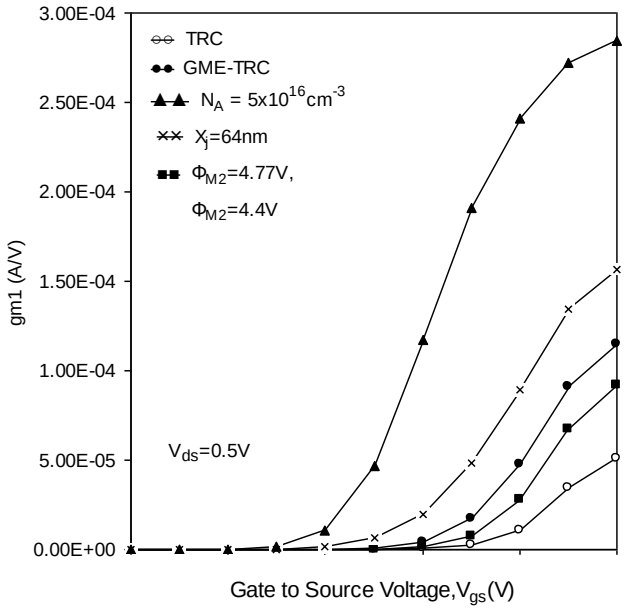

Fig.2. gm1 variation with gate to source voltage for TRC and GME-TRC variation for different workfunction difference, substrate doping and X_j.

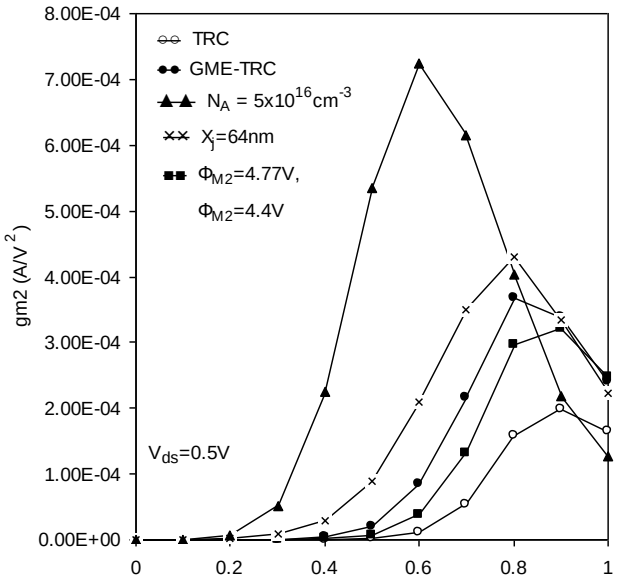

Fig.3. gm2 variation with gate to source voltage for TRC and GME-TRC variation for different workfunction difference, substrate doping and X_j.

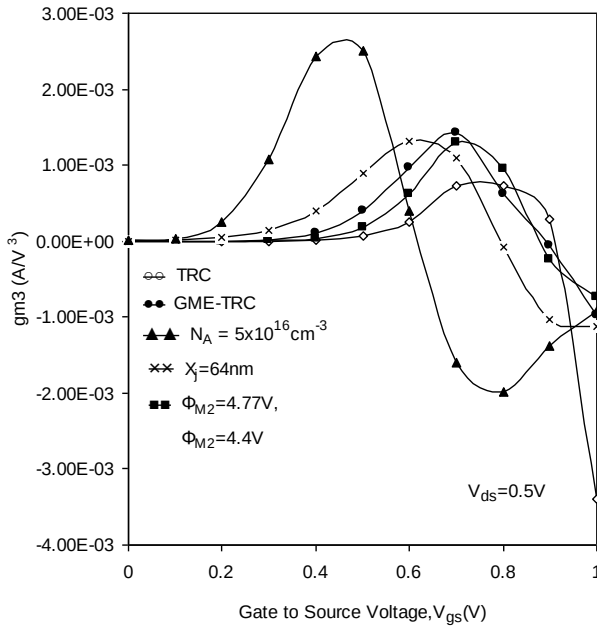

Fig.4. gm3 variation with gate to source voltage for TRC and GME-TRC variation for different workfunction difference, substrate doping and X_j.

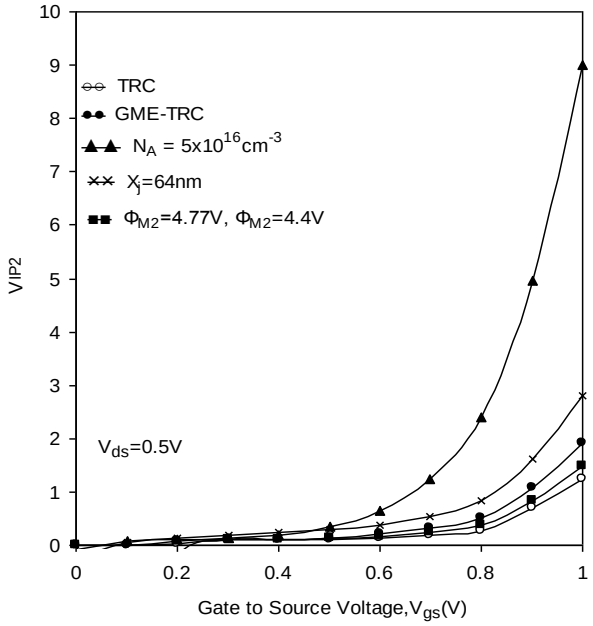

Fig.5. VIP2 variation with gate to source voltage for TRC and GME-TRC variation for different workfunction difference, substrate doping and X_j.

Fig.5. clearly reflect that VIP2 linearity index can be improved with the amalgamation of GME architecture on to a TRC MOSFET due to enhanced gate control over the channel, improved carrier transport efficiency and hence current driving capability, leading to improvement in the device transconductance and hence VIP2. The kink in VIP3 reflects the cancellation of third-order nonlinearity coefficient by device internal feedback around second-order nonlinearity; referred to as the second-order interaction effect. The device should preferably be biased in the pre-kink region. Fig.6. shows that, the kink is shifts towards the left for GME-TRC MOSFET as compared to TRC MOSFET. The decrease in NJD, substrate doping and increase in workfunction difference can further improved the linearity distortion performance due to the improved driving current capability and gate control for GME-TRC MOSFET, as shown in Fig.5 and 6 in terms of VIP2 and VIP3.

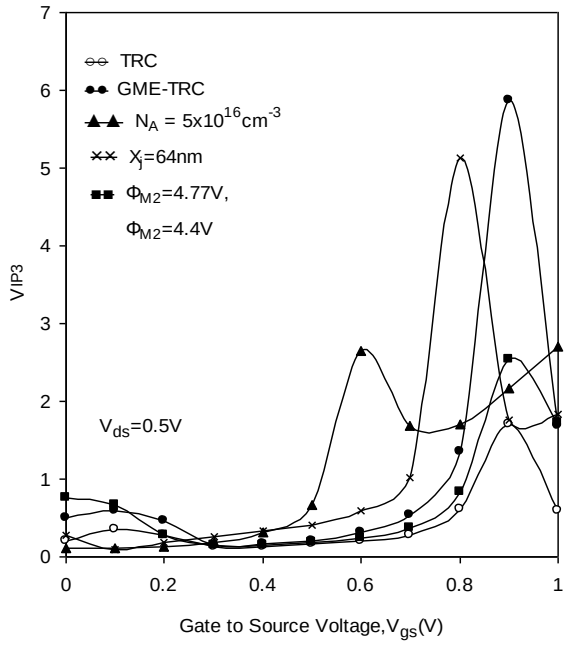

Fig.6. VIP3 variation with gate to source voltage for TRC and GME-TRC variation for different workfunction difference, substrate doping and X_j.

3 CONCLUSION

In this work, linearity performance of GME-TRC MOSFET is analyzed and the impact of various technological parameters such as work function difference, negative junction depth and substrate doping has been investigated and compared with conventional TRC MOSFET. The results reveal that GME-TRC design is superior to its counterpart TRC MOSFET in all aspects providing its consistently enhanced linearity performance in terms of improved higher order transconductance coefficients: gm1, gm2, gm3 and figure of merit (FOM) metrics: VIP2 and VIP3, thus proving its efficacy for RFIC design and wireless application.

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