Microwave and RF Applications of Gate Material Engineered Trapezoidal Recessed Channel (GME-TRC) MOSFET

Priyanka Malik *, Rishu Chaujar ** , Mridula Gupta* and R.S. Gupta *

* Semiconductor Devices Research Laboratory,Department of Electronic Science, University of Delhi, South Campus, New Delhi (India)-110021, prink.malik@gmail.com, rsgu@bol.net.in
** Department of Electronics, Deen Dayal Upadhyaya College, Karampura, University of Delhi, New Delhi-110015, rishuchaujar@rediffmail.com

ABSTRACT

In this paper, the RF performance for Gate Material Engineered-Trapezoidal Recessed Channel (GME-TRC) MOSFET has been investigated and the results so obtained are compared with Trapezoidal Recessed Channel (TRC) MOSFET, using device simulators; ATLAS and DEVEDIT. The result offers the opportunity for realizing the reliability of GME-TRC MOSFET for high speed logic and RF applications.

Keywords: ATLAS-3D, DEVEDIT-3D, GME, RF, SCEs.

1 INTRODUCTION

As the miniaturization of device proceed, conventional MOSFETs have demonstrated a continuous pace in performance improvement in order to develop opportunities for future high speed and low power applications, thus offering greater device efficiency for high performance RF applications. In highly scaled dimensions, MOSFETs have attained cut-off frequencies in the range of several GHz, making CMOS technology suitable for wireless communications and RF applications [1-4], thereby showing immense potential for mixed mode or system-on-chip applications. The scaled MOS device design, however is encountered with many challenges, such as the control of leakage current, short channel effects (SCEs), hot carrier effect and parasitic capacitances which results in degradation of device performance. Recessed Channel (RC) MOSFET mitigates many of the SCEs and hot-carrier effects [5–6] which is achieved by separating the source and drain (S/D) regions by a groove. Several studies have reported that the potential barrier at the corner of the groove is responsible for suppressing the SCEs, hot-carrier effects and punch-through. Although the improvement in SCEs is mainly attributed to these potential barriers, the carriers in the channel now require more energy to surmount these barriers, which limits its carrier transport efficiency and hence, the current driving capability.

In this work, an extensive study on GME-TRC MOSFET [7, 8] has been done and results reveal that the proposed design assimilate the potential benefits of RC MOSFET with GME architecture in terms of enhanced current driving capabilities and suppressed SCEs simultaneously, thereby improving RF performance of the proposed design. Further, the influence of technology parameters variation in terms of negative junction depth (NJD), gate metal workfunction difference and substrate doping (N_A) for GME-TRC MOSFET has been analysed, discussed and compared with conventional TRC MOSFET, using device simulators: ATLAS and DEVEDIT [9].

2 RESULT AND DISCUSSION

A schematic cross-sectional view of simulated devices i.e. TRC and GME-TRC MOSFET is shown in Fig.1 consisting of gate metal M1 of length L1 for TRC MOSFET and gate metal M1 and M2 of Length L1 and L2 for GME-TRC MOSFET. The work function of gate metal M1 is chosen as Φ_{M1}=4.77eV and channel length is taken as, L_g= L_1 =30nm for TRC. Further, for GME-TRC MOSFET, work function of gate metal M1 and M2 is chosen Φ_{M1}=4.77V and Φ_{M2} = 4.10V respectively.

Fig.2. reflects that there are considerably less parasitic capacitances for GME-TRC MOSFET as compared to conventional TRC MOSFET. This is due to the perceivable step in the surface potential profile as a consequence of different metal gate work functions, i.e. Φ_{M1} and Φ_{M2} for M1 and M2, respectively, that screens the channel region under metal gate M1 from drain potential variations, resulting in a redistribution of electric field across the channel, i.e. a relative increase near the source region and decrease near the drain region, which leads to improved electron concentration and driving current in the channel leading to a significant decrease in parasitic capacitances for GME-TRC MOSFET. Moreover, as NJD decreases, i.e. source/drain junction depth (X_j) increases, the effective height of barriers at the corner decreases, leading to the improvement in driving current across the channel, thereby reducing the parasitic capacitance.

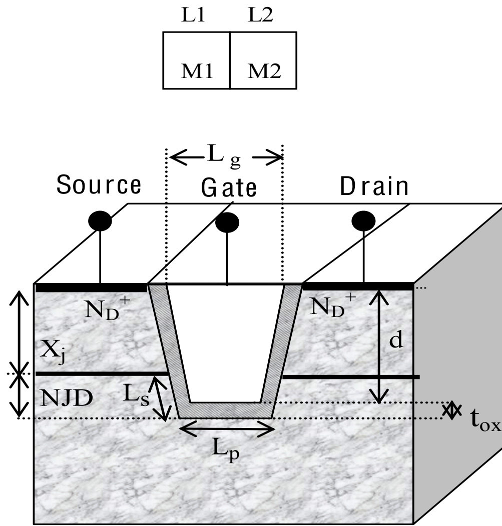

Fig.1. Schematic structure of GME-TRC and TRC MOSFET. The effective channel length L_{eff} corresponds here to the metallurgical channel length, taken along the gate oxide, i.e. L_{eff}= (2 x Ls) + Lp, where, Lp = 38nm, is the planar part and Ls = 32nm, is the angular part of the channel.Groove Depth (d)=76nm, NJD=32nm, N_A =$1x10^{17}$ cm^{-3}, N_D=$1x10^{20}$ cm^{-3}, t_{ox}=4nm, $_{ox}$=3.9. Work function (█$_{M1}$)=4.77V and channel length, Lg= L1 = 30nm for TRC MOSFET and for GME-TRC MOSFET, (█$_{M1}$)=4.77V and (█$_{M2}$) = 4.10V and and channel length Lg= L1 + L2 = 30nm . All these parameters are same in all figures unless stated otherwise.

Further, the decrease in substrate doping and increase in workfunction difference results in enhancement of transconductance and thus in CGS, as shown in Fig.2., due to improved carrier transport efficiency and gate controllability of the device.

The considerable decrease in parasitic capacitance contributes towards a significant improvement in cut-off frequency (ft), i.e. ft ≈ gm/2π(C_{GS}+C_{GD}), maximum unilateral power gain(MUG) and Gma (maximum available power gain) as shown in Fig. 3,4 and 5, respectively, for GME-TRC MOSFET as compared to conventional TRC MOSFET. Further, Fig.3,4 and 5 clearly shows that as NJD decreases, the effective height of barriers at the corner decreases, leading to the improvement in driving current across the channel, thereby reducing the parasitic capacitance and enhancing the ft, MUG and Gma, respectively. Further, as substrate doping decreases and difference in gate metal workfunction increases, gate control over the channel increases, leading to enhancement in transconductance, and thus improving MUG and Gma as shown in Fig.4 and 5 respectively.

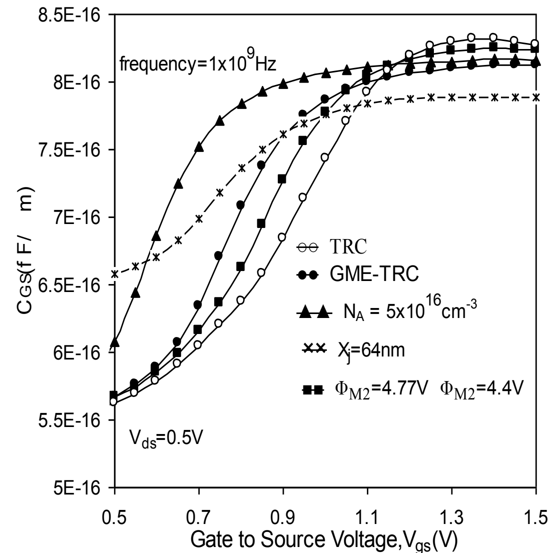

Fig.2. Parasitic Capacitance profile, i.e. C_{GS} versus V_{gs}, for GME-TRC MOSFET and TRC MOSFET with parameter variations such as metal gate workfunction difference, substrate doping (N_A) and NJD for GME-TRC MOSFET.

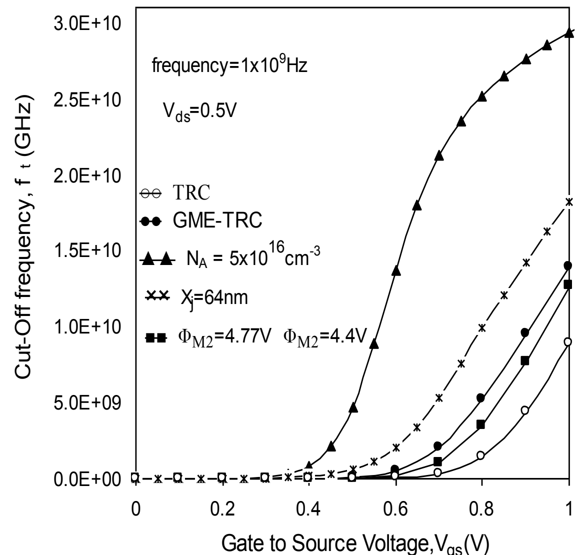

Fig.3. Cut-off frequency versus V_{gs} variation for GME-TRC and TRC MOSFET with different metal gate workfunction difference, substrate doping (N_A) and NJD for GME-TRC MOSFET.

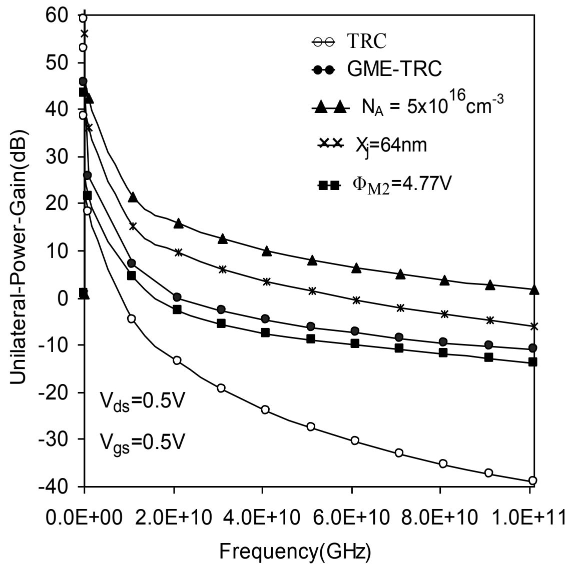

Fig.4. Unilateral power gain performance of TRC and GME-TRC MOSFET for different metal gate work function differences, substrate doping (N_A) and NJD and compared with previously described default parameters.

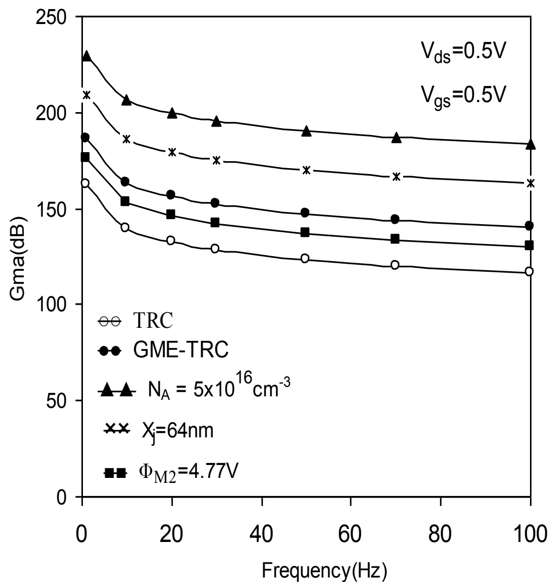

Fig.5. Maximum available power gain performance (Gma) of TRC and GME-TRC MOSFET GME-TRC MOSFET for different metal gate work function differences, substrate doping (N_A) and NJD and compared with previously described default parameters.

Fig.6. depicts that, the intrinsic delay, i.e. $(C_{gg} .V_{dd})/I_{ON}$, for GME-TRC MOSFET is significantly lower than that of TRC MOSFET, i.e. the incorporation of the dual material gate architecture leads to an appreciable reduction of intrinsic delay by 83.8%. The decrease in substrate doping further adds to the improvement in intrinsic delay by 89.5% due to the improved gate control and mobility across the channel, reflecting its use in high speed applications. Fig.6. also shows that, there is a significant improvement in intrinsic delay for higher gate metal workfunction difference and lower NJD due to increased carrier transport efficiency and decreased parasitic capacitances of the device. Thus, GME-TRC MOSFET exhibits superior performance in terms of cut-off frequency, unilateral power gain, maximum available power gain (Gma) and intrinsic delay.

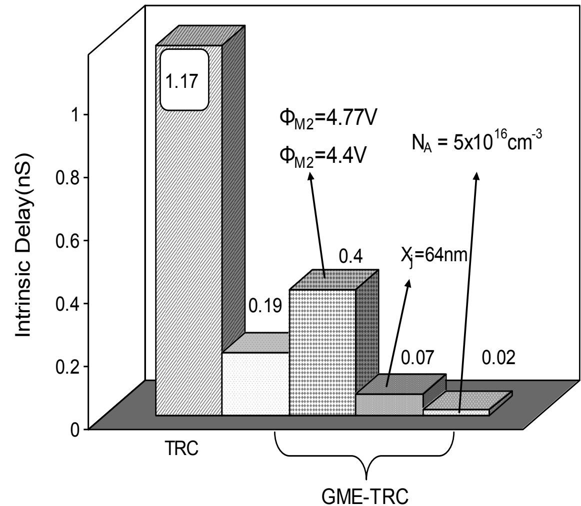

Fig.6 Intrinsic Delay of TRC and GME-TRC MOSFET GME-TRC MOSFET for different metal gate work function differences, substrate doping (N_A) and NJD and compared with previously described default parameters.

3 CONCLUSION

In this work, the RF performance investigation of proposed GME-TRC MOSFET has been carried out and the impact of various technological parameters such as work function difference, substrate doping and Negative Junction Depth are investigated for GME-TRC MOSFET and further compared with conventional TRC MOSFETs by using device simulators: ATLAS and DEVEDIT. Results clearly depict that, GME-TRC MOSFET exhibits superior performance as compared to TRC MOSFET in terms of reduced parasitic capacitances which further contributes towards the improved cut-off frequency, Unilateral power gain, maximum available power gain (Gma) and intrinsic delay, thus proving its efficacy for high speed logic and RF applications.

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