A Continuous Compact Model of Short-Channel Effects for Undoped Cylindrical Gate-All-Around MOSFETs

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ABSTRACT

A continuous and explicit compact model of short-channel effects (SCEs) for undoped cylindrical Gate-All-Around (GAA) MOSFETs is presented in this paper. SCEs are implemented into an analytic and continuous drain-current model based on a surface potential approach. Results regarding *I-V* characteristics, for short-channel transistors, are compared to numerical simulations and validate our method in all operating regions.

Keywords: compact modeling, gate-all-around mosfet, short-channel effects, surface potential model.

1 INTRODUCTION

Multiple-gate devices such as surrounding-gate transistors (Fig. 1) represent the most promising solution to reach the CMOS scaling roadmap for the 22nm node and beyond [1]. To provide a continuous drain-current model for short-channel MOSFETs (channel length below 100nm), parasitic effects have to be accounted for [2]. According to the gate length reduction, an accurate compact model of SCEs is presented and implemented into a surface-potential-based model for undoped cylindrical GAA MOSFETs. This novel short-channel compact model is validated in all operating regions from comparisons with TCAD numerical simulations [3], making it suitable for circuit design simulations.

2 SHORT-CHANNEL EFFECTS MODEL

Modeling SCEs for all operating regions consists in studying the device electrical behavior both in linear and saturation regions. In this way, the threshold voltage roll-off ΔV_{TH} and the subthreshold swing degradation *SS* are, in a first step, modeled. First, the approach consists in solving the 2D cylindrical Poisson's equation (1) written as

$$\frac{\partial^2\phi_{2D}(x,\rho)}{\partial\rho^2}+\frac{1}{\rho}\frac{\partial\phi_{2D}(x,\rho)}{\partial\rho}+\frac{\partial^2\phi_{2D}(x,\rho)}{\partial x^2}=\frac{q}{\varepsilon_{Si}}n_i e^{\frac{\phi_{2D}(x,\rho)}{ut}} \quad (1)$$

Where ut is the thermal voltage, ε_{si} the silicon permittivity, q the electron charge and n_i the intrinsic concentration.

Using a superposition method and satisfying boundary conditions, the 2-D electrostatic potential is then solved and written as

$$\phi_{2D}(x,\rho)=\phi_0(\rho)+\phi_1(x,\rho) \quad (2)$$

Where $\phi_0(\rho)$ is the 1D Poisson's equation solution and $\phi_1(x,\rho)$ is the remnant 2D Poisson's equation solution which are explicitly modeled in [4,5].

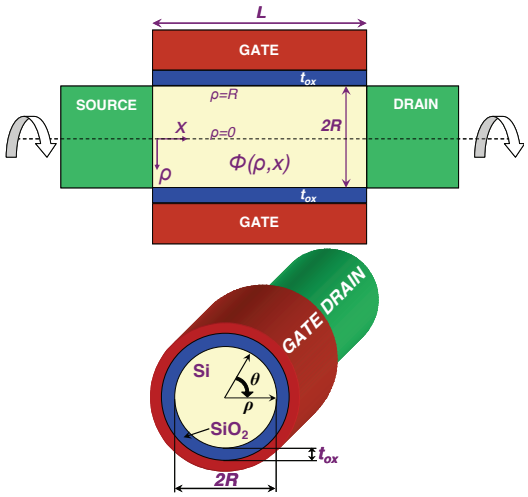

Fig. 1. Schematic cross sections in the channel direction *x* (up) and in the transverse direction ρ (down) of the cylindrical GAA MOSFET.

2.1 Threshold voltage roll-off

We propose in this paper a new effective and accurate method to model ΔV_{TH} (in both linear and saturation regions) and *SS*. The 2D electric potential expression $\phi_{2D}(x,\rho)$ is included into the subthreshold drain current I_{DS} expression (3). From the I_{DS} expression and by assuming it equal to $(2\pi R/L)10^{-7}$ at threshold (using the current-defined method), the threshold voltage can be expressed.

$$I_{DS} = \mu \pi R \frac{ut\left(1-\exp\left(\frac{-V_{DS}}{ut}\right)\right)}{\int_0^L \frac{1}{\int_0^R q\, n_i \exp\left(\frac{\phi_{2D}(x,\rho)}{ut}\right) d\rho} dx} \overset{@\ threshold}{=} \frac{2\pi R}{L} 10^{-7} \quad (3)$$

Where R is the nanowire radius, μ is the electron mobility, L the gate length of the device and V_{DS} the drain-source voltage. From [5], the method consists in solving explicitly all integrals in (3). Consequently, relevant assumptions are made in the two-dimensional potential expression $\phi_{2D}(x,\rho)$. This study leads therefore to express explicitly the drain current (3) written as follows

$$\frac{ut\left(1-\exp\left(\frac{-V_{DS}}{ut}\right)\right)}{\exp\left(\frac{\Delta\phi - V_{TH,SHORT}}{ut} + \ln\left(Y\left(V_{TH,SHORT}, V_{DS}\right)\right)\right)} = \frac{2\cdot 10^{-7}}{\mu\, q\, n_i\, R\, L} \quad (4)$$

From (4), $\ln(Y(V_{TH,SHORT},V_{DS}))$ is clearly identified to be the term corresponding to the threshold voltage shift when the gate length reduces. Moreover, the Y function corresponds to the following expression

$$\begin{aligned} Y &= \int_0^L \exp\left(\frac{-\phi_1(x,R)}{ut}\right) dx \\ &\approx 2\frac{R}{\lambda}\ln(ut) - \frac{R}{\lambda}\ln\left(ut + V_{bi} - \phi_0(R)\right) \\ &\quad - \frac{R}{\lambda}\ln\left(ut + V_{bi} - \phi_0(R) + V_{DS}\right) + L \end{aligned} \quad (5)$$

Where V_{bi} is the built-in voltage (≈0.6V) and λ is deducted from the 2D analysis and defined as

$$\lambda = \frac{-C_{ox} R}{\varepsilon_{si}} \frac{J_0(\lambda)}{J_1(\lambda)} \quad (6)$$

Where C_{ox} is the cylindrical gate oxide capacitance per area. J_0 and J_1 are the first kind Bessel functions respectively of order 0 and 1. In order to extract a short-channel threshold voltage expression from (4), the approach consists to expand $\ln(Y(V_{TH,SHORT},V_{DS}))$ to the first order. Based on TCAD simulations, we assume the short-channel threshold voltage value in a range between $V_{TH,LONG}$ and $V_{TH,LONG}$ − 100mV where $V_{TH,LONG}$ is the long-channel threshold voltage. A first order expansion is therefore achieved in the previous range and $\ln(Y(V_{TH},V_{DS}))$ is rewritten as follows

$$\ln\left(Y\left(V_{TH,SHORT}, V_{DS}\right)\right) = a \cdot V_{TH,SHORT} + b \quad (7)$$

with

$$a = 10 \cdot \left(\ln\left(Y\left(V_{TH,LONG}, V_{DS}\right)\right) - \ln\left(Y\left(V_{TH,LONG} - 0.1, V_{DS}\right)\right)\right) \quad (8)$$

$$b = \ln\left(Y\left(V_{TH,LONG} - 0.1, V_{DS}\right)\right) - a \cdot \left(V_{TH,LONG} - 0.1\right) \quad (9)$$

Where the long-channel threshold voltage is defined as

$$V_{TH,LONG} = \Delta\phi + ut\, \ln\left(\frac{L_{Di}^2}{R\, \mu\, \varepsilon_{Si}\, ut^2} 10^{-7}\right) \quad (10)$$

Where $\Delta\Phi$ is the work function difference between the gate material and the intrinsic silicon and L_{Di} is the Debye length. The short-channel threshold voltage expression $V_{TH,SHORT}$ is then obtained (11) which leads, by making the difference with the long-channel threshold voltage model $V_{TH,LONG}$ (10), to reproduce the roll-off ΔV_{TH} as the channel length reduces. The ΔV_{TH} model presents excellent matching with TCAD simulations as presented in Fig. 2.

$$V_{TH,SHORT} = \frac{1}{1-a}\left[\Delta\phi + b + ut\, \ln\left(\frac{L_{Di}^2}{R\, L\, \mu\, \varepsilon_{si}\, ut^2} 10^{-7}\right)\right] \quad (11)$$

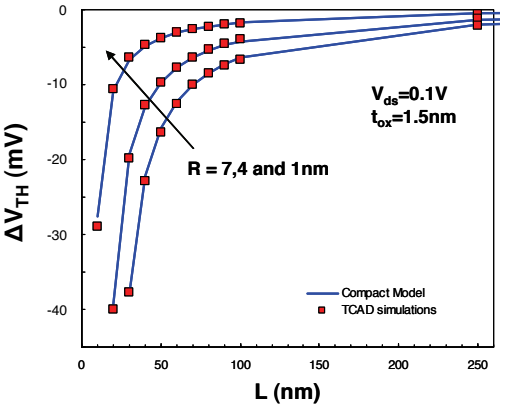

Fig. 2. Threshold voltage roll-off versus channel length for different nanowire radii (in linear region).

2.2 DIBL and subthreshold swing

As the short-channel threshold voltage gets a V_{DS} dependency through a, b and (5), DIBL is directly taken into account and can be evaluated setting (12). The DIBL model presents excellent matching with TCAD simulations as presented in Fig. 3.

$$DIBL = V_{TH,SHORT}(@\, V_{DS} = 1.2V) - V_{TH,SHORT}(@\, V_{DS} = 0.1V) \quad (12)$$

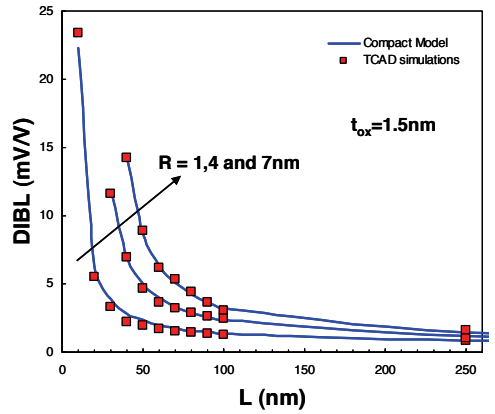

Fig. 3. DIBL versus channel length for different nanowire radii.

Moreover, by using the expression $\ln(Y(V_{GS},V_{DS}))$ in the drain current expression, *SS* is finally modeled explicitly with the subthreshold drain current slope (13).

$$SS = \frac{\partial V_{GS}}{\partial \log I_{DS}} \tag{13}$$

As observed in Fig. 4, the subthreshold swing model presents excellent matching with TCAD numerical simulations for both low and high drain-source voltage.

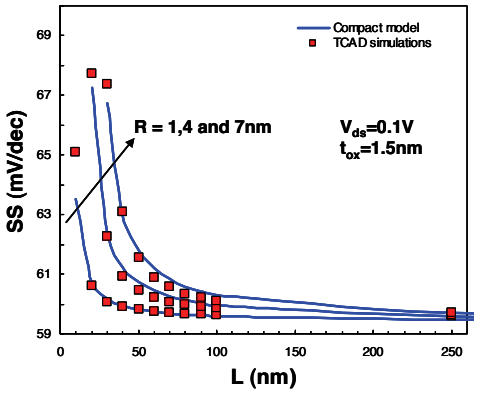

Fig. 4. Subthreshold swing versus channel length for different nanowire radii (in linear region).

2.3 Channel length modulation

In this work, the channel length modulation effect (CLM) is modeled as well. This effect results from the pinchoff displacement in the channel at high V_{DS} [6-7] making the channel shorter than the physical gate length L. The method consists in modeling the pinchoff through an electrical gate length expression L' replacing itself the physical gate length L in the drain current expression.

From [8], an explicit expression of the saturated drain-source expression is deducted which is expressed as

$$V_{DSsat}{}' = V_{GS} - \Delta\phi - ut \ln V_A - 2ut \ln\left(\frac{2L_{Di}}{R}\right) - 3ut \tag{14}$$

Where V_A is a constant parameter which indicates the reaching of the saturation region, fixed at 0.5 in this work. As the previous saturated drain-source voltage expression (14) is linear according to V_{GS}, a new drain-source saturation voltage expression with respect to TCAD simulations is investigated. In this way, V_{DSsat} is written as (15).

$$V_{DSsat} = \frac{\ln\left(1+\exp\left(20 \cdot V_{DSsat}{}'\right)\right)}{20} + 3ut \tag{15}$$

An effective drain-source voltage V_{DSeff} (16) is deducted (hold at V_{DSsat} when the saturation region is reached) which leads to express the gap ΔL between L and the channel pinchoff (17).

$$V_{DSeff} = \frac{V_{DS}}{\left(1+\left(\frac{V_{DS}}{V_{DSsat}}\right)^8\right)^{\frac{1}{8}}} \tag{16}$$

$$\Delta L = \lambda \ln\left(1+\frac{V_{DS}-V_{DSeff}}{V_E}\right) \tag{17}$$

Where V_E is a constant parameter. The CLM effect is then accounted for in the model by substituting L with the new gate length expression L' defined in (18).

$$L' = L - \Delta L \tag{18}$$

3 RESULTS

All SCEs terms including CLM are accounted for in the surface-potential-based compact model described in [8]. Therefore, an accurate short-channel correction is provided using a surface-potential-based drain-current model as observed on I-V characteristics and derivatives plotted Figs. 5-8.

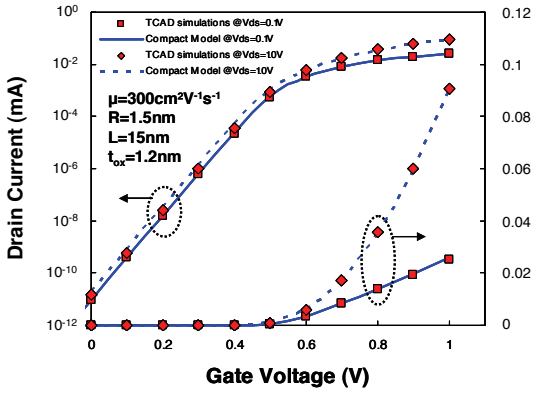

Fig. 5. Drain current versus gate voltage in linear (solid curves) and saturation regions (dashed lines).

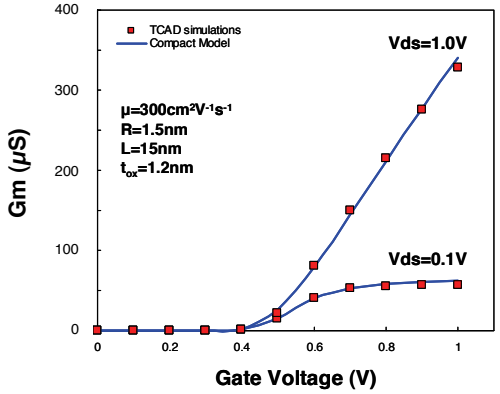

Fig. 6. Transconductance Gm in linear and saturation regions.

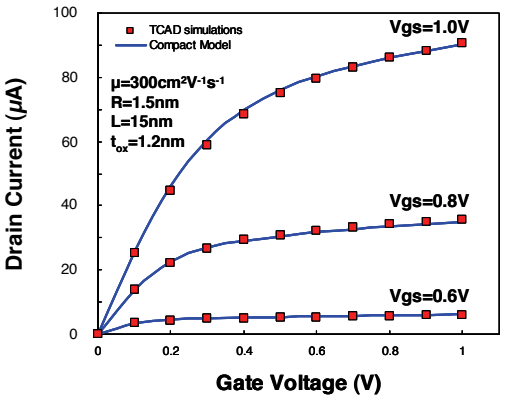

Fig. 7. Drain current versus drain voltage for several gate voltages.

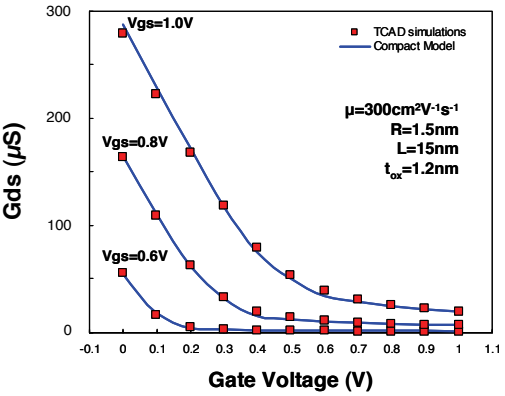

Fig. 8. Drain-source conductance Gds for several gate voltages.

4 CONCLUSION

A compact model of short-channel effects for undoped cylindrical GAA MOSFETs is presented in this paper. This model is validated in all operating regions and for gate lengths down to 10 nm by making confrontations with TCAD simulations. The excellent accuracy of this explicit compact model makes it suitable for circuit design simulations.

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