Xsim: Benchmark Tests for the Unified DG/GAA MOSFET Compact Model

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ABSTRACT

This paper presents benchmark tests of the unified compact model (Xsim) for double-gate (DG) and gate-all-around (GAA) silicon-nanowire (SiNW) MOSFETs, which has been developed over the years with the unified regional modeling (URM) approach. The core Xsim model is extended from the bulk-MOS model that encompasses partial- and full-depletion SOI as well as DG/GAA FinFET/SiNW devices, with doping scaling from highly-doped to undoped body. Terminal currents and terminal charges are physically scalable over wide ranges of geometry and structural variations, satisfying the basic model benchmark tests such as Gummel symmetry test (GST), slope-ratio test (SRT), tree-top test (TTT), harmonic-balance test (HBT), as well as transcapacitance symmetry and reciprocity. The ultimate goal of the Xsim model is for unification of MOSFET compact models with various gate, body, as well as source/drain structures and dimensions in one unified core framework for simulating and designing integrated circuits in future generation technologies, including bulk/SOI/FinFET/SiNW or a hybrid of them.

Keywords: Benchmark tests, compact model, double-gate (DG), gate-all-around (GAA), MOSFET, silicon nanowire (SiNW), unified regional modeling (URM), Xsim.

1 INTRODUCTION

CMOS technology has evolved over half a century with continued scaling, so do the generations of compact models that represent its building block — the MOSFET, from conventional bulk/SOI to emerging double-gate (DG) and gate-all-around (GAA) silicon-nanowire (SiNW) devices. The demands on the features and qualities of compact models have also evolved over the years, from simple piecewise and empirical models in the early days to highly complex formulations fulfilling various model requirements in today’s nanoscale analog/digital designs. Gone with the days in which pieces of models for various effects from different sources can be assembled and implemented into a core model. A single physics-based core model that is developed with dc/ac consistency and with bias/geometry/temperature/frequency scalability is needed, from which variability/noise/distortion/reliability modeling can be developed [1]. This represents a major undertaking in developing a core model for future generation technologies.

Our compact model (Xsim) development is such an effort over the past 12 years [2]–[13], which aims at unification of MOSFET compact models with the unified regional modeling (URM) approach. It is based on unified regional surface-potential solutions for bulk-MOS, which can be extended to generic SOI/DG/GAA MOSFETs with common/independent-gate biasing and with/without body contact. The dc/ac full model is physically scalable in geometry/bias and in body thickness/doping, encompassing partial/full depletion and volume/strong inversion. New paradigm shift in “ground-referencing” [4] as well as “source/drain by label” [5], [6] provides complete Gummel symmetry while allowing physical modeling of asymmetric devices, which also provides easy extension to include contact effects for modeling PN-junction and Schottky-barrier (SB) [7] or dopant-segregated Schottky (DSS) [8] source/drain. The core model is directed towards modeling emerging devices and technologies in one unified framework without duplicating efforts, which also provides seamless transitions among various device structures and operations, with selectable accuracy for simulation and verification of future-generation ULSI circuits.

This paper presents basic benchmark tests of the Xsim model for the generic DG/GAA MOSFET, such as transcapacitance symmetry/reciprocity, Gummel symmetry test (GST), harmonic-balance test (HBT), slope-ratio test (SRT) and tree-top test (TTT).

2 XSIM MODEL

The basic idea in the URM approach to Xsim model development is the regional modeling of the surface potential in the generic MOSFET with two gates and arbitrary body doping and thickness. The drain current is expressed as separate functions of the top/front and bottom/back gates as well as source/drain terminal voltages, with asymptotic surface-potential solutions in the respective accumulation, depletion, volume-inversion, and strong-inversion regions and unified through smooth transition functions and coupled with seamless transitions across different region of operations. The core model equations have been presented in [2], [3].
Many higher-order effects have been modeled during bulk-model development and extended to DG/GAA modeling, such as vertical-field mobility [9], bias-dependent series resistance [10], velocity saturation and overshoot [11], poly-silicon accumulation/depletion/inversion effects (PAE/PDE/PIE) [12], and quantum-mechanical effect (QME) [13].

3 BENCHMARK TESTS

3.1 DC I–V Characteristics

Accurate dc I–V modeling is the basis of a core model. Xsim DG/GAA model has less than 30 model parameters that can be extracted following a one (or two) iteration procedure. Model playback (lines) of a \( L = 180\) nm and \( R = 2\) nm GAA device is shown in Fig. 1(a) for the transfer and output characteristics, compared with measurements (symbols). Note that negative values of \( V_{ds} \) have been physically modeled. The corresponding 1\(^{st}\) and 2\(^{nd}\) order derivatives are shown in Figs. 1(b) and 1(c), respectively.

![Figure 1(a)](image1a.png)

**Figure 1(a):** GAA SiNW: (left) linear/saturation \( I_{ds} - V_{gs} \) and (right) \( I_{ds} - V_{ds} \) characteristics, compared with measurements (symbols).

![Figure 1(b)](image1b.png)

**Figure 1(b):** Corresponding derivatives of 1(a): (left) linear/saturation \( g_{m} - V_{gs} \) and (right) \( g_{d} - V_{ds} \) characteristics.

![Figure 1(c)](image1c.png)

**Figure 1(c):** Corresponding derivatives of 1(b).

Model playback (lines) of a \( L = 500\) nm and \( T_{Si} = 140\) nm undoped DG FinFET is shown in Fig. 2 for the transfer and output characteristics, compared with measurements (symbols).

![Figure 2](image2.png)

**Figure 2:** DG FinFET: (left) \( I_{ds} - V_{gs} \) and (right) \( I_{ds} - V_{ds} \) characteristics, compared with measurements (symbols).

3.2 AC C–V Characteristics

Physical and scalable charge-based C–V modeling is another key requirement for a core model. Xsim ac model is consistently derived from the dc/charge model. Among the 30 model parameters, 9 of them are related to ac model. Fig. 3 shows model playback (lines) of a long-channel DG FinFET transcapacitances at various biasing conditions, compared with Medici numerical data (symbols).

![Figure 3](image3.png)

**Figure 3:** DG FinFET: (left) normalized gate capacitance at 3 \( V_{gs} \) and (right) transcapacitance in saturation, compared with Medici data (symbols).

PDE and QME are modeled in the coupled surface-potential solutions. One example for the DG FinFET is shown in Fig. 4. Another example for bulk-MOS is shown in Fig. 5 at various biases, and the exacted physical parameters are verified with Medici of the same device.

![Figure 4](image4.png)

**Figure 4:** DG FinFET: (left) \( C_{gs} \) with or without PDE and (right) surface potential with or without QME and compared with Medici data (symbols).
GST for the undoped DG FinFET [4], with the 6th-order derivative is to be fulfilled. Fig. 7 shows such a behavior in a common “ground” reference in model formulations [4], [5] instead of swapping source/drain terminals for negative Vds (which implies “source-reference”). This is believed to remedy the effect due to neglecting the hole currents from source/drain PN junctions in the unipolar assumption. However, such glitches will result in incorrect high-order harmonics in HBT [15], which are important in RF circuits. Even with a perfectly formulated drain-current model that is an exact odd function of Vds in DG/GAA devices in which the body potential is floating, hole currents from source/drain PN junctions have small contributions when Vds approaches zero; however, they are not included in compact models based on the unipolar assumption. This is analogous to the one-carrier solution of the Poisson equation in almost all compact models, and the effect of neglecting one carrier (hole) in undoped DG/GAA devices is only observable in the gate capacitance near flatband condition when rigorous two-carrier solution is solved [16]. In Fig. 9, we show Xsim HBT result, in which a “symmetric imref correction” (SIC) is implemented to remedy the effect due to neglecting the hole currents from source/drain PN junctions in the unipolar formalism.

3.3 Transcapacitance Symmetry/Reciprocity

Transcapacitance symmetry and reciprocity are two major model requirements, which also represent a difficult task in physical charge model formulations. Xsim model behaviors are demonstrated in Fig. 6.

3.4 Gummel Symmetry Test

The GST [14] is another key benchmark test and difficult task as well. It becomes even more challenging in DG/GAA devices in which there is no body contact. The solution is to model the source/drain current separately with a common “ground” reference in model formulations [4], [5] instead of swapping source/drain terminals for negative Vds (which implies “source-reference”). This is believed to be the only feasible approach if the GST at any higher-order derivatives is to be fulfilled. Fig. 7 shows such a GST for the undoped DG FinFET [4], with the 6th-order derivative (inset) passing through Vx = 0 smoothly. Any singularities at Vds = 0 will destroy Gummel symmetry, and any inappropriate smoothing will result in wrong number of zero crossings in the even-order derivatives, although it may pass Vx = 0 smoothly. Another GST for the GAA SiNW is shown in Fig. 8, compared with measured GST.

3.5 Harmonic-Balance Test

A model with small glitches in higher-order GST would have negligible effects on its current and conductance. However, such glitches will result in incorrect high-order harmonics in HBT [15], which are important in RF circuits. Even with a perfectly formulated drain-current model that is an exact odd function of Vds in DG/GAA devices in which the body potential is floating, hole currents from source/drain PN junctions have small contributions when Vds approaches zero; however, they are not included in compact models based on the unipolar assumption. This is analogous to the one-carrier solution of the Poisson equation in almost all compact models, and the effect of neglecting one carrier (hole) in undoped DG/GAA devices is only observable in the gate capacitance near flatband condition when rigorous two-carrier solution is solved [16]. In Fig. 9, we show Xsim HBT result, in which a “symmetric imref correction” (SIC) is implemented to remedy the effect due to neglecting the hole currents from source/drain PN junctions in the unipolar formalism.
3.6 Slope-Ratio and Tree-Top Tests

Last, but not the least, SRT and TTT [14] of the Xsim DG/GAA model are shown in Fig. 10, showing model behavior complying with theory. The Xsim drain current can be evaluated around or even below the flatband voltage.

![Graph](image)

Figure 10: GAA: (left) SRT at 3 temperatures and DG/GAA: (right) TTT in linear/saturation regions.

4 SUMMARY AND CONCLUSIONS

The past decade has seen us developing a full core model (Xsim), starting with the 0.25-μm technology node in threshold-voltage-based model [17], evolving through non-pinned surface potential [18], strained-Si/DG [19], scalable surface-potential-based URM [20], and unified bulk/SOI/DG/GAA/SB/DSS core model [21] for nanoscale CMOS technology nodes. The efforts in Xsim model development pave the way towards unification of MOS compact models in one unified framework, which will prove to be useful for future generation ULSI technology nodes and emerging device building blocks.

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REFERENCES


