Modeling of Gate Leakage, Floating Body Effect, and History Effect in 32nm HKMG PD-SOI CMOS

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ABSTRACT

The High-K Metal Gate (HKMG) technology has become the keystone to reduce gate leakage and enable the continuous scaling of transistors towards 32nm node and beyond. However, the reduction of gate leakage in 32nm HKMG PD (Partially Depleted)-SOI (Silicon-On-Insulator) CMOS (Complementary Metal–Oxide–Semiconductor) inevitably changes the modeling methods for gate current, floating body effect, and history effect that were used in poly gate technology. Consequently the modeling of SOI transistor needs to account for the change of gate leakage and diode currents as well. In this study, we investigated the gate leakage, floating body effect, and history effect in 32nm HKMG PD-SOI CMOS transistors, and developed comprehensive SOI gate leakage and diode current models for the purpose of circuit simulation and design. Compared to 45nm poly gate PD-SOI transistors, the gate leakage in 32nm HKMG counterparts is at least one order lower, the floating body voltage has been reduced, and history effect in high-threshold (HVT) devices at Vdd=0.9V and T=25C is decreased from 8% to 2%.

Keywords: high-k metal gate, silicon-on-insulator, floating body effect, history effect.

1 INTRODUCTION

For over 20 years, the gate length of transistors has been aggressively scaled down. One of the key methods for achieving gate length scaling is to thin gate oxide continuously. However, the scaling of electrical gate oxide thickness (Tox) in poly gate transistors has encountered substantial technical difficulties since 90nm node due to large gate leakage and running out of atoms in ultra-thin oxide layer. Gate oxide with thickness of 1.2nm has already been implemented in 90nm node [1]. Thereafter, the scaling of gate oxide roughly remained stagnant in poly gate transistor. The impasse was overcome by the High-K Metal Gate (HKMG) technology, which not only significantly reduces gate leakage but also keeps ~0.7X scaling of gate oxide towards 32nm node or beyond [2]. Nevertheless, the reduction of gate leakage in 32nm HKMG PD-SOI CMOS and HKMG related specifics largely impact and complicate the modeling for gate current, floating body effect, and history effect, which are critical to model SOI transistors accurately. In the paper, we will present the measured results and discuss modeling details for gate current, floating body voltage, and history effect in 32nm HKMG PD-SOI CMOS, respectively. A short conclusion will be summarized in the end.

2 GATE LEAKAGE

Although high-k dielectrics can relieve the burden of electrical field in the gate stack and thereby reduce the leakage, the tunneling current still dominates gate current when electrical oxide thickness is less than 2nm. In addition, interface traps and formation of oxygen vacancies in high-k gate stack can also cause defect-related leakage. The defect-related leakage has to be minimized or eliminated in order to meet the reliability requirements.

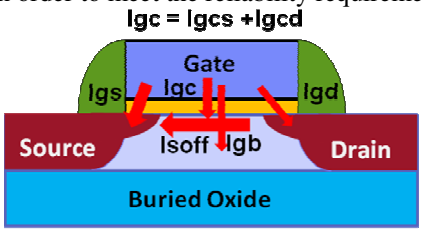

Fig 1. Components of gate leakage

As shown in Fig. 1, gate current consists of four major components: Igb (gate-to-substrate), Igs (gate-to-source), Igd (gate-to-drain), and Igc (gate-to-channel). Igc is further partitioned into Igcs (gate-to-channel at source side) and Igcd (gate-to-channel at drain side). Depending on device structure and device technology, those components of gate current can have different dependence on electrical field and temperature. At very large electrical field and under persistent electrical stress, gate current can increase with time due to field-induced traps and recombination centers, which eventually leads to catastrophic failure or rupture of gate dielectrics. Furthermore, the interaction between gate current and interface traps in high-k dielectrics may cause the shift of threshold voltage, and current and capacitance dispersion in transistors. Thus, the gate stack has to be well-engineered to mitigate the adverse impact of traps and recombination centers.

In 32nm PD-SOI transistors, various gate current components can substantially influence the I-V characteristics of the device. Gate current in conjunction with other currents such as channel current, diode currents, BJT current, impact ionization current, and gate induced drain leakage (GIDL) determine the floating body voltage in the device channel. The floating body voltage can be largely regulated by Igb, which in turn impacts history effect (hysteresis) caused by dynamic charge variations in the floating body of PD-SOI CMOS transistors during switching. Igs and Igd could be a concern in deep

accumulation region or pass-gate configuration. Igcs and Igcd can change the channel current distribution in the strong inversion region.

The gate current has exponential dependence on electrical oxide thickness. Due to random local variations and processing variations across the wafer [3, 4], the electrical oxide thickness could fluctuate around a normal value. Generally, for any given bias point, the measured data of gate leakage has a considerable distribution across the wafer as illustrated in Fig. 2. (The gate stack of the transistors for the data points in Fig. 2 is not fully optimized.)

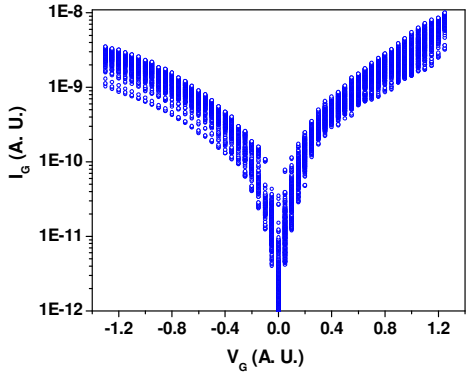

Fig. 2. Example of gate leakage variations in PD-SOI transistors

We used SAS program to remove the outliers or bad data points and chose median data points for modeling. The variability of gate current is considered through the distribution parameters in the model.

3 FLOATING BODY VOTAGE AND HISTORY EFFECT

The floating body effect in PD-SOI transistors is critical to SOI circuit simulation and design. The body currents (Igb, diode currents, BJT current, impact ionization current, and GIDL) and capacitive voltage coupling from the device terminals control the body voltage of floating PD-SOI devices. Under DC condition, the floating body voltage is mainly determined by two body current components: Igb and diode currents. Thus, the measurement of Igb and diode currents in PD-SOI transistors is essential to modeling of floating body effect. The floating body effect leads to history effect in switching SOI circuit.

In a floating SOI transistor, the body voltage can change the threshold voltage of the transistor during switching. Under transient conditions, the body voltage is also a function of input switching conditions like gate pulse width, period and slew rate. When the terminal input is changing very slowly with time, the body potential can reach its equilibrium value. However, if the input is switching fast compared to the charging/discharging times of the body through various body currents and coupling capacitors, and then the body potential does not reach its equilibrium value before the input changes to a new state. Thus there is a difference in body potential of a transistor between a steady (slowly switching) input and a fast switching input, which depends on the switching history of the transistors. This leads to a variation in the threshold voltage of the device which in turn causes variations in the propagation delay through a transistor. Such effect is called history effect in SOI transistors. History effect introduces uncertainty in predicting the performance of the circuit. It is thus important to take into account this variability in gate delay while designing circuits.

The switching transition delays of an inverter chain responding to a sharp pulse in time domain can be used to characterize the history effect in PD SOI logic device technology. The propagation delays of the first switch and the second switch are used to define the technical term "History" in the measurement. The first switch (1SW) is a transition in which the input switches after a long period of inactivity so that the charges in the floating body have come to equilibrium. The second switch (2SW) is referred to a transition "immediately" following a previous input transition such that the floating body charges have still not come to equilibrium. History is defined as 2(T1-T2)/(T1+T2) [5], where T1 is the propagation delay during 1SW transition and T2 is the delay during 2SW transition. A positive history means that 1SW delay T1 is larger than 2SW delay T2, while larger 2SW delay results in a negative history. Since the difference of body potential in 1SW and 2SW transition is closely tied to the delay difference between 1SW and 2SW, therefore, the delay measurement clearly manifests the history effect.

4 MEASUREMENT AND MODELING

We systemically measured gate current, diode currents, body voltage, and history in 32nm HKMG PD-SOI transistors. Separate test designs were employed for the measurement of total gate current, Igb, diode currents, and history. Based on measured results, model for each current component was developed and integrated into the transistor model.

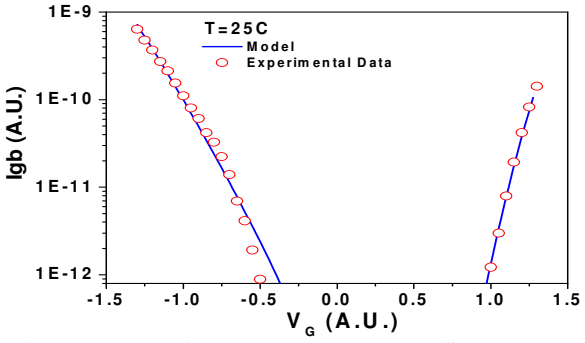

Fig. 3. Igb experimental data and model fit at T=25C

Igb and diode currents were measured in body-contacted counterparts of floating PD-SOI transistors at 125C, 85C, 25C, -10C, -40C. Fig. 3 and Fig. 4 shows measured data and model fit for Igb and diode currents.

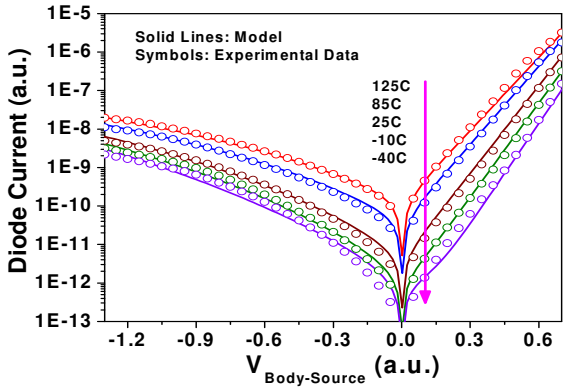

Fig.4. Diode Currents at T=125C, 85C, 25C, -10C, -40C

History effect can cause a pulse to shrink (if the history is positive) or stretch (if the history is negative) as it propagates down a chain of inverters. We exploit this property to measure history effect using the technique described in [5]. History effect in three VT types of 32nm HKMG PD-SOI CMOS (RVT/HVT/SVT) at different Vdd was measured to verify Igb and body diode models, which is shown in Fig. 5.

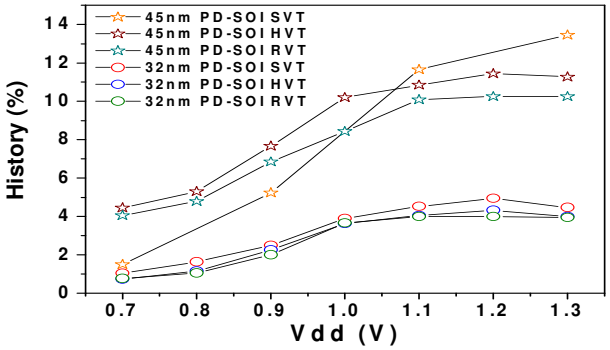

Fig. 5. Vdd dependence of history effect in PD SOI CMOS

The body voltage in 1SW is determined by a balance of forward and reverse diode currents. The body voltage in 2SW is regulated by inversion Igb and the forward diode current as well as ratio of capacitive coupling of the body-to-drain and body-to-gate. In 32nm HKMG PD-SOI transistors, the Igb is several orders lower than the reverse diode leakage at Vds=Vdd, thus, Igb does not affect the body potential at transistor "OFF" state. However, at transistor "ON" state, due to gate-to-body capacitive coupling, Igb can readily change the body potential. Igb tends to reduce the body potential if Vgb <0 and increase the body potential if Vgb>0. As Vdd increases, both Igb and diode current increase, the elevated Igb and forward diode current drive the 2SW body voltage to have stronger Vdd dependence than 1SW body voltage; hence the difference of body potential in 1SW and 2SW transition becomes larger. This leads to the increase of history with Vdd. As seen from Fig. 5, the device with lower threshold voltage tends to have smaller history effect. This can be explained by the tradeoff between higher Igb and weaker drain coupling due to smaller junction capacitance.

The temperature dependence of history effect in 32nm HVT CMOS at different Vdd was extensively studied. Fig. 6 shows the results. A good agreement has been achieved between history data and model results. For the devices under consideration, average inverter history decreases with temperature. Since capacitive coupling and generation/recombination currents are strong functions of temperature, hence history has significant temperature dependence. The diode current quickly increases with temperature; however, Igb is a very weak function of temperature. Thus, the temperature dependence of body potential in both 1SW and 2SW is mainly determined by the diode current. At elevated temperature, the charging/discharging time of the body is shortened and diode currents reduce the body potential in both 1SW and 2SW. Therefore, the difference of body potential in 1SW and 2SW is also reduced accordingly, so is the history.

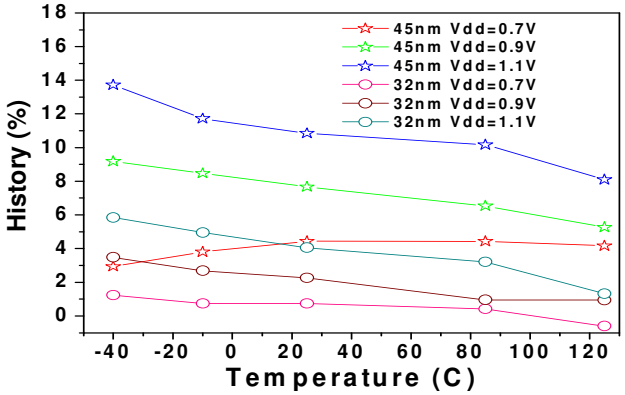

Fig. 6. Temperature dependence of history effect in HVT PD SOI CMOS

The history effect in 32nm HKMG PD-SOI CMOS at Vdd=0.9V and T=25C is decreased from 8% in 45nm poly-gate PD-SOI CMOS to 2%, which is partially due to suppression of floating body effect with thinner Tox and smaller Igb current. Compared to 45nm poly-gate PD-SOI CMOS technology, the floating body voltage in 32nm HKMG PD-SOI CMOS has been reduced, especially in p-type transistor as shown in Fig. 7.

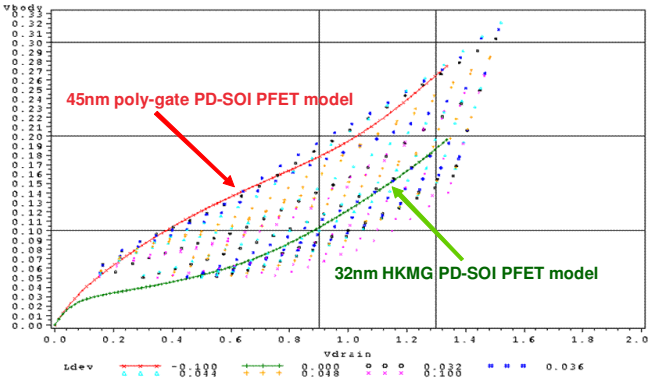

Fig. 7. Floating body voltage in 45nm poly-gate and 32nm HKMG PD-SOI p-type transistor

To model Igs, Igd, Igcs, and Igcd currents accurately, total gate current was fully characterized in floating-body transistors with a variety of gate length and width across the wafer. The measurement was performed at different gate and drain bias in the temperature range of -40C to 125C.

The transition points at different drain bias as shown in Fig. 8, where the total gate current changes conduction direction, were determined from the data, which are important to determine the partition of Igcs and Igcd currents in gate current model. Using the gradual channel approximation, the average surface potential along the channel at those transition points is roughly equal to gate bias. Thus, the work function of the gate stack in the transistors can be estimated using either device model or TCAD simulation.

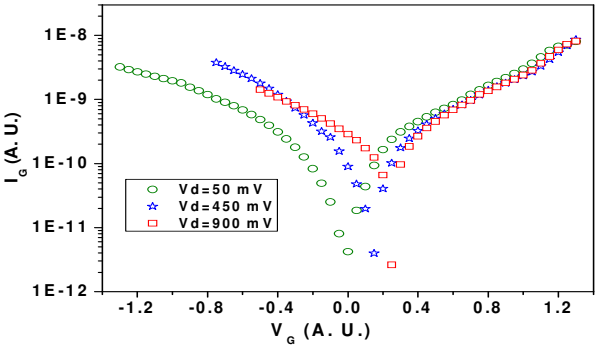

Fig. 8. Sign change of total gate leakage

The overlap gate current components: Igs and Igd, dominate the gate current in the deep accumulation region while all gate current components contribute to the total gate current in the strong inversion region. The dependence of gate currents on gate length was also investigated experimentally. It was found that the gate length dependence of gate current is weak. Based on the measured data, an as-fit SOI gate leakage model for all gate current components was developed for 32nm HKMG PD-SOI CMOS first, and then re-centered to meet the targets and integrated with the transistor model.

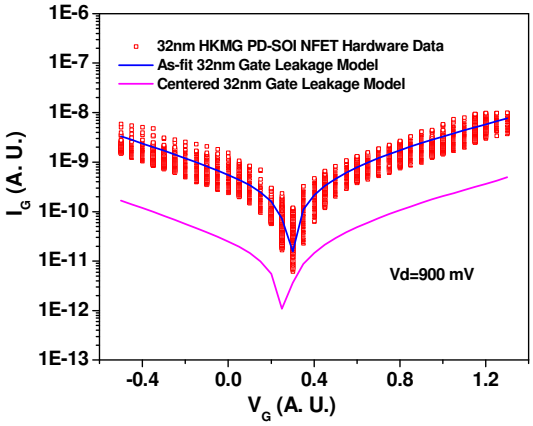

Fig. 9. Gate leakage data, as-fit gate leakage model, and centered gate leakage model for 32nm HKMG PD-SOI n-type transistor.

The experimental data and model results of total gate leakage for n-type and p-type transistors (The gate stack of the transistors is not fully optimized.) are shown in Fig. 9 and Fig. 10, respectively. Compared to measured data of gate leakage in 45nm poly gate PD-SOI transistors, 32nm HKMG devices have much lower gate leakage, which results in smaller history effect and floating body voltage.

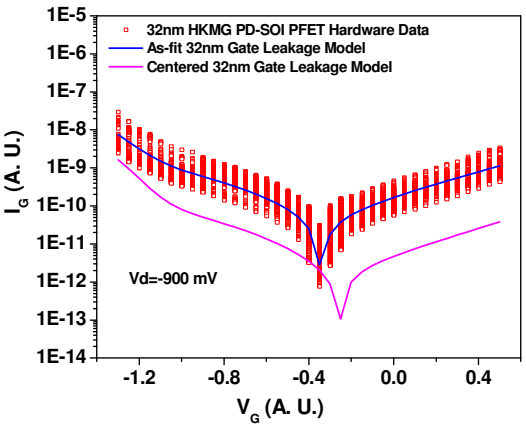

Fig. 10. Gate leakage data, as-fit gate leakage model, and centered gate leakage model for 32nm HKMG PD-SOI p-type transistor.

5 SUMMARY

In summary, the gate leakage, floating body effect, and history effect in 32nm HKMG PD-SOI CMOS have been extensively investigated and analyzed. Based on the measured data, comprehensive HKMG PD-SOI gate leakage and diode current models have been developed for PD-SOI circuit simulation and design. The model simulation results for the bias dependence of total gate leakage and floating-body voltage agreed with the experimental data very well. A good prediction on history effect in 32nm HKMG PD-SOI CMOS has also been achieved by the model. The reduction of gate leakage in 32nm HKMG PD-SOI CMOS results in smaller history effect and floating body voltage. The history in 32nm HKMG HVT devices at Vdd=0.9V and T=25C is reduced from 8% to 2% as compared to 45nm poly gate PD-SOI transistors.

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