Correlation between Gated-Diode R-G Current and Performance Degradation of SOI n-MOSFETs after F-N Stress Test

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ABSTRACT

A correlation between the gated-diode R-G current and the performance degradation of SOI n-channel MOS transistor after F-N stress test has been demonstrated in this paper. Due to increase of interface traps after F-N stress test, the generation-recombination (R-G) current of the gated-diode in the SOI-MOSFET architecture increases while the performance characteristics of MOSFET transistor such as the saturation drain current and sub-threshold slope generate degradation. From a series of experimental measurements of the gated-diode and the SOI-MOSFET DC characteristics, a linear decrease of the drain saturation current and increase of the threshold voltage as well as the like-line rise of the sub-threshold swing and the corresponding degradation of the trans-conductance are also observed. These results provide theoretical and experimental evidences for us to use the gated-diode tool to monitor SOI-MOSFET degradation.

Keywords: MOSFET degradation, F-N stress, interface traps, gated-diode method, SOI technology.

1 INTRODUCTION

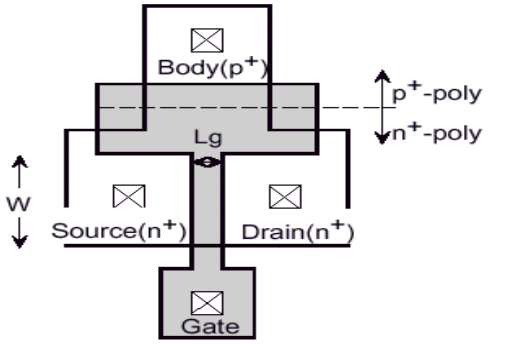
SOI devices are of great interest for low voltage low-power CMOS circuits, memory, high frequency and high temperature applications. The main advantages are related to improved isolation, reduced sub-threshold slope, parasitic capacitance and low leakage currents, as well as possible reduction of the short channel effects compared with bulk silicon devices. However, when the devices are scaled down, SOI MOSFETs also suffer from hot carrier effects. In order to control and model transistor performance, it is essential to accurately monitor hot carrier injection-induced interface states in SOI MOSFETs.

Recently, a refined forward gated-diode method has been used to characterize the interface states and extract the bulk carrier recombination lifetime in the SOI devices [1-3]. This method uses the gate-voltage-controlled interfacial recombination-generation current (R-G) IR-G to monitor the generation rate of interface traps and the charging rate of oxide traps in MOSTs. It has shown that the method is simple, sensitive, quickly applicable and nondestructive and some very good results have been achieved.

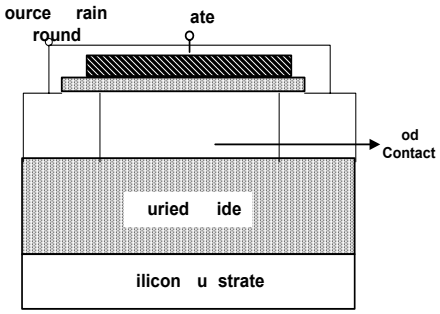
However, traditional transistor reliability measurements monitor the shifts in the saturation drain current ΔI_{dsat}, threshold gate voltage ΔV_{th}, maximum trans-conductance ΔG_m and sub-threshold voltage swing ΔS of the MOSFET transistors [4-5]. In order to erect the clear figure from the R-G current of the gated-diode method to the performance degradation of MOSFET devices, we demonstrate the anticipated dependencies of these traditional characteristics on the forward gated-diode R-G current from the experiments of MOSFET's F-N stress tests in this paper.

2 EXPERIMENTS

The experiments were performed in PD SOI n-channel MOSTFET, fabricated on a SIMOX wafer. This tested SOI-MOST has a drawn channel length/width aspect ratio of L/W = 30 μm /15 μm, a 160A gate oxide, and separate source, drain, gate, and body contact pads. The top review of the fabricated SOI device and the experimental set-up are shown in Fig.1(a) and (b), respectively.



(a)



(b)

Fig.1 Top view of the fabricated SOI device (a) and diagram of the experimental set-up (b).

During the stress-and-measure (SAM) experiments, the nMOSTs were stressed by F-N tunneling current under the conditions of a constant gate voltage of 5V and the different stress time while their electrical characteristics were measured after each stress duration. In each gated-diode method experiment, the R-G current was obtained under the conditions that the source and drain are connected to ground while applying the biased voltage V_b of 0.35V to the body contact. As a result, the source and drain / body contact forms a forward diode. By scanning the gate voltage, we can obtain the R-G current characteristics modulated by the gate voltage. In each measurement of the MOSFET performance, the drain saturation current is measured at V_{DS}=V_{GS}=1.0V. The threshold voltage is defined as the gate voltage at I_{ds}=1 μ A with V_{DS}=0.5V. The subthreshold slope is computed at I_{ds}=100nA with V_{DS}=0.5V while the maximum trans-condutance is obtained form the same curve.

3 RESULTS AND DISCUSSION

Fig.2 shows typical gated-diode IR-G -VG characteristics with increasing accumulated stress time of an nMOST stressed by the F-N effect. As seen in this figure, the IR-G-peak increases with F-N stress time and occurs at a nearly constant VG ≈ 0.45V. The rise of IR-G-peak is due to the stress-generated SiO2/Si interface traps over the channel space-charge region.

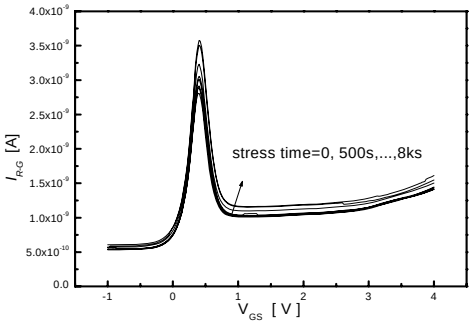


Fig.2 Dependence of R-G current on the F-N stress time.

The negligible VG shift of the IR-G-peak indicates negligible charging of the oxide fixed charges over total channel space-charge region because the F-N stress effect do not have sufficient kinetic energy, KE=q(VDS–VDS-sat) ≈ q[VDS-(VGS -VT)], ≈ 3.3-1.6=1.7eV, to surmount the 3.13eV SiO2/Si barrier [6].

The typical transfer characteristics of this n-channel device with different F-N stress time were shown in Fig.3. The stress-induced widening of the sub-threshold swing and the corresponding threshold voltage shift can be observed in this figure. According to our requirement mentioned above, the sub-threshold swing and the threshold voltage for the different F-N stress time can be extracted and the dependence on the stress time is obtained.

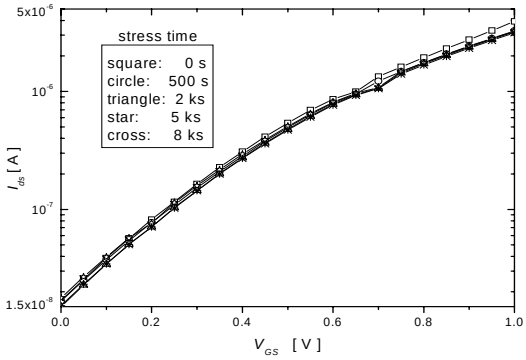


Fig.3 Typical transfer characteristics of SOI n-channel MOSFET devices with the different F-N stress time.

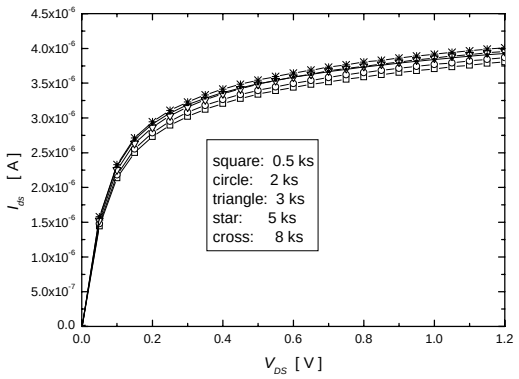


Fig.4 Typical output characteristics of n-channel SOI MOSFET device under the different F-N stress time.

Fig. 4 shows the dependence of the drain current on the sets of stress condition. This linear dependence is anticipated from the simple textbook theory of Idsat and VGT. Carrier mobility degradation in the channel should be responsible for the decrease of the drain current in the linear region. The more decrease of the drain current in the saturation region is determined by two key factors, the mobility degradation and the threshold voltage shift. From the simple square equation of the MOST current, Idsat=(W/2L)Coxμ_{eff}(VGS-Vth)2, the output characteristics degradation with the stress time is easy to be understood.

Based on our obtained the R-G current of the gated-diode, transfer curve and the output curves characteristics of the n-channel SOI MOSFET device, it is an easy thing to perform the correspondence analysis between the R-G current and the performance degradation of MOSFET after F-N stress tests.

Fig.5 demonstrates the linear dependence of ΔI_{dsat} ΔV_{th} on $\Delta I_{R-G-peak}$ for the F-N stress effect. This linear relationship is anticipated from the simple theory of I_{dsat} and V_{th} : from the parabolic equation of the MOST output characteristics in the saturation region, mentioned above, we obtain $I_{dsat} / I_{dsat\,0} \approx -(2\Delta V_{th})(V_G - V_{th})$ where $I_{dsat\,0}$ denotes the pre-stress value. Since $\Delta V_{th} = -q(\Delta N_{ot} + \Delta N_{it})C_{ox}$ and $I_{R-G-peak} \propto N_{it}$, the oxide traps can be negligible from Fig.2, we can immediately obtain $\Delta I_{dsat} \propto \Delta V_{th} \propto I_{R-G-peak}$.

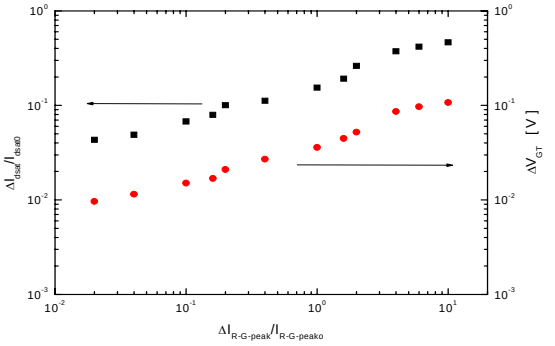


Fig.5 Extracted correspondence between $\Delta I_{dsat} / I_{dsat\,0}$, ΔV_{th} and $\Delta I_{R-G-peak} / I_{R-G-peak_0}$ from the measured gated-diode R-G current and the SOI-MOSFET output characteristics.

The calculated sub-threshold swing variation and the trans-conductance degradation were shown in Fig.6. It increases initially as $\Delta S \propto \Delta I_{R-G-peak}$, then rises faster, and finally approaches again $\Delta S \propto \Delta I_{R-G-peak}$. This is consistent with the simple expression, S=2.303(kT/q)[1+(Cit+Cd)/Cox] where Cit=qNit which indicates an initial and final linear dependence, $\Delta S \propto \Delta C_{it} \propto qN_{it} \propto I_{R-G-peak}$ while the super-linear rise of ΔS in the mid-range of stress is caused by the faster change of the surface potential with Δ Vth relative to the change of Nit. Similarly, the trans-conductance degradation of $\Delta G_m / G_m$ can be explained. However, due to the unique Kink feature of the PD SOI MOSFET devices, the trans-conductance degradation of this SOI device demonstrates more complex.

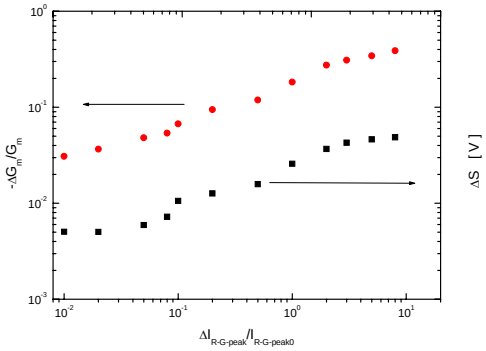


Fig. 6 Extracted correspondence between ΔS, $\Delta G_m / G_m$ and the $\Delta I_{R-G-peak} / I_{R-G-peak\,0}$, $L = 100nm$, $t_{ox} = 2nm$, $T = 300K$.

4 CONCLUSION

In this paper, the correlation between performance degradation of SOI n-channel MOS transistor and gated-diode R-G current after F-N stress test has been studied

experimentally. A proof is given of the theoretically expected dependence of saturation drain current, threshold voltage, sub-threshold swing and trans-conductance degradations on the gated-diode R-G current peak. This correlation provides the basis for using the forward gate-diode method to monitor MOS transistor degradation.

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