Electrical Characteristics of 16-nm Multi-Gate-and-Multi-Fin Field Effect Transistors and Digital Circuits

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ABSTRACT

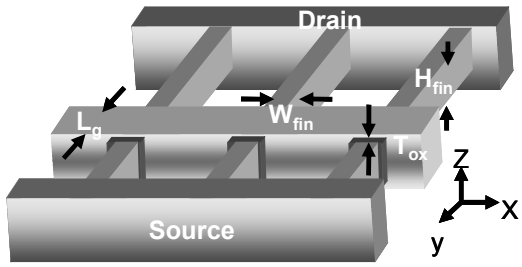
The structure with vertical channel is attractive due to suppression of the short-channel effect, where the shape of silicon fin determines the device performance. In this work, the DC characteristics of single-fin FinFET are simulated, which shows a better immunity against fluctuation induced by random dopant than that of tri-gate and quasi-planar fin shapes. Increasing the number of silicon fins of FinFET can further improve the performance. Examining the fluctuation induced by random dopant in CMOS inverter and SRAM circuits with triple-fin structure shows that the fluctuation of intrinsic gate delay and SNM in triple-fin FinFET are smaller and larger, respectively, than that of others due to higher driving current.

Keywords: Fin aspect ratio, FinFET, Tri-gate FET, Co-planar FET, Static noise margin, Gate delay, Random-dopant-induced fluctuations, 3D density-gradient equations

1 INTRODUCTION

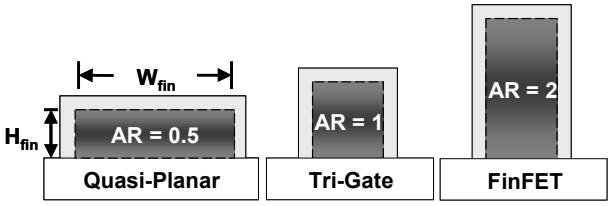
As the gate length of bulk metal oxide semiconductor field effect transistor (MOSFET) shrinks below 32 nm, devices with vertical channel have drawn people's attention due to diverse fascinating characteristics [1-3]. Multi-gate-and-multi-fin FETs have thus been proposed to provide a large driving capability [3]. Investigation of DC and AC characteristics of multi-gate-and-multi-fin devices plays a crucial role for IC application; unfortunately, studies on their digital circuits' behavior and random-dopant-induced fluctuations have not been clearly drawn yet.

In this work, we estimate electrical characteristics including threshold voltage (V_{th}) and gate capacitance (C_g) of 16-nm-gate multi-gate-and-multi-fin FETs, and delay time of an inverter and static noise margin (SNM) of a 6T SRAM. Large-scale random-dopant-induced fluctuations of the aforementioned characteristics are further discussed with respect to different fin aspect ratio (AR = the fin height / the effective fin width), where the device characteristics are obtained by solving a set of 3D density-gradient equations coupled with Poisson equations as well as electron-hole current continuity equations [3] under our parallel computing system [4]. Notably, an experimentally validated simulation [5] is also conducted to investigate the fluctuation property.

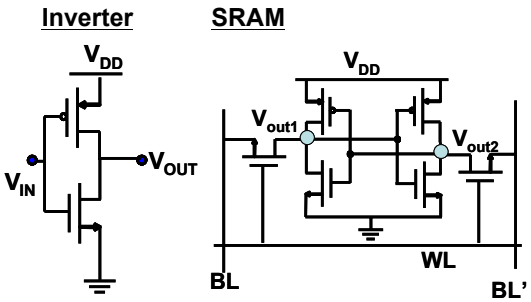


(a)

Normalized V_{th} Variation		
AR = 0.5	33.3 %	27.3 %
AR = 1	26.7 %	20.0 %
AR = 2	18.7 %	11.3 %



(b)



(c)

Figure 1: (a) A schematic and (b) fin cross-section view of triple-fin MOSFET. The fin shapes of transistor are FinFET (AR = 2), tri-gate (AR = 1) and quasi-planar (AR = 0.5) and their normalized V_{th} variation are summarized in the table, where the normalized V_{th} variation is defined as the difference of V_{th} between the 14.5-nm- and the 17.5-nm-gate lengths divided by the nominal V_{th}. (c) Inverter and SRAM are used as the test circuit, where V_{DD} is 1 V.

2 SIMULATION TECHNOLOGY

The nominal channel doping concentration of the explored devices is 1.48 x 10^{18} cm^{-3}. They have a 16 nm gate, a gate oxide thickness of 1.2 nm, and a work function of 4.4 eV. Considering the effect of random dopant fluctuation (RDF), we take FinFET shape as a generation example of random dopant. There are 378 dopants are first randomly generated in a cube of 80 x 40 x 80 $(nm)^3$. The 80 x 40 x 80 $(nm)^3$ cube is then partitioned into 125 subcubes of 16 x 8 x 16 $(nm)^3$. The number of dopants in each subcube varies from zero to 9, with an average of three. The 125 generated subcubes are then equivalently mapped into the channel region of the device channel for the 3D device simulations with discrete dopants.

The device simulation is performed by solving a set of 3D density-gradient equations coupled with Poisson equations as well as electron-hole current continuity equations [6-9] on a parallel computing system [10-16]. In "atomistic" device simulation, the resolution of individual charges within a conventional drift-diffusion simulation using a fine mesh creates problems associated with singularities in the Coulomb potential [17]. The potential becomes too steep with fine mesh, and therefore, the majority carriers are unphysically trapped by ionized impurities, and the mobile carrier density is reduced. Thus, the density-gradient approximation is used to handle discrete charges by properly introducing related quantum-mechanical effects, and coupled with Poisson equation as well as electron-hole current continuity equations [18-19]. The accuracy of the simulation technique was confirmed by comparing simulated fluctuation results with measurements of experimentally fabricated 20 nm devices.

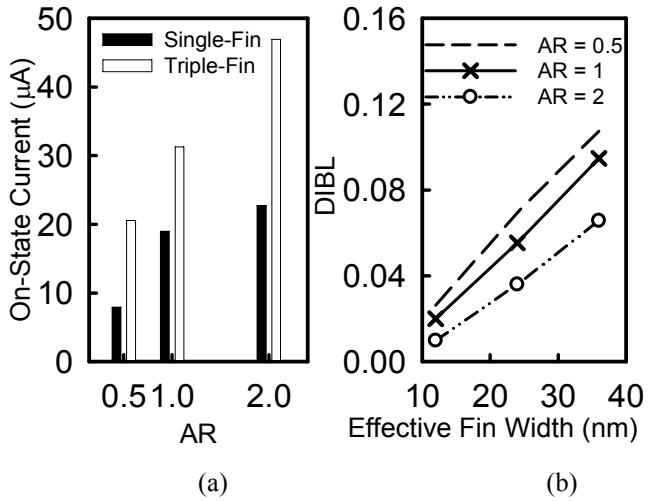


Figure 2: (a) Plots of the on-state current for the 16-nm-gate single-fin and triple-fin MOSFETs with AR = 0.5, 1 and 2. (b) DIBL for 16-nm-gate triple-fin MOSFETs with AR = 0.5, 1 and 2.

3 RESULTS DISCUSSION

Figure 1(a) illustrates the studied 3D triple-fin transistors. The Fig. 1(b) shows the plot of fin cross-section views for FinFETs (AR = 2), tri-gate (AR = 1) and quasi-planar (AR = 0.5), respectively. The inset table of Fig. 1(b) presents that the normalized V_{th} of triple-fin FinFET is 1.7 (18.7 / 11.3 = 1.7) times smaller than single-fin FinFET transistors that means the short channel effect can be suppressed well. To compare the device characteristics on a fair basis, the cross-section area of the fin for the explored devices are fixed at about 128 nm^2. The similar cross-section area and V_{th} indicates the same control volume of device channel under the same operation condition. Figure 1(c) shows the inverter and SRAM circuits which are tested for electrical characteristics of multi-fin device. The device gate length is chosen as 16 nm. The V_{th} of the explored 16-nm-gate transistors are calibrated to 150 mV.

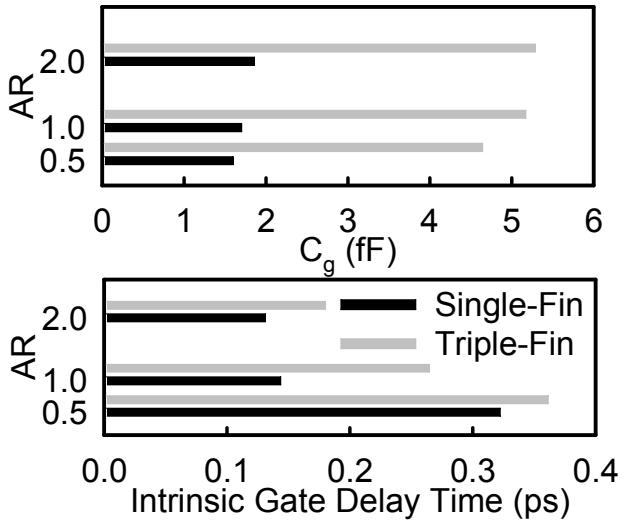
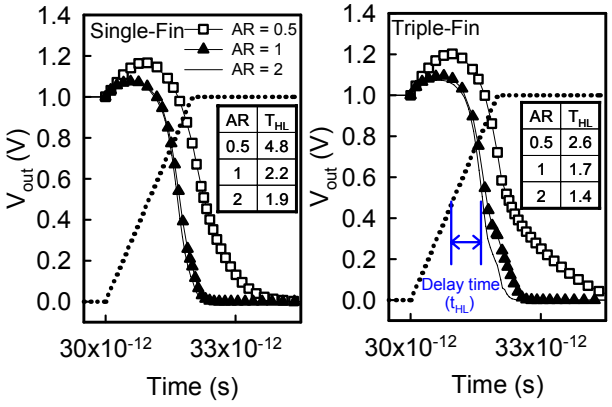


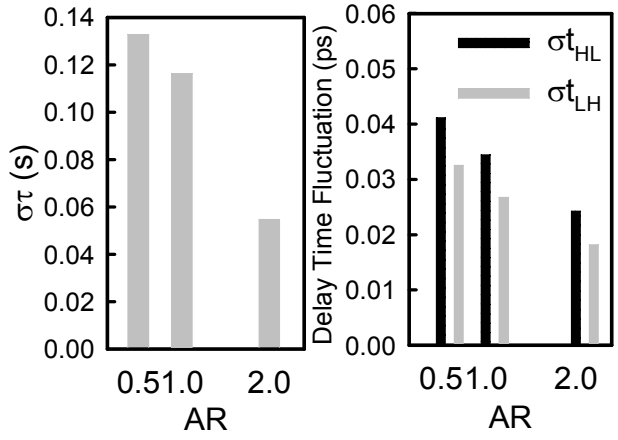
Figure 3: The upper and lower plot show the gate capacitance and intrinsic gate delay time for the 16-nm-gate single-fin and triple-fin MOSFETs with different fin structure, respectively.

The on-state current of triple-fin FinFET has larger on-state current than single-fin FinFET, as shown in Fig. 2(a). Comparison of different fin shape shows that the DIBL of triple-fin FinFET is 1.63 times smaller than quasi-planar MOSFET due to better gate control capability, where the effective fin width is the sum of the fin width and two times fin height. The upper illustration of Fig. 3 demonstrates the gate capacitance of the 16-nm-gate single- and triple-fin devices. Compared with the triple-fin quasi-planar devices, C_g of triple-fin FinFETs is increased by a factor of 3.7. The large C_g of triple-fin MOSFET with a large AR enhances charge control; nevertheless, the increased C_g affects the operation speed of transistors. In order to study the trade-off



(a) (b)

Figure 4: The high-to-low transition for (a) single-fin and (b) triple-fin MOSFET with AR = 0.5, 1 and 2, where the high-to-low delay time is defined in the inset.



(a) (b)

Figure 5: (a) The στ of triple-fin transistors. (b) The σt_{HL} and σt_{LH} of the tested inverter with AR = 0.5, 1 and 2, respectively.

between I_{on} and C_g, we calculate intrinsic gate delay of transistor ($\tau = C_g V_{DD} / I_{on}$), as shown in the lower illustration of Fig. 3. The results show that single-fin FinFET presents 1.1 and 2.5 times smaller than that of the tri-gate FinFET and the quasi-planar MOSFET due to relatively smaller C_g. Then we test the performance of single- and multi-fin MOSFET in inverter circuit, as shown in Fig. 4. As expected, both single- and triple-fin FinFET inverters present smallest t_{HL} with respect to different AR and show the benefit of FinFET in both DC and dynamic characteristics. Although the gate capacitance of the triple-fin transistor is larger, it provides a smaller transition delay than that of the single-fin transistor due to increase of driving current. Consider the fluctuations induced by random-dopant, the στ of triple-fin FinFET is 2.4 times smaller than that of single-fin one. Though C_g of triple-fin

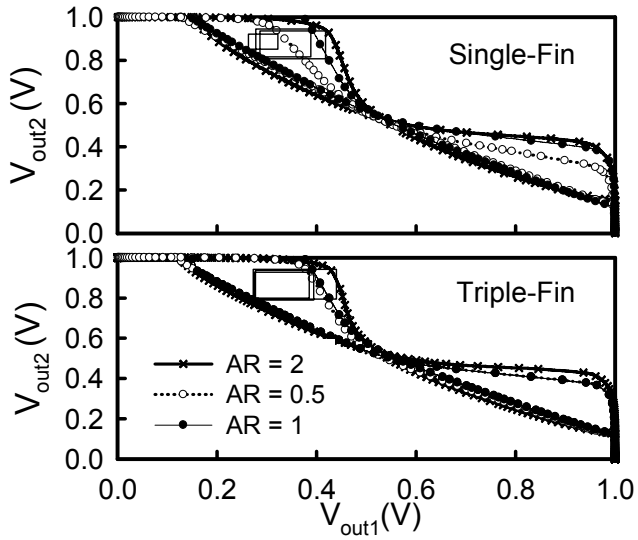


Figure 6: The upper and lower plot of static transfer characteristics for single- and multi-fin with AR = 0.5, 1 and 2, respectively.

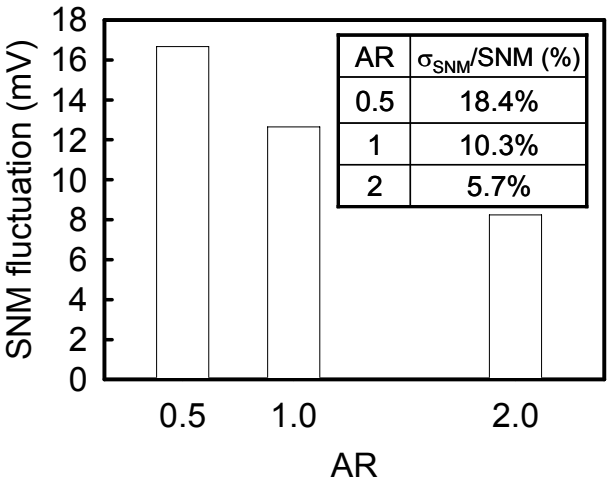


Figure 7: SNM fluctuation of the examined multi-fin structure with AR = 0.5, 1 and 2, respectively. The normalized σSNM is summarized in the inset table.

FinFETs is quite large, the large on-state current reduces the στ of triple-fin FinFET, as shown in Fig. 5(a). Fig. 5(b) shows the delay time of triple-fin FinFET inverter has 2.4 times smaller than triple-fin quasi-planar MOSFET because of better driving capability. And the σt_{HL} exceeds σt_{LH} due to controlled by n-FETs which has larger mobility. For SRAM examination, the static transfer characteristic of triple-fin transistor shows larger SNM than single-fin transistor, as shown in Fig. 6. The triple-fin FinFET exhibits the largest SNM among the explored three structures, where the SNM is calculated from the length of the side of a square having the longest diagonal. The cell ratio and pull-up ratio are assumed to be one in this examination. Fig. 7 presents the random-dopant-induced

SNM fluctuation (σSNM) of the triple-fin devices SRAM cells and the triple-fin FinFETs has the smallest σSNM due to smallest normalized V_{th}, where the normalized σSNM are summarized in the inset table of Fig. 7.

4 CONCLUSIONS

The DC characteristics and dynamic behavior of 16-nm-gate multi-gate-and-multi-fin devices and circuits with different AR have been examined including random-dopant-induced fluctuations. Increase of the fin number and AR is revealed to be favorable for device performance with a view to suppression of SCE and relatively moderate enhancement in current drive. The triple-fin FinFET has exhibited a promising SCE, driving current, timing characteristic, SNM, and fluctuation resistivity than the triple-fin tri-gate and the quasi-planar MOSFET. We are currently studying the optimal fin number and pinch distance among channel fins for the manufacturability of multi-fin FinFETs. In addition, parasitic capacitances of these devices are crucial for advanced multi-gate-and-multi-fin transistor design.

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