Characteristic Optimization of Single- and Double-Gate Tunneling Field Effect Transistors

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ABSTRACT

Optimal single- and double-gate tunneling field-effect transistor (TFET) with a structure of p++ source, intrinsic channel and n+ drain region are explored. Two-dimensional device simulation is adopted to assess device characteristic influenced by the source doping, the channel doping and the thickness of junction overlap between the source and gate. The result of this study shows that the source doping and junction overlap significantly affect the drain current (I_D). Then, we compare the single- and double-gate TFETs with the optimized parameters, where the junction overlap is 6 nm, the source doping is 10^{22} cm^{-3}, and the intrinsic channel doping. For the explored double-gate TFET, a steeper subthreshold slope (SS) of 32 mV/dec and a higher on/off current ratio (I_{on}/I_{off}) of $5x10^9$ are obtained, compared with the single-gate device.

Keywords: Tunneling, Field Effect Transistor, DC characteristic, Subthreshold slop, On/off state current ratio, Optimal parameters, Device simulation

1 INTRODUCTION

For sub-100-nm CMOS technologies and beyond, the devices face fundamental physical limitations [1-2]. For example, the controllability of channel potential is poor, the drain induced barrier lowering (DIBL), and band to band tunneling (BTBT) resulted from the short channel effect are severed; consequently, the off-state current (I_{off}) is high. To maintain low I_{off} and high I_{on} with supply voltage (V_{DD}) reduction is substantial for power management and circuit performance. However, this is limited due to the scaling of threshold voltage (V_{th}). Therefore, silicon-based tunneling field-effect transistors (TFETs) which consist of a gated p-i-n diode have attracted much interest [3-6]. The TFET device exploits the gate-controlled band-to-band tunneling [7-8] mechanism to overcome the fundamental kT/q thermodynamic limit placed on the abruptness of the subthreshold slope (SS) in conventional planar MOSFETs [9]. Although single-gate TFETs possess a low I_{off}, its I_{on} is much lower (about two-order magnitude) than a high-performance MOSFET and could not meet the requirement set in the prediction of ITRS [10]. A double-gate (DG) TFET that boosts I_{on} was reported recently [11]. Diverse approaches have investigated the subthreshold slope and the on/off current ratio (I_{on}/I_{off}) of several kinds of TFETs [12]. Optimization of device characteristics may benefit the TFET technologies.

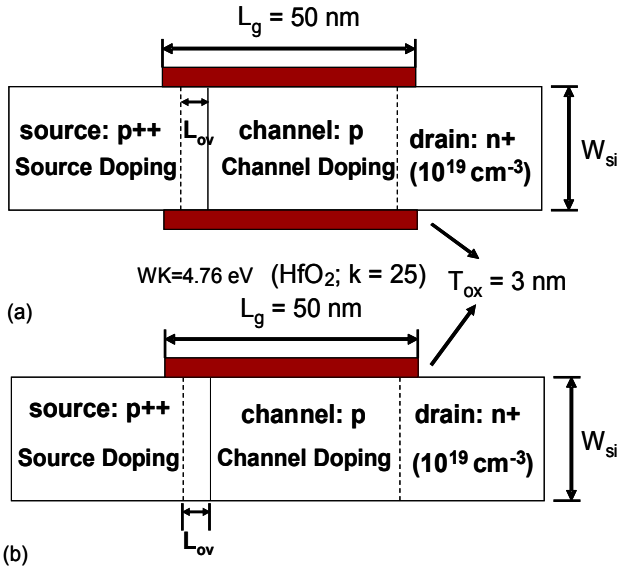

Fig. 1. Schematic of the tested TFET with (a) double-gate and (b) single-gate. For an n-channel transistor, the drain is doped n^+ while source is doped p^{++}. The pn junctions are denoted by dash lines.

In this work, the two-dimensional device simulation is carried out to investigate single- and double-gate Si TFET device characteristics. We for the first time optimize the device performance, such as subthreshold slop and on/off current ratio, by varying the thickness of overlap junction between source and gate (L_{ov}) with a deviation of 6 nm, the source doping concentration from 10^{19} cm^{-3} to 10^{21} cm^{-3} and the channel doping concentration varying from $5x10^{15}$ cm^{-3} (intrinsic) to 10^{18} cm^{-3}; and consequently, the prediction of the advanced structures of TFETs is drawn. For a junction overlap of 6 nm, a source doping concentration of 10^{22} cm^{-3}, and intrinsic channel doping, device shows superior subthreshold slope of 32 mV/dec and the on/off current ratio of $5x10^9$ of a 50 nm double-gate TFET, compared with a single-gate one.

2 DEVICE STRUCTURE AND MODELING

The band-to-band tunneling rate G_{BTBT} is modeled using Kane's model [13] as follows:

$$G_{BTBT} = A\frac{\xi}{E_g^{1/2}}\exp\left(-B\frac{E_g^{3/2}}{\xi}\right), \qquad (1)$$

where ξ and E_g are the electric field and bandgap, respectively. Parameters A and B are functions of carrier effective mass, and for Si, they are $3.5\text{x}10^{21}$ $(\text{eV})^{1/2}/\text{cm s V}^2$ and $22.5\text{x}10^6$ V/cm $(\text{eV})^{3/2}$, respectively. To obtain significant tunneling, there must be a gate-induced band bending such that the thickness of tunneling barrier t (see Fig. 3, for example) is sufficiently small. Moreover, Kane's model has been employed in silicon tunnel FET and has shown a good agreement between simulation and experimental data at both low and high temperature [14]. According to the simulation results, related technologies could be improved for the design and fabrication of high performance TFET. The method for deriving the dependency of tunnel current density on semiconductor properties could be returned to [15]; using a triangular barrier Wentzel–Kramers–Brillouin (WKB) approximation [16], we have an expression for the current density [17]:

$$J = \frac{q^3\xi V_R}{4\pi^2\hbar^2}\sqrt{\frac{m^*}{2E_G}}\exp\left(-\frac{4\sqrt{2m^*E_G^{3/2}}}{3q\xi\hbar}\right) \qquad (2)$$

By simultaneously integrating the developed numerical device simulation and Eq. (2), the TFET performance could be boosted. Figures 1(a) and 1(b) illustrate the *n*-channel single-gate and double-gate structures. The devices have a gate length of 50 nm and a 3 nm HfO_2 high-κ gate dielectric. The Si film thickness W_{si} is equal to 10 nm. The doping concentration of 10^{19} cm^{-3} for the drain region are assumed and the channel is *p*-type doped with a concentration of $5\text{x}10^{16}$ cm^{-3}. The junction overlap between the source and gate is defined as L_{ov} of 5 nm.

3 RESULTS AND DISCUSSION

Figures 2(a)-(b) are the on/off current ratio and the subthreshold slope as a function of the source doping concentration for single- and double-gate TFET at V_{gs} = 1.2V and V_{ds} = 1.2V. The result shows that the device characteristics improved as the source doping concentration increased. The reason is that as the source doping increased from $1\text{x}10^{19}$ cm^{-3} (black solid line) to $1\text{x}10^{20}$ cm^{-3} (red dash line) and fixed the channel doping concentration, the thickness of overlap junction and the silicon film thickness,

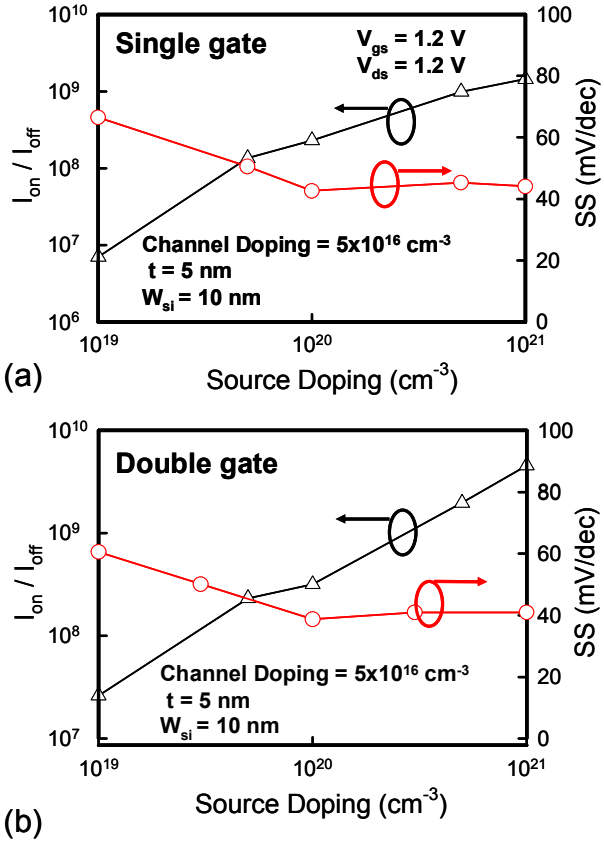

Fig. 2. The On/off current ratio (black line) and the subthreshold slope (red line) as a function of source doping concentration for (a) single-gate and (b) double-gate TFETs, respectively.

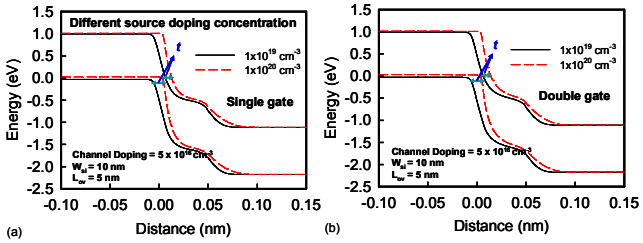

Fig. 3. The energy band diagrams along the source to channel direction near surface with different source doping concentration for (a) single-gate and (b) double-gate TFETs, respectively. The black solid line indicates source doping concentration of $1\text{x}10^{19}$ cm^{-3} and red dash line is source doping concentration of $1\text{x}10^{20}$ cm^{-3}.

the thickness of tunneling barrier t is significantly decreased, and thus increase tunneling probability, as shown in Fig. 3. As a result, the on-state current is increased and the SS is reduced at heavily source doping for both structures. However, the current ratio and SS show small discrepant of studied structures with different channel doping concentration, as shown in Fig. 4. It is because of

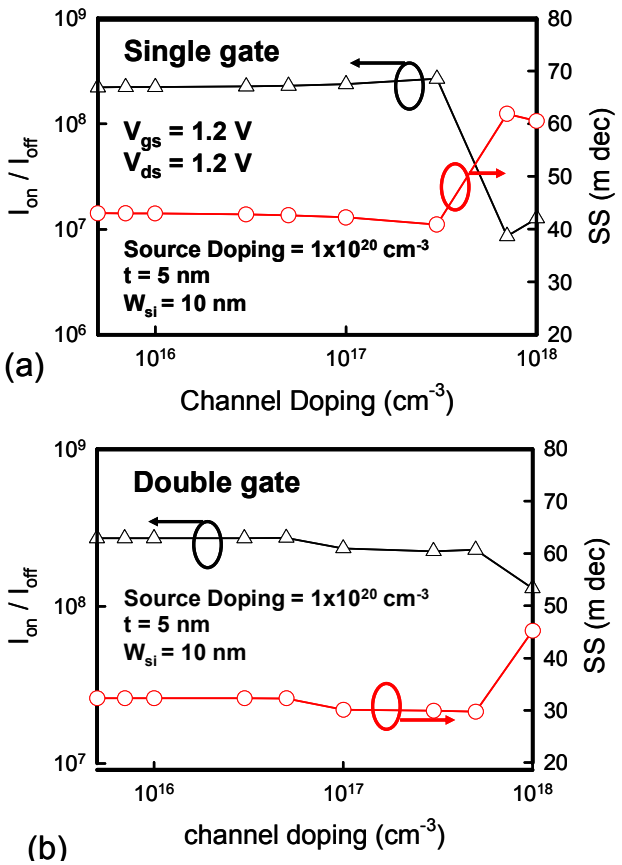

Fig. 4. The On/off current ratio (black line) and subthreshold slope (red line) as a function of channel doping concentration for (a) single-gate and (b) double-gate TFETs, respectively.

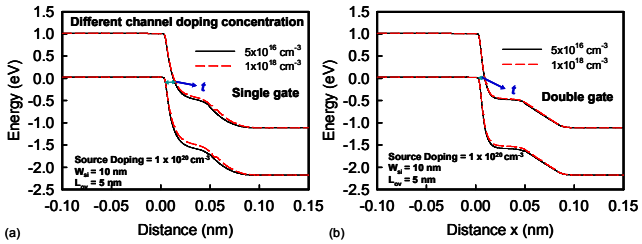

Fig. 5. The energy band diagrams along the source to channel direction near surface with different channel doping concentration for (a) single-gate and (b) double-gate TFETs, respectively. The black solid line indicates channel doping concentration of 5x10^{16} cm^{-3} and red dash line is channel doping concentration of 1x10^{18} cm^{-3}.

the thicknesses of tunneling barrier *t* are quite equal while the channel doping concentration increasing form 5x10^{16} cm^{-3} (black solid line) to 1x10^{18} cm^{-3} (red dash line), as displayed in Fig. 5. Notably, in Figs. 5(a)-(b), the *t* of double-gate TFET is smaller than that of single-gate and

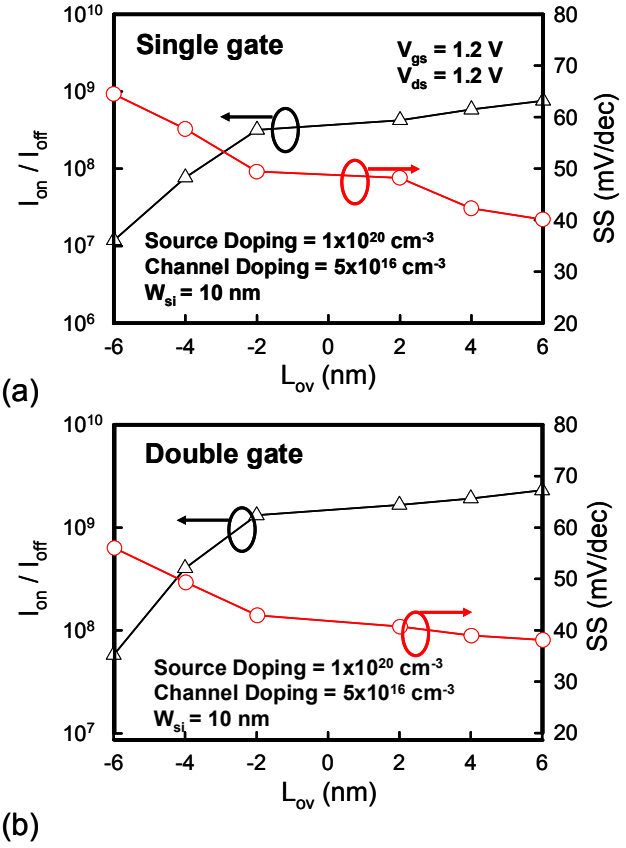

Fig. 6. The On/off current ratio (black line) and subthreshold slope (red line) as a function of junction overlap for (a) single-gate and (b) double-gate TFETs, respectively.

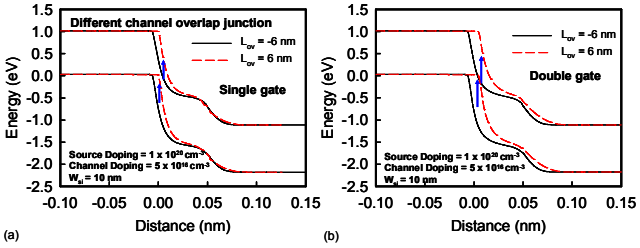

Fig. 7. The energy band diagrams along the source to channel direction near surface with different L_{ov} for (a) single-gate and (b) double-gate TFETs, respectively. The black solid line indicates L_{ov} of -6 nm and red dash line is L_{ov} of 6 nm.

results in larger current ratio and smaller SS of double-gate structure. The current ratio and SS result from L_{ov} for single- and double-gate are further explored in Fig. 6. As the L_{ov} increased, the device performance improved due to the junction moves closer to the gate edge, the energy band becomes increasingly influenced by the gate field and built-in potential barrier is lowered, as shown in Fig. 7. Figure 8

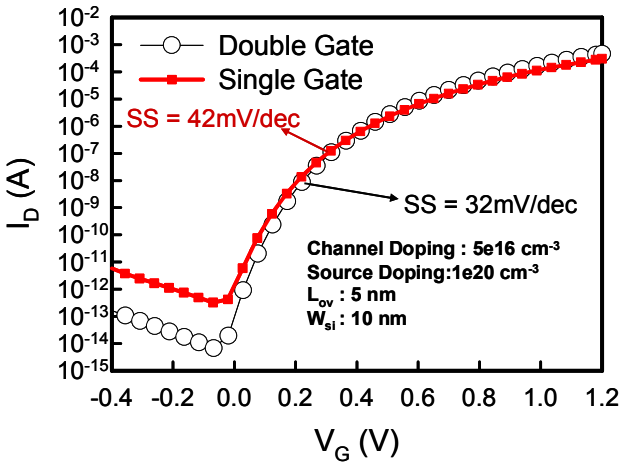

Fig. 8. The optimized I_D-V_G characteristics comparison of the single- and double-gate TFETs.

shows optimized I_D-V_G characteristics comparison of the examined single-gate and double-gate structures. The double-gate TFET has the higher on/off current ratio with $5x10^9$ and lower SS with 32mV/dec, compared with the results of single-gate one due to better gate controllability. Such characteristics could be considered for device structure design optimization for Si TFETs.

4 CONCLUSIONS

The device performance such as SS and current ratio have been optimized by varying the device parameters, source doping concentration, channel doping concentration and L_{ov}. The simulation results of this study have shown that the device with heavier source doping and shorter effective channel length lead to interesting device performance of single- and double-gate TFETs. Moreover, the double-gate TFETs show superior on/off current ratio and SS than those of single-gate TFETs. We are currently extending this study to include more designing and material parameters for high-performance TFET devices in low power ICs.

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