Enhancement of Defect Tolerance in the QCA-based Programmable Logic Array (PLA)

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ABSTRACT

Improved layout of QCA(quantum-dot cellular automata)-based PLA (programmable logic array) that enhance the defect tolerance is proposed, in order to develop next generation circuit technology that replace the conventional CMOS technology. We analyze which QCA device (quantum-dot cell) limits the defect tolerance of the AND/OR plane cell of the QCA-PLA by using QCA circuit simulator or QCADesigner. It is assumed that there is single defect in the circuit and the defect model is shift of a QCA device. The result shows that coplanar crossing limits the defect tolerance. Several layouts that possibly improve the defect tolerance are studied. Triple-redundant configuration of the wire shows the best result. We implemented the both AND plane and OR plane with the improved AND/OR plane cell and evaluated the PLA. Here, multiple defects are assumed. Our improved layout shows significant enhancement of the defect tolerance.

Keywords: QCA, PLA, coplanar-crossing, triple-redundancy, defect tolerance

1 INTRODUCTION

CMOS technology faces serious challenges due to the fundamental physical limits such as ultra-thin gate oxides and doping fluctuations in nanoscale era. Different devices that might either replace or augment CMOS technology are required. The work presented here looks at the quantum-dot cellular automata (QCA) device architecture [1] – and more specifically a programmable logic array (PLA) architecture realized with QCA devices.

The QCA is one of the alternative device candidates that attract considerable attention [1]. QCA circuits could potentially achieve logical operations and data transfer with higher clock frequency and/or with lower power dissipation than conventional CMOS circuits. Several implementations of the QCA have been proposed: the metal-dot QCA [2], [3], the molecular QCA [4], and the magnetic QCA [5].

The PLA is a reconfigurable system-level architecture. A programmable memory device and a few logical gates are duplicated and arranged in an array manner. The circuit function can be reconfigured after the chip has been fabricated and assembled. Not only the MOS-based PLA but Also the QCA-based PLA have been proposed [6]. The PLA architecture makes it easy to implement circuit functions and enables us to repair malfunction caused by defects.

One of the most critical issues in nano-scale devices such as the QCA will be defect tolerance. Defect tolerance in the QCA-based PLA has been discussed and a logic mapping technique has been proposed in order to improve the tolerance [7]. However any methods to improve defect tolerance of the QCA-based PLA AND/OR plane cell itself has not been discussed to our knowledge. In this paper we analyze the conventional AND/OR plane cell and propose a modified layout that has better defect tolerance.

2 BACKGROUND

2.1 Quantum-Dot Cellular Automata (QCA)

A QCA device can consist of 2 or 4 quantum dots. A 4-quantum-dot QCA device is shown in Fig. 1(a). Diagonal 2 dots are occupied by electrons in the 4-quantum-dot QCA device. As is shown in Fig. 1(b), two charge configurations correspond to the logic value 0 and 1, respectively. QCA circuits are composed by arranging QCA devices. Basic circuit elements are shown in the rest of Fig. 1. Fig. 1(c) shows a wire that transfer signals. Fig. 1(d) is a inverter-chain in which logic value is toggled step-by-step. A 3-input and 1-output majority voter (MV) is shown in Fig. 1 (e). A 2-input AND/OR gate can be made by setting one input of an MV to 0/1, respectively. Figures 1 (f) and (g) show crossings. Methods to implement multilevel crossing of wires have not been proposed yet. Therefore, coplanar crossings are used. In this paper, we refer to these crossings as "type-A" (Fig.1 (f)) and "type-B" (Fig. 1 (g)) crossing, respectively. In the QCA circuit, the direction of signal propagation is controlled by clocking scheme [8].

2.2 QCA-PLA

Structure of the QCA-PLA is shown in Fig. 2. As is shown in Fig. 2 (a), same as the MOS-based PLA, the QCA-PLA contains two planes: AND plane and OR plane. These planes are arrays of AND/OR plane cells. Layout of the AND plane cell is shown in Fig. 2(b). Layout of the OR plane cell is very similar to that of the AND plane cell, except the layout is flipped. The AND/OR plane cell contains wires, an inverter-chain, a coplanar-crossing, an AND gate, an OR gate, and a programmable memory element. The value of the

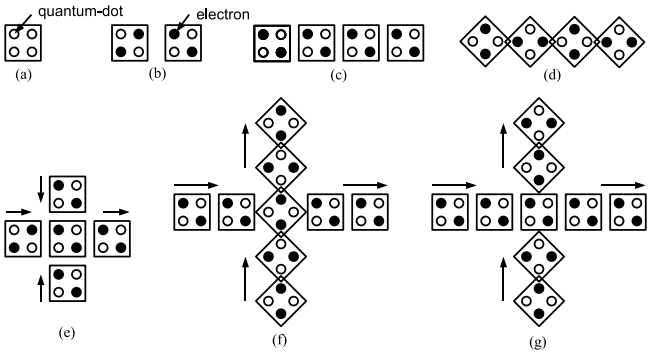

Figure 1: QCA device and basic circuit elements

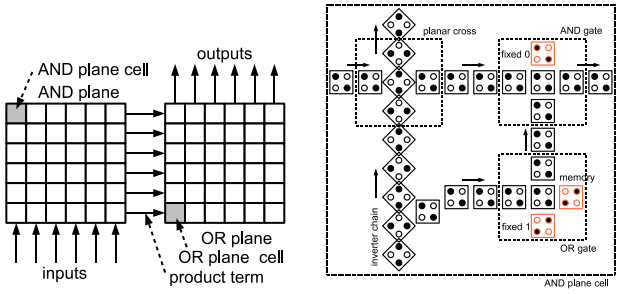

Figure 2: QCA-based PLA

programmable memory element is fixed in the normal operation mode, while an arbitrary value is written into the element in the programming mode. The operation mode is controlled by the clocking.

3 Evaluation of the conventional PLA AND/OR plane cell

We analyzed which QCA device (quantum-dot cell) limits the defect tolerance of the conventional AND/OR plane cell [6]. We modified the "QCADesigner" software [9] to compare output logic signals between the defect-less circuit and that with a defect, then simulated behavior of the conventional AND/OR plane cell. Considered defect model is the shifted device (a deviation of a QCA device from the ideal device in terms of location) and single defect is assumed here. One defective QCA device is selected exhaustively from the layout. Then, the amount of the device shift was set at 21 steps ranging from -2nm to 2nm in X-direction and Y-direction, respectively. The simulated result is shown in Fig. 3. In this figure, a box with solid black line corresponds to one QCA device and there are 21×21 pixels in the box. The color of a pixel shows whether all logic signals on the output terminals are good or not. Cyan pixels show good outputs and red pixels show faulty ones. The center pixel in a box corresponds to the defect-less circuit so that the center pixel is always colored cyan. The displacement from the center of a box shows amount of shift of the corresponding device. From the Fig. 3, we found that the crossing-point of

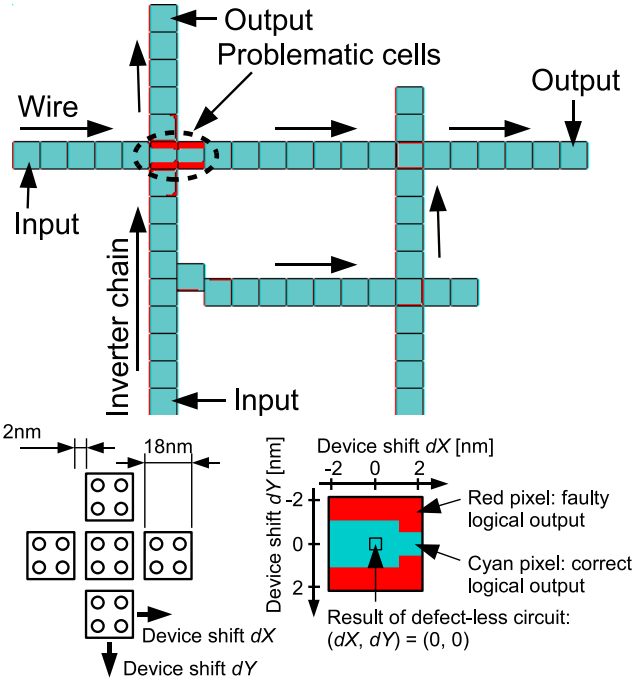

Figure 3: Simulated Result of the conventional AND/OR plane cell

a wire and an inverter-chain causes degradation of the defect tolerance.

4 Improvement of AND/OR plane cell layout

In order to improve defect tolerance of the PLA AND/OR plane cell, We tried alternative layouts by means of selecting circuits elements from the following selections:

- either a type-A or type-B crossing,
- either a thick wire/inverter-chain or triple-redundant wires/inverter-chains at the crossing point.

One of the layouts is shown in Fig. 4. In this layout, triple-redundant wires and a type-A crossing are selected. The modified layouts are evaluated in the same way mentioned in the previous section. A normal wire/inverter-chain is also evaluated for the sake of comparison. The results are shown in Fig. 5. Correspondence between figures in Fig. 5 and the circuit-element selections are listed in Table 1. From these results, we found that triple-redundant wires and a type-A crossing, Fig. 5 (e), shows best defect tolerance.

5 Evaluation

We evaluated the defect tolerance of the QCA-based PLA with the conventional AND/OR plane cells and that with the proposed cells. As is shown in Fig. 6, the PLA have a 3×3 AND plane and a 3×1 OR plane. Multiple faults are assumed here. The simulated result is shown in Fig. 7. Figure 7 (a) shows defect tolerance of the PLA with conventional

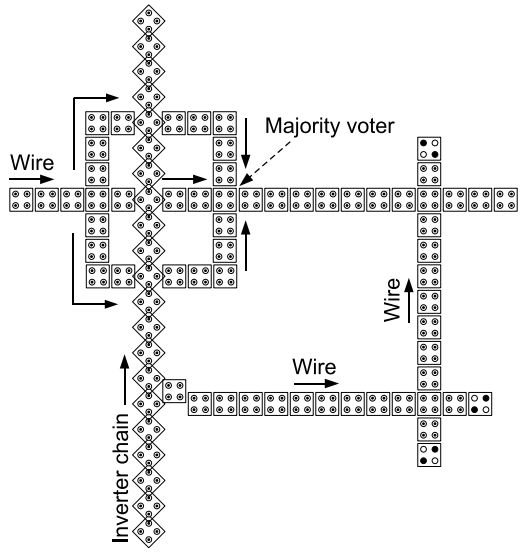

Figure 4: Improved AND/OR plane cell layout

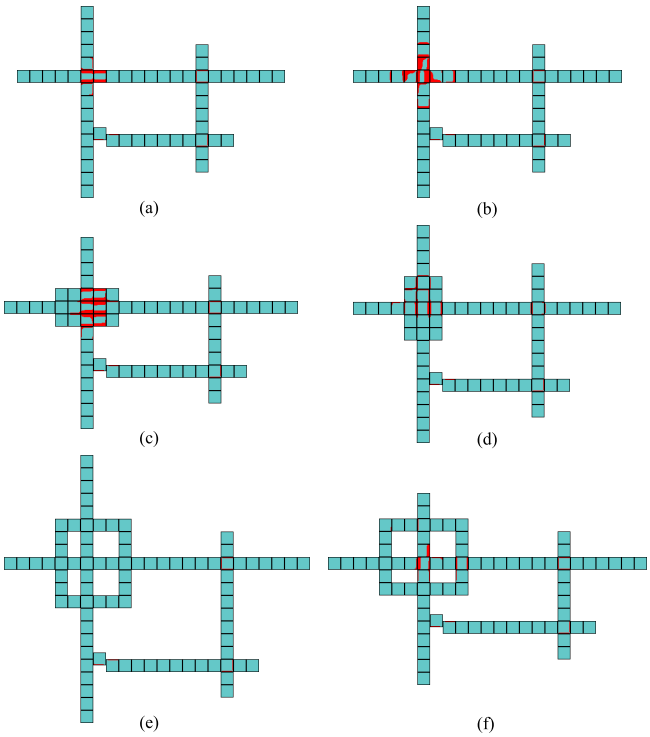

Figure 5: Results of defect tolerance evaluation

cells and Fig. 7 (b) shows that with proposed cells. In these figures, the X, Y, and Z axes show the defect rate, device shift, and the probability of correct outputs. Locations of devices where defects are injected and the direction of device shift are decided by uniformly distributed random numbers. Line profiles where the defect rate is 2 % and the device shift is 1nm are shown in Fig. 8 (a) and (b), respectively. These figures show that our PLA have better defect tolerance.

Table 1: Correspondence between Fig. 5 and circuit-element selections

wire/inverter-chain type	crossing type	
	type-A	type-B
normal	Fig. 5(a)	Fig. 5(b)
thick	Fig. 5(c)	Fig. 5(d)
triple-redundant	Fig. 5(e)	Fig. 5(f)

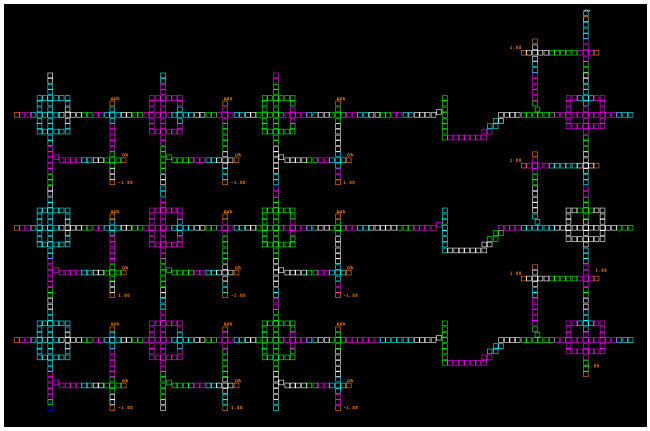

Figure 6: Layout of the improved QCA-PLA

6 Conclusions

Improved layout of QCA(quantum-dot cellular automata)-based PLA (programmable logic array) that enhance the defect tolerance was proposed, in order to develop next generation circuit technology that replace the conventional CMOS technology. We analyzed which QCA device (quantum-dot cell) limits the defect tolerance of the AND/OR plane cell of the QCA-PLA by using QCA circuit simulator or QCADesigner. It was assumed that there is single defect in the circuit and the defect model is shift of a QCA device. The result showed that coplanar crossing limits the defect tolerance. Several layouts that possibly improve the defect tolerance were studied. Triple-redundant configuration of the wire showed the best result. We implemented the both AND plane and OR plane with the improved AND/OR plane cell and evaluated the PLA. Here, multiple defects were assumed. Our improved layout showed significant enhancement of the defect tolerance.

REFERENCES

[1] F. Lombardi, and J. Huang, eds., *Design and test of digital circuits by quantum-dot cellular automata*, Artech House, 2008.

[2] I. Amlani, A. Orlov, G. Snider, C. Lent, and G. Bernstein, "Demonstration of a six-dot quantum cellular automata system," *Applied Physics Letters*, vol.72, no.17, pp.2179-2181, 1998.

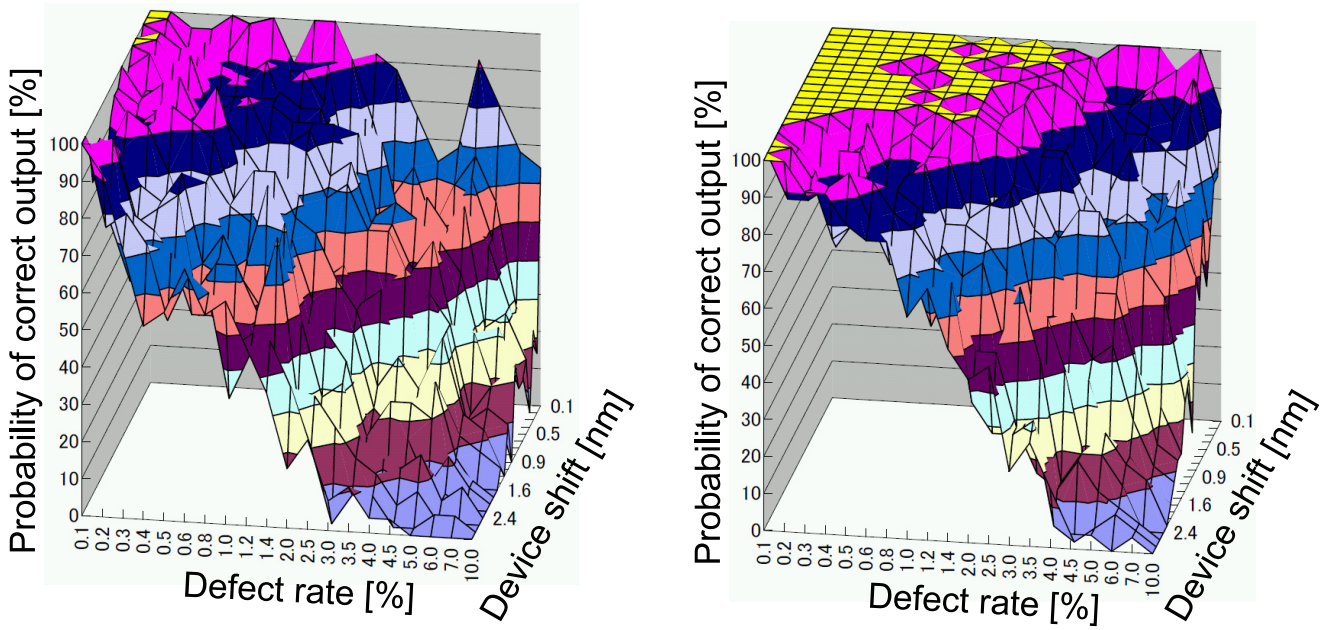

Figure 7: Simulated result: probability of correct output versus defect rate and device shift: (a) conventional PLA, (b) proposed PLA.

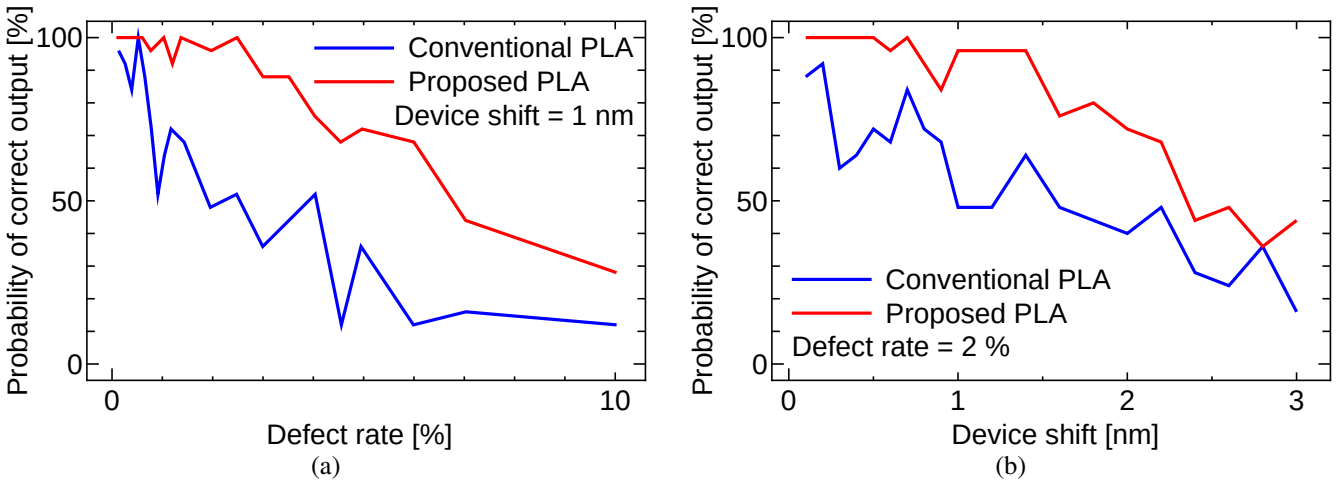

Figure 8: Line profiles of Fig. 3: (a) device shift=1nm, (b) defect rate=2%.

[3] A. Orlov, I. Amlani, G. Bernstein, C. Lent, and G. Snider, "Realization of a functional cell for quantum-dot cellular automata," *Science*, vol.277, no.5328, pp.928-930, 1997.

[4] M. Lieberman, S. Chellamma, B. Varughese, Y. Wang, C. Lent, G. Bernstein, G. Snider, and F. Peiris, "Quantum-dot cellular automata at a molecular scale," *Analysis of the New York Academy of Sciences*, vol.960, pp.225–239, 2006.

[5] R. Cowburn, and M. Welland, "Room temperature magnetic quantum cellular automata," *Science*, vol.287, no.5457, pp.1466-1468, 2000.

[6] M. Crocker, X.S. Hu, M. Niemier, M. Yan, and G. Bernstein, "PLAs in quantum-dot cellular automata", *IEEE Trans. Nanotechnology*, vol. 7, no. 3, pp. 376–386, 2008.

[7] M. Crocker, X.S. Hu, and M. Niemier, "Defect tolerance in QCA-based PLAs", in *Proc. IEEE International Symposium on Nanoscale Architectures*. 2008, pp. 46–53.

[8] K. Hennessy, and C. Lent, "Clocking of molecular quantum-dot cellular automata," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol.19, pp.1752-1755, 2001.

[9] K. Walus, V. Dimitrov, G. A. Jullien, and W. C. Miller, "QCADesigner: A CAD tool for an emerging nanotechnology", in *Micronet Annual Workshop*, 2003.