Synthesis and Charging Properties of Cobalt-Based Nanoparticles in Silicon Dioxide

Jong-Hwan Yoon

Department of Physics, College of Natural Sciences, Kangwon National University, Chuncheon, Gangwon-do 200-701, Korea, jhyoon@kangwon.ac.kr

ABSTRACT

Cobalt silicide (CoSi) nanocrystal (NC) layer distributed within narrow spatial region is synthesized by thermal annealing of a sandwich structure comprised of a thin cobalt (Co) film sandwiched between two silicon-rich oxide (SiO_x) layers. It is shown that the size of the CoSi NCs can be controlled by varying the Co film thickness and Si concentration, an increase in the size with increasing thickness and concentration. Capacitance-voltage (*C-V*) measurements on a test metal/oxide/semiconductor (MOS) structure with floating gate based on CoSi NCs of 3.8 nm in diameter and 1.4×10^{12} cm^{-2} in density are shown to have *C-V* characteristics suitable for nonvolatile memory applications, including a large *C-V* memory window of about 10 V for sweep voltages between -15 V and +8.

Keywords: cobalt silicide nanoparticles, nonvolatile memory

1 INTRODUCTION

Recently, there have been considerable research efforts devoted to realizing nonvolatile memory (NVM) devices with smaller size, faster operating speed and larger storage capacity. One approach to realize such NVM devices is to use a floating-gate transistor which consists of discrete charge traps instead of a continuous conducting layer used in many conventional devices [1]. The memory devices with floating gate based on discrete charge traps offer particular advantages over conventional floating gate structures, including the fact that charges trapped at discrete sites are more stable than in a conventional conductive floating gate for lateral leakage path in the gate oxide. This improvement in the stability of charges trapped at floating gate makes it possible that devices can be scaled to smaller dimensions by reducing the tunnel oxide layer thickness.

Various discrete-charge traps, such as semiconducting [2 - 5] and pure metal nanocrystals [6 - 9], have been studied for possible applications to NVM devices. In particular, recent works [10, 11] have demonstrated that metal nanocrystals have additional advantages compared to those of semiconducting nanocrystals, namely, an enhancement in the charge storage capacity and retention time due to a higher density of states near Fermi level and a higher work function, respectively. On the other hand, as metal silicides [12, 13] have physical properties similar to those of pure metals they have also received particular attention.

In this work, we report the direct growth of cobalt silicide (CoSi) nanocrystals, which are metallic material with a work function of about 4.7 eV [13], by thermal annealing of a simple sandwich structure consisting of an ultra thin Co layer sandwiched between two silicon-rich oxide (SiO_x) layers. It is observed that CoSi NCs grow into well-defined boundaries and approximately spherical shape within the SiO_2 matrix, increasing with Co film thickness. The MOS structures with floating gate based on CoSi NCs produced by this method are shown to have *C-V* characteristics suitable for nonvolatile memory applications.

2 EXPERIMENTAL DETALS

CoSi NCs were formed by thermally annealing a sandwich structure comprised of a thin Co film sandwiched between two silicon-rich oxide (SiO_x) layers, as depicted in Fig. 1. SiO_x layers were produced by plasma-enhanced chemical vapor deposition (PECVD) at a substrate temperature of 300 ^oC using fixed flow rates of SiH_4 and N_2O, and ultra-thin Co layer was prepared by conventional thermal evaporation. The sandwich structures were formed by alternate deposition of SiO_x and Co layers on (100) oriented *p*-type silicon wafers as required. Nucleation and growth of CoSi NCs were achieved by thermal annealing of the sandwich structures at elevated temperature in a quartz-tube furnace using high purity nitrogen gas (99.999 %) as an ambient.

The microstructure of CoSi NCs was investigated by transmission electron microscopy (TEM) using a JEOL JEM 2010 instrument operating at 200 kV. The chemical composition of NCs was analyzed by energy dispersive X-ray spectroscopy (EDS) using an energy dispersive spectrometer attached to the TEM instrument.

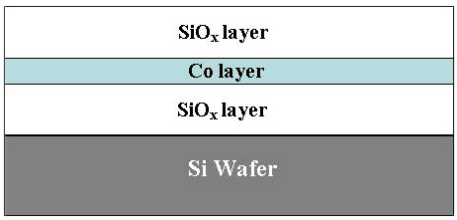

Figure 1: Schematic of layered sample structure for the formation of cobalt-based nanoparticles.

For the EDS analysis, the electron beam was focused to a spot as small as 1.5 nm in size. The MOS capacitors for memory properties were fabricated by evaporating Al through a mask with circular holes of area 0.03 mm^2 as a control electrode. Capacitance-voltage (*C-V*) measurements on the MOS capacitors were performed at 300 K using a Keithley 590 capacitance meter (1 MHz frequency) and a Keithley 230 programmable voltage source.

3 RESULTS AND DISCUSSION

First, the formation of CoSi nanoparticles using the layered structures shown in Fig. 1 was examined. Figure 2 shows a representative cross-sectional transmission electron microscopic (XTEM) image, which was taken for a layered structure comprised of Co film of 0.2 nm thickness sandwiched between two $SiO_{1.67}$ layers of 5 nm after annealing at 650 ^oC for 1 h. The XTEM image clearly shows the presence of nanoparticles with well-defined boundaries and approximately spherical shape. Especially, the image shows that the spatial distribution of the nanoparticles is much narrow, thereby demonstrating the efficacy of the technique for making nanocrystal floating gate structures for nonvolatile memory devices. In the present case, the average diameter of the nanoparticles is about 3.0 nm with standard deviation of 0.47 nm.

To identify exact phase of the Co-based nanoparticles shown in Fig. 2, energy dispersive x-ray spectroscopy (EDS) was performed on each individual nanoparticles. Figures 3(a) and (b) present representative EDS spectra obtained outside and inside nanoparticles, respectively. As seen in Figure 3, little or no Co is observed outside of nanoparticle but it is clear that the nanoparticles contain Si and Co atoms, supporting the premise that they are cobalt silicide particles. The Co-based nanoparticles shown in Fig. 2 were formed by annealing at a temperature of 650 ^oC where they are expected to be at a stable phase [14]. Furthermore, the high-magnification TEM image of nanoparticles shown in Fig. 5(b) reveals a regular lattice structure consistent with it being a single crystal phase. These results demonstrate the fact that the nanoparticles are cobalt silicide (CoSi) nanocrystals (NCs).

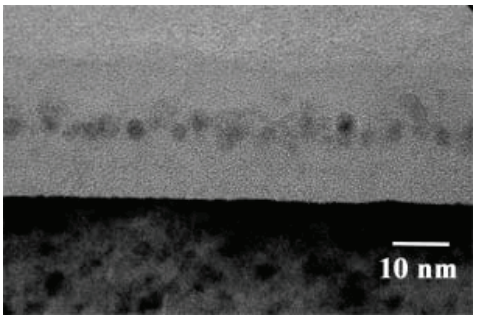

Figure 2: Cross-sectional transmission electron microscope image of the sandwich structure of $SiO_{1.67}$/Co/ $SiO_{1.67}$ after annealing for 1 h at 650 ^oC.

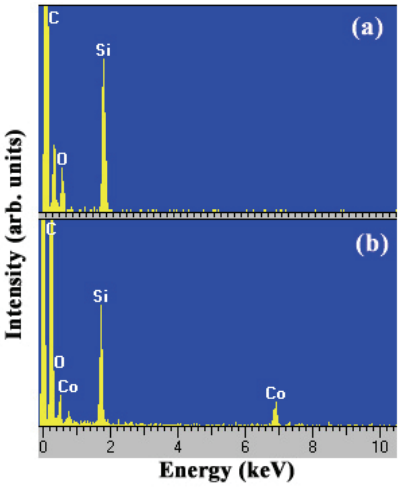

Figure 3: EDS spectra taken (a) outside and (b) inside of Co-based nanoparticle shown in Fig. 2. Note that no Co signal is observed outside of the nanocrystals.

Figure 3 shows cross-sectional transmission electron microscopic images of a layered structure with different Co thickness. The layered structure was comprised of Co films (0.2 nm, 0.5 nm, and 0.8 nm in thickness) sandwiched between two $SiO_{1.51}$ layers after annealing at 650 ^oC for 2 h. The image also shows the presence of NCs distributed within narrow spatial region. Furthermore, it is clear from the image that the size of the NCs increases as Co layer is thickened. The mean diameters estimated for 0.2 nm, 0.5 nm, and 0.6 nm Co thicknesses were about 2.2 nm, 2.9 nm, and 4.7 nm, respectively. In the case of 0.2 nm thickness, in particular, the diameter is smaller than that in the case shown in Fig. 2 despite the same Co thickness. This fact demonstrates that the size of CoSi NCs is also associated with concentration of Si atoms.

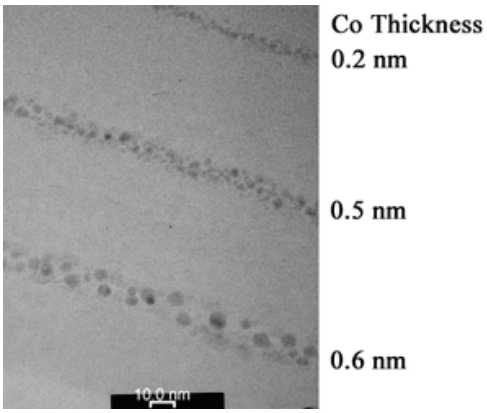

Figure 4: Cross-sectional transmission electron microscope image of $SiO_{1.51}$ layer embedded Co layers with different thickness after annealing at 650 ^oC for 2 h.

In order to explore the potential of CoSi nanocrystal floating gates for memory applications, a well-controlled metal/oxide/semiconductor (MOS) sample containing CoSi NCs between tunnel and control oxide layers was prepared for capacitance-voltage (*C-V*) measurements. The MOS structure with CoSi NCs was formed with the following layers: tunnel $SiO_2/SiO_{1.51}$/Co/$SiO_{1.51}$/control SiO_2. The thickness of tunnel and control oxide layer was 5 nm and 7 nm, respectively, and the thickness of $SiO_{1.51}$ and Co layer was 3.5 nm and 0.6 nm, respectively. This structure was subsequently annealed at 650 ^oC for 2 h to form CoSi NCs, with the resulting microstructure shown in Figure 5, which represents the XTEM images of the sample after annealing. Figure 5(a) and (b) show the overall and high-magnification images, respectively. These images clearly show the formation of well-defined CoSi NC monolayer distributed within the narrow region, and the regular lattice structure consistent with it being a single crystal phase [Fig. 5(b)]. The average size and areal density of the CoSi NCs are about 3.8 nm and 1.4×10^{12} cm^{-2}, respectively. The size is smaller than that for 0.6 nm Co thickness shown in Fig. 4. The difference might be likely to result from a smaller concentration of Si atoms due to the relatively thinner layer of SiO_x in the case of Fig. 5. The MOS capacitors for *C-V* characteristics were fabricated by evaporating Al gate electrodes on the control oxide layer.

Figures 6(a) and (b) show the *C-V* curves measured for the MOS capacitors without and with NCs, respectively. The MOS capacitors without NCs were also fabricated with the same layer structure as the case with CoSi NCs except for the absence of Co layer. The gate voltage was swept from accumulation region (-15 V) to inversion region (8 V) before being swept back from inversion (8V) to accumulation (-15V). As seen in Fig. 6, there is clearly a distinct difference in the memory window for the two cases.

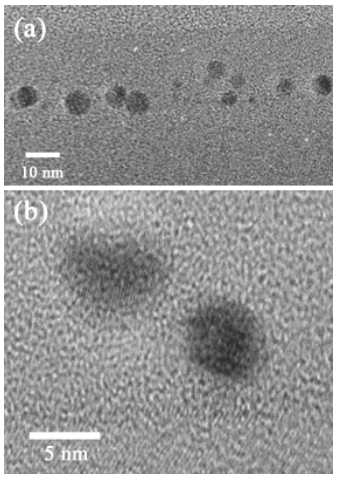

Figure 5: (a) High-resolution cross-sectional TEM images of a sample prepared using a $SiO_2/SiO_{1.51}$/Co /$SiO_{1.51}/SiO_2$ structure with a Co film of 0.6 nm thickness, and (b) the high-magnification TEM image of the CoSi NCs, showing regular lattice structure.

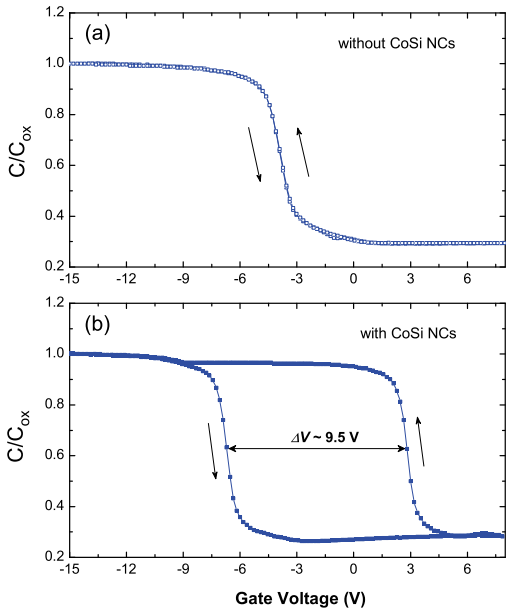

Figure 6: *C-V* hysteresis loops of MOS capacitors a) without, and b) with CoSi nanocrystals.

The MOS capacitor with CoSi NCs exhibits large memory window of approximately 10 V, while the MOS capacitor without CoSi NCs does not reveal significant memory window. This difference demonstrates that the large memory window is closely associated with the presence of the CoSi NCs. The width of *C-V* hysteresis loop, i.e., memory window, is due to the charge (Q) trapped at NCs, increasing the memory window with increasing the charge trapped at the NCs. In the case of metallic NCs, because of a high density of states near the Fermi level, several electrons per NC can be trapped [10]. We can estimate the average number, n, of electrons trapped at a CoSi NC by using the simple relation $n=(\Delta V_{FB}\cdot C_{acc})/(en_0S)$, where ΔV_{FB} is the flat band voltage shift due to the electron charge trapped at NCs, C_{acc} is the accumulation region capacitance, n_0 is the areal density of NCs, e is the electron charge, and S is the gate electrode area. At a gate voltage of +8 V, which causes a fully electron charged state of the NC, ΔV_{FB}=4.5 V and C_{OX}= 35 pF, $n_0=1.4\times10^{12}$ cm^{-2}, and S=0.03 mm^2, so that for the sample shown in Fig. 4 the number of electrons (n) trapped in each NC is about 2.4. This value is a little bit smaller than those reported by others [6]. The difference is likely to be due to the difference in either the work function or size of NCs. As a consequence, the large memory window of the MOS capacitor with CoSi NC floating gate, as shown in Fig. 6(b), is thus attributed to a large number of electrons trapped per NC due to the metallic properties of the CoSi NCs.

4 SUMMARY

A simple method for fabricating metallic cobalt silicide (CoSi) nanocrystals (NCs) with narrow spatial distribution has been demonstrated and shown to produce structures for nonvolatile memory applications. The method is to form CoSi NCs by thermally annealing a simple sandwich structure consisting of an ultrathin cobalt (Co) layer sandwiched between two silicon-rich oxide (SiO_x) layers, The CoSi NC size is shown to be controlled by thickness of Co layer and Si concentration in SiO_x. Capacitance-voltage (*C-V*) measurements on the test metal/oxide/semiconductor capacitor based on CoSi nanocrystal floating gate with average diameter of 3.8 nm and areal density of 1.4×10^{12} cm^{-2} in density are shown to have *C-V* characteristics suitable for future nonvolatile memory applications, including a large memory window of 10 V for sweep voltages between -15 V and +8 V.

ACKNOWLEDGEMENT

This work was supported by the Korea Research Foundation Grant funded by the Korean Government (MOEHRD, Basic Research Promotion Fund, KRF-2008-313-C00303).

REFERENCES

[1] D. Kahng and S. M. J. Sze, Bell Syst. Tech. 46**,** 1283, 1967.

[2] S. Tiwari, F. Rana, K. Chan, H. Hanafi, A. Hartstein, E. F. Crabbe, and K. Chan, Appl. Phys. Lett. 68, 1377, 1996.

[3] Y. Shi, K. Saito, H. Ishikuro, and T, Hiramoto, J. Appl. Phys. 84**,** 2358, 1998.

[4] S. H. Hong, M. C. Kim, P. S. Jeong, S. H. Choi, Y. S. Kim, and K. J. Kim, Appl. Phys. Lett. 92**,** 093124, 2008.

[5] T. Z. Lu, M. Alexe, R. Scholz, V. Talelaev, and M. Zacharias, Appl. Phys. Lett. 87**,** 202110, 2005.

[6] C. Lee, J. Meteer, V. Narayanan, and E. Kan, J. Electron Meter. 34, 1, 2005.

[7] S. K. Samanta, W. J. Yoo, and G. Samudra, Appl. Phys. Lett. 87**,** 113110, 2005.

[8] D. Zhao, Y. Zhu, and J. Liu, Solid State Electronics 50, 268, 2006.

[9] D. U. Lee, M. S. Lee, J. H. Kim, and E. K. Kim, Appl. Phys. Lett. 90**,** 093514, 2007.

[10] Z. Liu, C. Lee, V. Narayanan, C. Pei, and E. C. Kan, IEEE Trans. Electron Dev. 49**,** 1606, 2002.

[11] Z. Liu, C. Lee, V. Narayanan, C. Pei, and E. C. Kan, IEEE Trans. Electron Dev. 49**,** 1614, 2002.

[12] J. Yuan, G. Z. Pan, Y. L. Chao, and J. C. S. Woo, Mater. Res. Soc. Proc. 824, B7.11.1, 2005.

[13] E. M. Gullikson, A. P. Mills, and J. M. Phillips, Surface Science 195, L150, 1989.

[14] H. Miura, E. Ma, and C. V. Thompson, J. Appl. Phys. 70, 4287, 1991.