1/*f* Noise Model for Double-Gate FinFETs Biased in Weak Inversion

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ABSTRACT

An approach to model 1/*f* noise in the weak inversion range of symmetrical double-gate FinFETs is proposed, based on Hooge's theory (mobility fluctuation model). Starting from conduction equations in the subthreshold regime, a method to evaluate the total number of carriers under the gate is presented and allows us to deduce the Hooge parameter α_H. This model is applied to FinFETs of different fin widths, with the proposed model, the unique value of α_H is obtained in weak inversion.

Keywords: 1/*f* noise, FinFET, volume inversion

1 INTRODUCTION

Low frequency noise (LFN) is an important parameter for analog and RF applications. For example, LFN in MOS devices is up-converted to oscillator phase noise, degrading system performance [1]. While recently high performance nanoscale FinFET, which has a double-gate straddling a silicon fin, is a very attractive solution for ultra-scaled CMOS technologies at the 45nm node and beyond. The advantages by using FinFET technology are mainly improved drive current, better control of the short channel effect and reduced drain-induced-barrier-lowering [2]-[4]. This paper concerns the study of the 1/*f* noise of double-gate FinFETs in weak inversion. Generally, in this regime, for bulk nMOS transistors, experimental results show a quadratic variation versus drain current and can be modeled following McWhorter theory (number fluctuation model) [5]. However, the aim of this paper is to analyze 1/*f* noise following Hooge's theory (mobility fluctuation model) [6][7] in weak inversion due to different current conduction behavior of FinFET devices compared to bulk transistors in this regime.

2 MODEL EQUATIONS

In the subthreshold region, current conduction behavior in the FinFET is very different from that in the bulk transistor. In the subthreshold region of a lightly-doped symmetrical double-gate FinFET, both the total inversion charge and drain current are proportional to the fin width for a given bias condition, and volume inversion takes place [8][9]. The carrier charges flow through the whole silicon channel body and, thus, can be considered as 'bulk conduction' compared with the 'surface-conduction' in bulk-CMOS transistors. The interaction between the oxide traps and the conduction channel is thus suppressed due to the large separation of most carriers from the interface and the oxide traps. The generation of LFN through the carrier trapping and de-trapping process near the Si/SiO_2 interface become less probable. Hence, in the subthreshold region, mobility fluctuation noise behaviors are observed in the investigated devices, instead of the number fluctuation ones.

The empirical relation of Hooge mobility fluctuation model is:

$$\frac{S_{Id}(f)}{I_d^2} = \frac{\alpha_H}{fN} \tag{1}$$

with α_H the Hooge parameter and N the total number of carriers under the gate. Equation (1) needs the knowledge of N in weak inversion.

Starting from the general equation of the drain current

$$I_d = g[V(x)]\frac{dV(x)}{dx} = W\mu Q_i(x)\frac{dV(x)}{dx} \tag{2}$$

where $g[V(x)]$ is the channel conductance for unit length, $V(x)$ the electron quasi-Fermi potential at x along the channel, $W = 2H_{fin}$ is the total channel width and $Q_i(x)$ is the carrier charge density per unit area in the channel at x, the subthreshold current of lightly-doped symmetrical long-channel double-gate FinFETs can be expressed as [8]:

$$I_d = \mu\frac{W}{L}kTn_iW_{fin}e^{\frac{q(V_{gs}-\Delta\phi)}{kT}}(1-e^{-\frac{qV_{ds}}{kT}}) \tag{3}$$

with $\Delta\Phi$ the work function of both the top and bottom gate electrodes with respect to the almost-intrinsic silicon.

As described in [8], the electric potential ψ across the silicon body is obtained by integrating the Poisson's equation twice, and β is a constant used in the solution of ψ and to be determined from the boundary condition in different operation regions. In the subthreshold region, both $\beta_s, \beta_d << 1$, where β_s, β_d are the β values at source and drain sides respectively. From both the surface potential expression ψ_s and Gauss's Law applied at the oxide/silicon interface, a β-dependent expression $f_r(\beta)$ is obtained as

$$f_r(\beta) = \frac{q}{2kT}(V_{gs} - V_o - V(x)) \tag{4}$$

with

$$V_o = \Delta\phi + \frac{2kT}{q}\ln[\frac{2}{W_{fin}}\sqrt{\frac{2\varepsilon_{si}kT}{q^2 n_i}}] \quad (5)$$

In the subthreshold region, $f_r \sim ln\beta$, thus β can be derived as:

$$\beta = e^{\frac{q}{2kT}[V_{gs}-V_o-V(x)]} \quad (6)$$

The carrier charge density per unit area for lightly-doped FinFET device is derived in [8] as:

$$Q_i(x) = 8\frac{\varepsilon_{si}}{W_{fin}}\frac{kT}{q}\beta\tan\beta \quad (7)$$

For $\beta << 1$ in the subthreshold region, we have $tan\beta \approx \beta$ and substitute (5) and (6) into (7), we have:

$$Q_i(x) \approx 8\frac{\varepsilon_{si}}{W_{fin}}\frac{kT}{q}\beta^2 = qn_i W_{fin} e^{\frac{q}{kT}[V_{gs}-\Delta\phi-V(x)]} \quad (8)$$

Hence the total number of carriers in the channel is finally derived as

$$N = \frac{W}{q}\int_0^L Q_i dx \quad (9)$$

With the help of (2), we can transform the previous integration variable from x to $V(x)$ and together with (3) and (8), the final N expression can be integrated out as:

$$N = \frac{W^2\mu}{qI}\int_0^{V_{ds}} Q_i^2 dV = \frac{L^2}{2\mu kT}\frac{1+e^{\frac{-qV_{ds}}{kT}}}{1-e^{\frac{-qV_{ds}}{kT}}} I_d \quad (10)$$

Substitute (10) into (1), the expression of S_{Id}/I_d^2 from the $1/f$ noise Hooge mobility fluctuation model is

$$\frac{S_{Id}(f)}{I_d^2} = \frac{\alpha_H}{fN} = \frac{\alpha_H}{f}\frac{2\mu kT}{L^2}\frac{1-e^{\frac{-qV_{ds}}{kT}}}{1+e^{\frac{-qV_{ds}}{kT}}}\frac{1}{I_d} \quad (11)$$

For very low drain biases, $V_{ds} << kT/q$, (11) can be written as

$$\frac{S_{Id}(f)}{I_d^2} = \frac{\alpha_H}{fN} = \frac{\alpha_H}{f}\frac{q\mu}{L^2}V_{ds}\frac{1}{I_d} \quad (12)$$

For very large drain biases, $V_{ds} >> kT/q$, (11) can be written as

$$\frac{S_{Id}(f)}{I_d^2} = \frac{\alpha_H}{fN} = \frac{\alpha_H}{f}\frac{2\mu kT}{L^2}\frac{1}{I_d} \quad (13)$$

3 MODEL VERIFICATION

The device fabricated for model verification is as follows: The n-channel FinFETs were fabricated on 8" silicon-on-insulator (SOI) substrates with 120-nm thick Si (100) film with boron doping of 10^{15} cm^{-3} on a 150-nm buried oxide. As a hard mask for definition of the Si fin, 60 nm of SiO_2 was deposited. After patterning using a 248-nm lithography and plasma etching, fins of ~ 140 nm in width were obtained. The hard mask was retained for the protection of the fin in a subsequent gate-etch process. A 2-nm sacrificial oxide was then grown on the fin sidewalls to repair the damage caused by the plasma etching. Following its removal, a 9-nm SiO_2 was used as the gate dielectric before depositing 130-nm amorphous silicon (α-Si) as the gate electrode. After gate pattering and etching, the source/drain and α-Si gate were implanted using arsenic with a dose of 4×10^{15} cm^{-2} and energy of 30 keV for n-FETs. It was followed by the standard metal contact formation and sintering processes. Figure 1 shows a schematic of the double-gate FinFET device with important dimensions indicated.

By adding an ideality factor m related to gate biases into (3), we have the modified subthreshold current expression:

$$I_d = \mu\frac{W}{L}kTn_i W_{fin} e^{\frac{q(V_{gs}-\Delta\phi)}{mkT}}(1-e^{-\frac{qV_{ds}}{kT}}) \quad (14)$$

From DC measurements, conduction parameters have been extracted [10] and are summarized in Table 1. These parameters describe perfectly the above-threshold conduction in the ohmic region as well as the subthreshold current.

LFN measurements were performed with an HP35670A Dynamic Signal Analyzer in the frequency range of 1 Hz – 10 kHz. SR570 Low-Noise Current Preamplifiers were used for direct measurements of the channel current noise spectral density. Batteries provide all supplies at low-level signal stages in order to reduce any external LFN.

In the subthreshold conduction, typical variation of the normalized drain current noise spectral density S_{Id}/I_d^2 (f = 10 Hz) are given in Figure 2 versus the drain current I_d at V_{ds} = 100 mV. The normalized variations versus I_d exhibit a slope close to -1 and show that the mobility fluctuation model (Hooge's theory) is involved [11]. (In the McWhorter model S_{Id}/I_d^2 is independent of the drain current). From these variations, α_H following (11) have been extracted and reported in Figure 3 and we obtain $\alpha_H \approx 1.3\times10^{-3}$.

In order to verify (11), $1/f$ noise measurements performed in the subthreshold region S_{Id}/I_d versus V_{ds} is also shown in Figure 4. A linear increase with low V_{ds} values is observed as described by (12) and a plateau is reached for high V_{ds} values ($S_{Id}/I_d = 1.039\times10^{-15}$ A/Hz) as described by (13). In Figure 4, the computed values of S_{Id}/I_d using (11) and taking into account the value of the various parameters previously extracted are also reported. Good agreement is observed.

It is also clearly shown in Figure 5 that for a given bias condition V_{gs} = 0.1 V and V_{ds} = 100 mV, the normalized drain current noise power spectral density S_{Id}/I_d^2 is decreasing with increasing fin width. From the linear fitting to the plot of $\log(S_{Id}/I_d^2)$ vs. $\log(W_{fin})$, as shown in the inset of Figure 5, the normalized noise power spectral density is

found to be almost inversely proportional to the fin width, i.e., $S_{Id}/I_d^2 \sim W_{fin}^{-1}$ for a given bias condition. This is clear from (3) and (11), since S_{Id}/I_d^2 is inversely proportional to the drain current level I_d, while I_d is in turn proportional to the fin width W_{fin}.

4 CONCLUSION

In conclusion, 1/*f* noise in weak inversion has been described using Hooge's theory. From the drain current equation and the channel conductance expression, the total number of carriers under the gates has been evaluated. This quantity is the main parameter needed to deduce the Hooge parameter α_H in the subthreshold conduction. 1/*f* noise in n-channel double-gate FinFETs has been investigated. These transistors exhibit 1/*f* noise in agreement with Hooge's theory when they are biased in weak inversion due to their volume inversion conduction behavior.

REFERENCES

[1] T. H. Lee, *et al*., "Oscillator phase noise: A tutorial," *IEEE J. Solid-State Circuits*, vol. 35, pp. 326-336, 2000.

[2] Y. K. Choi, *et al*., "Nanoscale CMOS spacer FinFET for the terabit era," *IEEE Electron Device Lett.*, vol. 23, pp. 25-27, 2002.

[3] J. Kedzierski, *et al*., "High-performance symmetric-gate and CMOS-compatible Vt asymmetric-gate FinFET devices," in *IEDM Tech. Dig.*, 2001, pp. 437-440.

[4] Y. K. Choi, *et al*., "Spacer FinFET: Nanoscale double-gate CMOS technology for the terabit era," *Solid State Electron.*, vol. 46, pp. 1595-1601, 2002.

[5] G. Reimbold, "Modified 1/f trapping noise theory and experiments in MOS transistors biased from weak to strong inversion – Influence of interface states," *IEEE Trans. Electron Devices*, vol. 31, pp. 1190-1198, 1984.

[6] F. N. Hooge, "1/f noise is no surface effect," *Phys. Lett. A*., vol. 29, pp. 139, 1969.

[7] F. N. Hooge, *et al*., "Experimental studies on 1/f noise," *Rep. Prog. Phys.*, vol. 44, pp. 497-532, 1981.

[8] Y. Taur, *et al*., "A continuous, analytic drain-current model for DG MOSFETs," *IEEE Electron Device Lett.*, vol. 25, pp. 107-109, 2004.

[9] Y. Taur, "Analytic solutions of charge and capacitance in symmetric and asymmetric double-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 48, pp. 2861-2869, 2001.

[10] G. Ghibaudo, *Characterization methods for submicron MOSFETs,* Kluwer Academic Publishers, 1995.

[11] M. Valenza, *et al*., "Overview of the impact of downscaling technology on 1/f noise in p-MOSFETs to 90nm," *IEE Proc.-Circuits Devices Syst.*, vol. 151, pp. 102-110, 2004.

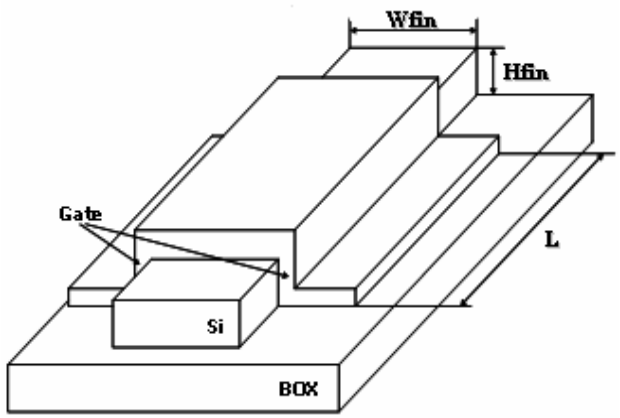

Figure 1. Schematic of a double-gate FinFET device, showing important dimensions: fin width (W_{fin}), fin height (H_{fin}) and gate length (L).

TABLE 1. Conduction parameters extracted at V_{ds} = 100mV for device dimensions: W_{fin} = 0.14 μm, H_{fin} = 0.12 μm, L = 5 μm.

C_{ox} F/cm^2	V_T V	μ cm^2/Vs	ΔL μm	θ V^{-1}	R_S kΩ	S mV/dec	m
3.83×10^{-7}	0.13	228	0.15	0.13	1.346	71.2	1.186

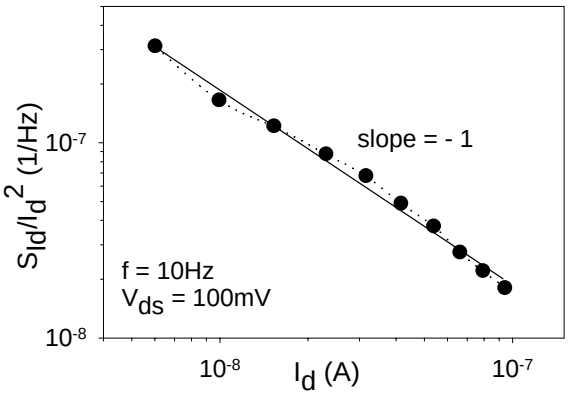

Figure 2. Normalized drain current noise power spectral density S_{Id}/I_d^2 vs. drain current I_d at f = 10 Hz and V_{ds} = 100 mV in the subthreshold region. -●- experimental data. Solid line: model fitting by (11). The slope (-1) agrees with Hooge's theory. (W_{fin} = 0.14 μm, H_{fin} = 0.12 μm, L = 5 μm).

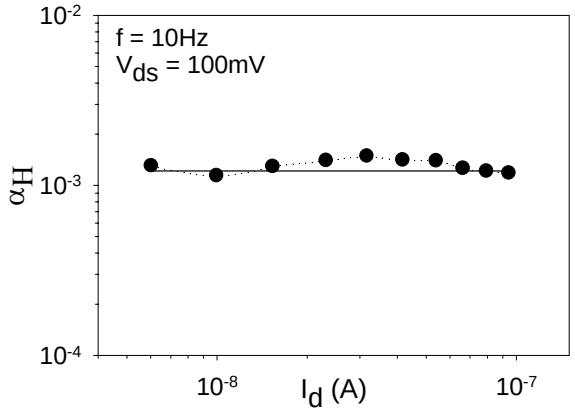

Figure 3. Hooge's parameter α_H vs. drain current I_d at f = 10 Hz and V_{ds} = 100 mV in the subthreshold region. -●- extracted from experimental data. Solid line: average value of α_H (around 1.3×10^{-3}).

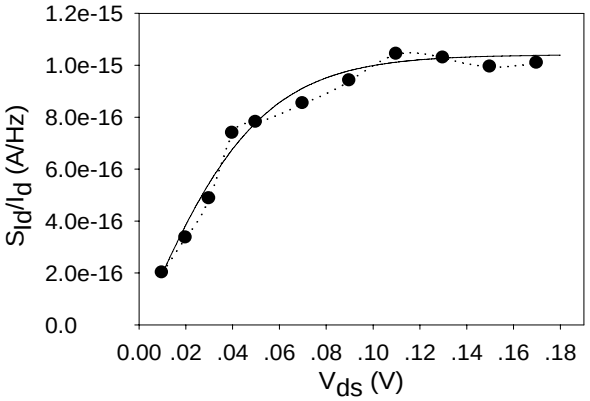

Figure 4. Variations of S_{Id}/I_d vs. drain voltage V_{ds} at f = 10 Hz in the subthreshold region. -●- experimental data. Solid line: model fitting by (11). Good agreement between experimental and computed data showing the validity of (11).

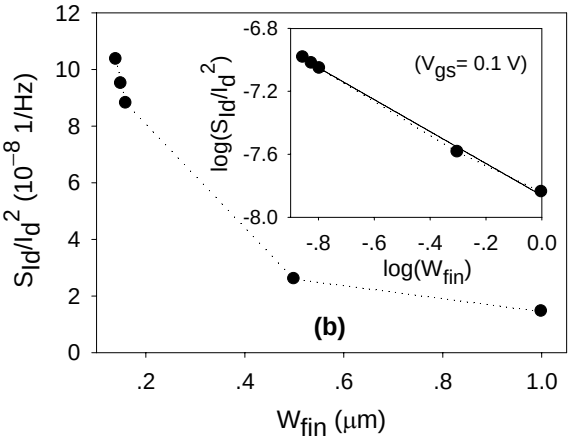

Figure 5. Normalized drain current noise power spectral density of FinFETs with different fin widths extracted at V_{gs} = 0.1 V and V_{ds} = 100 mV. The inset shows the logarithm values of S_{Id}/I_d^2 vs. W_{fin}. Symbol: experimental data, Solid line: linear fitting.

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